CPEG 340 Project
VHDL Implementation
[Total marks = 15% --- Report = 8% Individual Assessment = 7%]
Due date – December 23, 2021 @ 2 pm

Using the algorithm/high-level program provided to you in the assignment and the FSMD and processor datapath that you submitted for the assignment, you are to implement the processor datapath using VHDL under Quartus. You are free to select the structural hierarchy of the implementation; the implementation could be behavioral, structural, or a mixed implementation. Test your implementation by simulating the VHDL implementation in ModelSim and provide relevant timing diagrams. Provide detailed discussion on the timing diagrams with respect to the accuracy of your implementation.

Deliverables:

Write a report that explains the implementation, analysis, and evaluation of the VHDL implementation and its testing. It is critical that you explain the Whys and Hows of your technical work. Include all relevant and necessary code. Also include any drawings of FSMD and datapath as part of your report. Students will work in the same groups they made for the assignment submission. The names and student IDs of the group members MUST be clearly written on the first page of the report. Submit a zip file that contains your code files, VHDL files and technical report (in PDF format) by **December 23 @ 2pm.**