Kuwait University
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ELECTRONICS III

Memory Circuits

Chapter 16 - Part (2)

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Semiconductor Memories

- Semiconductor Memories has two type:
  1. Random Access memory (RAM)
  2. Read only memory (RoM)

1 Random Access memory (RAM):

a. Static RAM "SRAM"

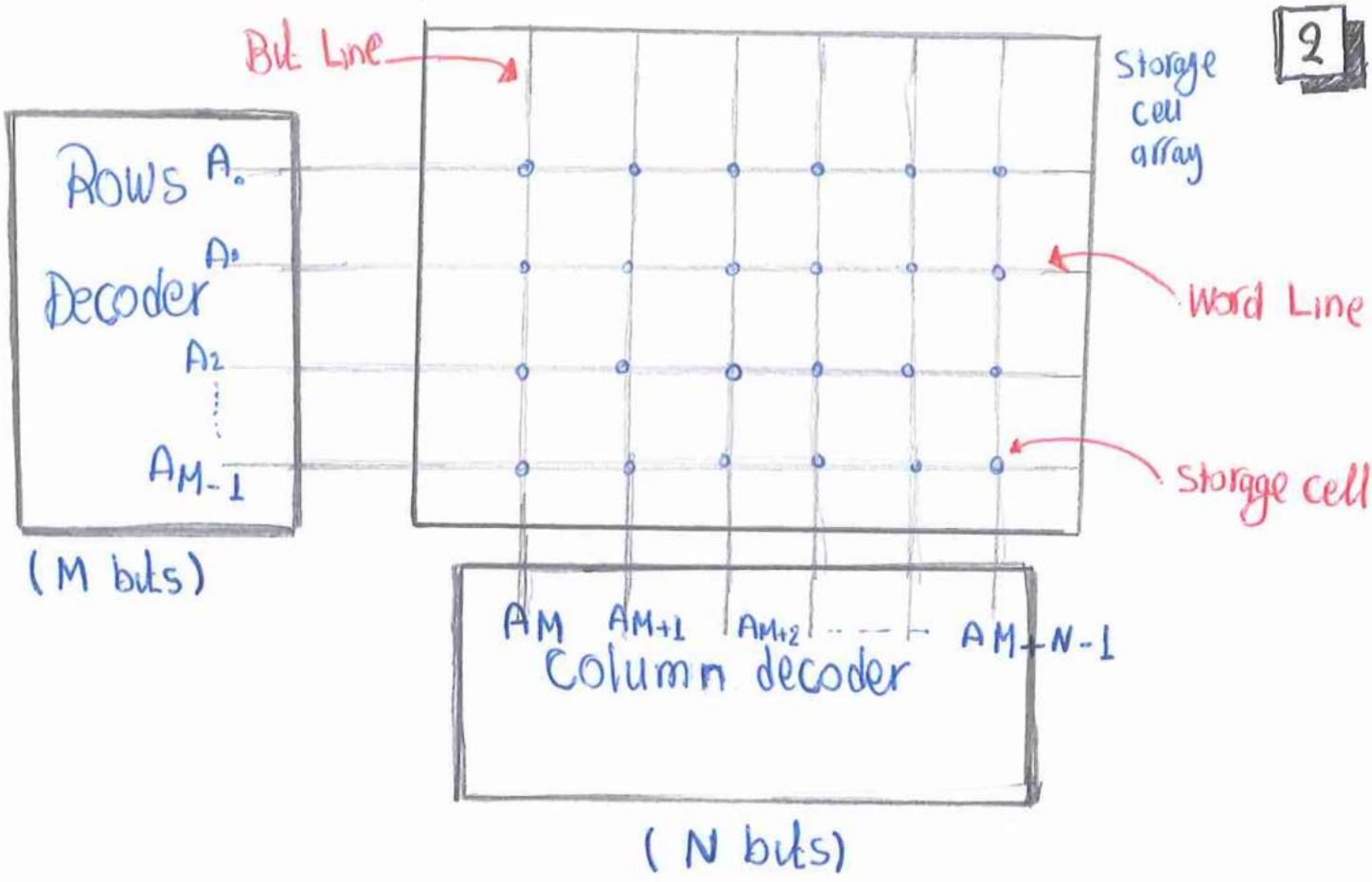
b. Dynamic RAM "DRAM"

and This type of Memory can Read and write.

2 Read only memory (RoM):

a. Programable RoM "PRoM"

b. Erasable PRoM "EPRoM"



⊙ cell Matrix : * 2^M rows

* 2^N Column

and $N = M$ (square Matrix)

▢ Total storage capacity $C_T = 2^M \times 2^N = 2^{M+N}$

Example:

1 M bit memory is orginZied in a squre memory with $M = N = 10$

Find: * cell rows and columns

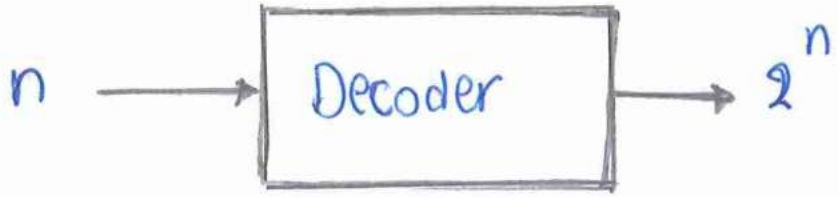
* total capacity of cell

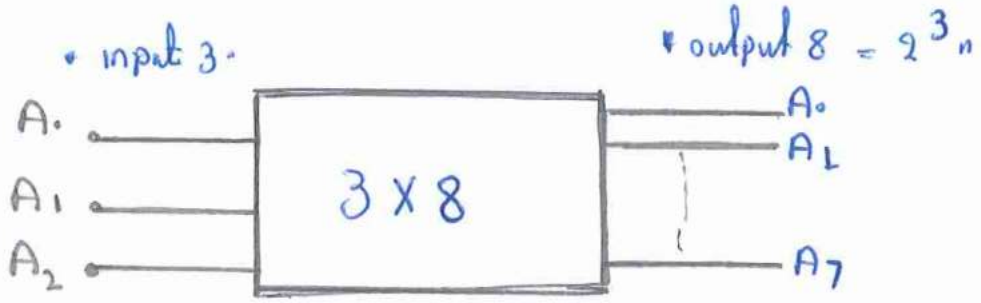
Row = $2^M = 2^{10}$ Word Line

Column = $2^N = 2^{10}$ But Line

Total capacity = $2^{10} * 2^{10} = 2^{20}$ cells

Decoder:





* M & N can determine the capacity of Memory.

Read: All bits on single word line are activated and only one bit is selected.

Write: Word Line is Activated 0 or 1 applied to the input interface direct to activated Line.

Example:

Assume 64 bit memory orginzed in a square Memory $M = N = 3$.

(a) Find cell Matrix Size

(b) Show how can you read The content of Address $[57]_{10}$

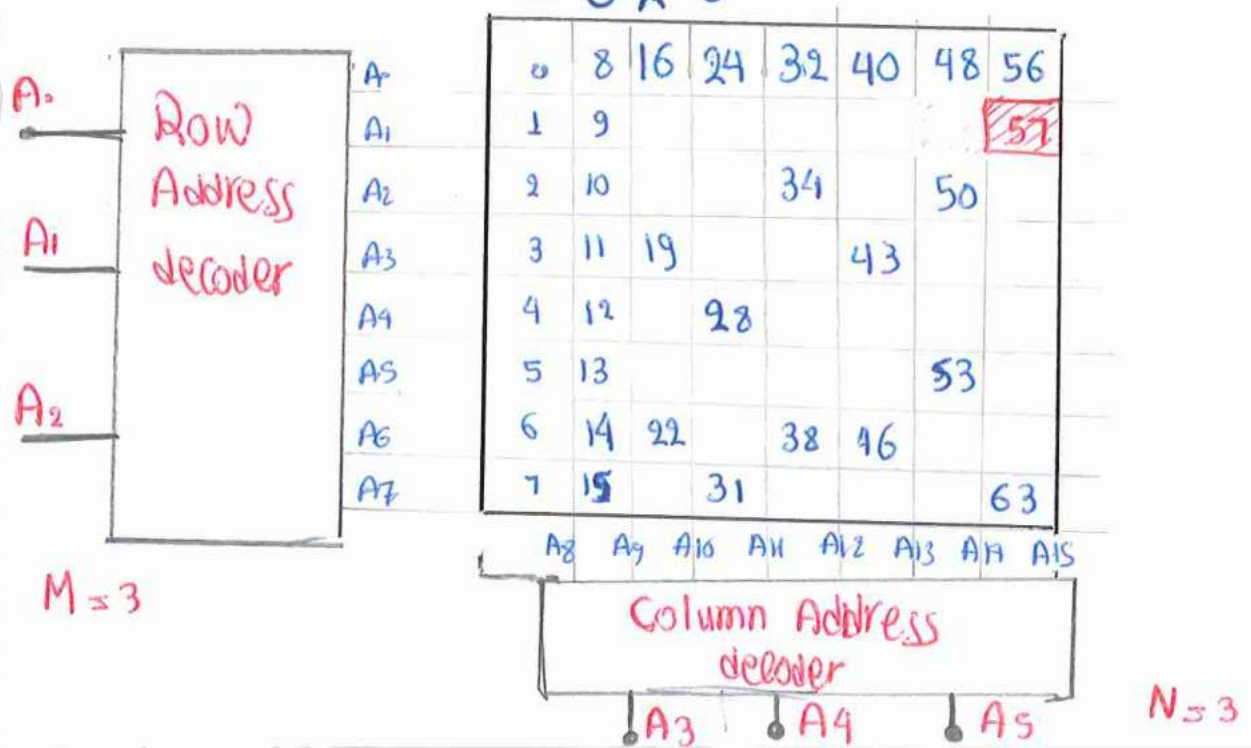
(c) Draw Memory cell indicate.

Solution

(a) Cell Size $= 2^M * 2^N$

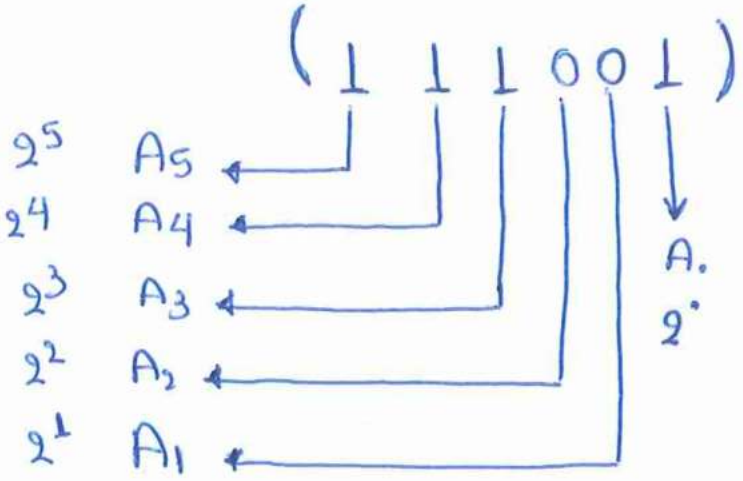
$= 2^3 * 2^3$

$= 8 \times 8$



$(57)_{10} = (111001)_2$ Bainry

Decimal



Memory chip- timing:

(a) memory access time: time between initiation of Read operation and the apperance of the output data.

(b) memory cycle time: The minimum time allowed between 2 consecutive memory operations.

↳ (Read, write)

A 1.5-V, 1-Gbit dynamic RAM (called DRAM) by Hitachi uses a 0.16-µm process with a cell size of 0.38 × 0.76 μm^2 in a 19 × 38 mm^2 chip. What fraction of the chip is occupied by the I/O connections, peripheral circuits, and interconnect?

* Cell Area = RAM capacity * cell size

$= 1 * 10^9 [(0,38 * 10^{-6}) * (0,76 * 10^{-6})]$

$= 0,289\ mm^2$

* Total chip area $= (19 * 10^{-3}) * (38 * 10^{-3})$

$= 0,722\ mm^2$

* The space occupied by I/O = Total Area chip - Total cell area

$= 0,722 - 0,289$

$= 0,433\ mm^2$

* The fraction of chip area occuipied $= \frac{0,433}{0,722} * 100$

$= 60\ \%$

A 4-Mbit memory chip is partitioned into 32 blocks, with each block having 1024 rows and 128 columns. Give the number of bits required for the row address, column address, and block address.

7

* The number of row in each block 1024

number of bits in row = $1024 = 2^{10}$

∴ The number of bits required for row = 10

* number of columns 128

∴ $128 = 2^7$

number of bits required for coulums = 7

* number of blocks in 1 M-bit for 32 block

$32 = 2^5$

∴ The number of bits for 1 Mbit is 5

∴ for 4 Mbit = $2^2 * 2^5 = 2^7$

∴ The number of bit for 4 Mbit = 7

RAM (Random access memory):

a. Static RAM: latches can hold Large Size

b. Dynamic memory: capacitors can store data.

Dynamic

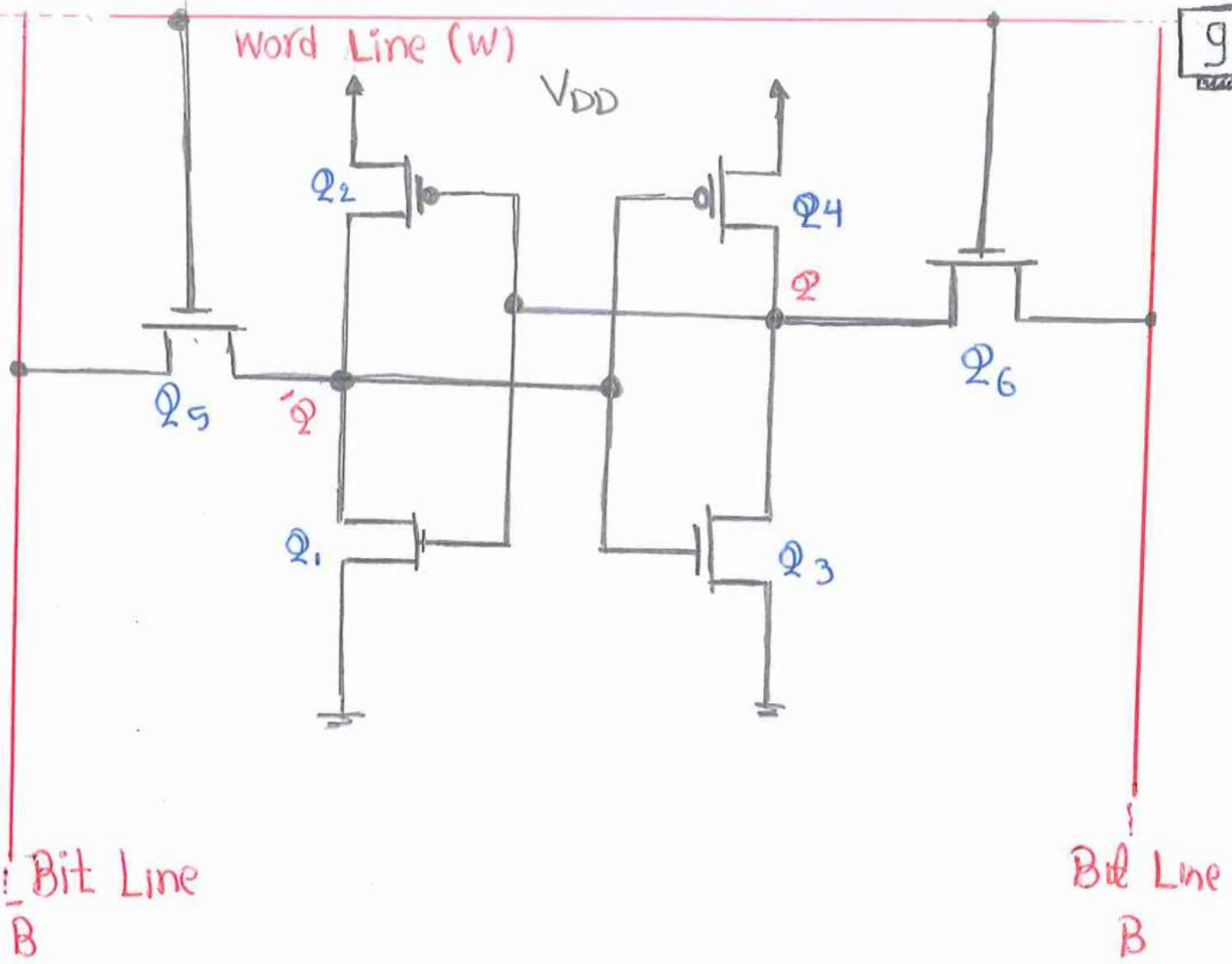
* In RAM The size will be variable due to C charge OR Discharge

* In RAM When power off All data Will be Lost.

a. Static memory cell (SRAM)

The CMOS technology can used as static memory cell which is a flip-flop comprising two cross-coupled inverter and two Access Transistor.

- Draw The CMOS implementation of SRAM.



* Q_5 and Q_6 are Access Transistor
* Q_6 connected to Bit line B and Q_5 connected to Bit Line $\bar{B}$.

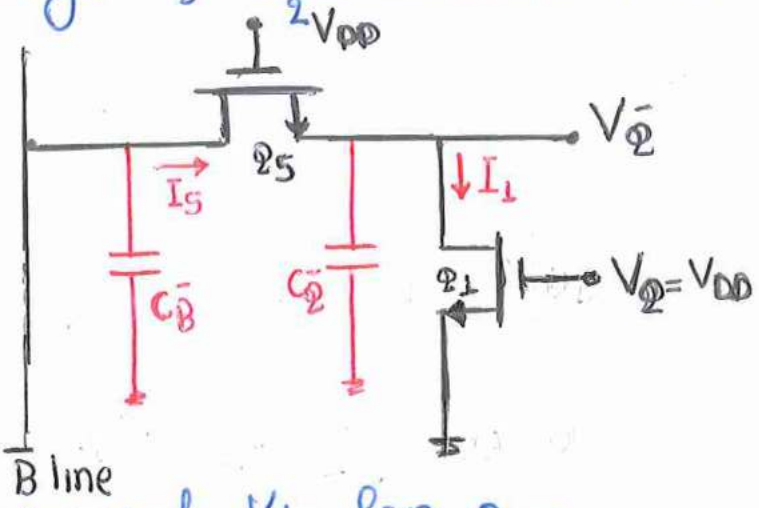
The operation in SRAM: (1) Read operation
(2) write operation

1 Read operation:

* Assume cell storing 1, at this case Q will be high at V_{DD} and $\bar{Q}$ will be Low at 0V.

$$\therefore V_Q = V_{DD} \quad \& \quad V_{\bar{Q}} = 0$$

* But Lines always precharge by $\frac{V_{DD}}{2}$ and raised to V_{DD} (B & $\bar{B}$)



* capacitor $C_{\bar{B}}$ will charge by $\bar{B}$ line, The The current will folw through $C_{\bar{Q}}$.
* This make Q_1 ON, but we Should know that $V_{\bar{Q}}$ will not exceed V_{tn} for Q_3.

* Q_5 in Saturation So:

$$I_5 = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_5 \left(V_{DD} - V_{tn} - V_{\bar{Q}}\right)^2$$

* Q_1 Triode:

$$I_1 = \mu_n C_{ox} \left(\frac{W}{L}\right)_1 \left[\left(V_{DD} - V_{tn}\right) V_{\bar{Q}} - \frac{1}{2} V_{\bar{Q}}^2\right]$$

* but $I_1 = I_5$

$$\therefore \frac{V_{\bar{Q}}}{V_{DD} - V_{tn}} = 1 - \frac{1}{1 + \frac{(W/L)_5}{(W/L)_1}}$$

$$\therefore \frac{(W/L)_S}{(W/L)_1} \leq \frac{1}{1-\left(\frac{V_{\bar{Q}}}{V_{DD}-V_{tn}}\right)} - 1$$

we can say also $(W/L)_S = (W/L)_a$ refer to access transistor and $(W/L)_1 = (W/L)_n$ refer to Q_n in the inverter.

* The read delay time can be found by

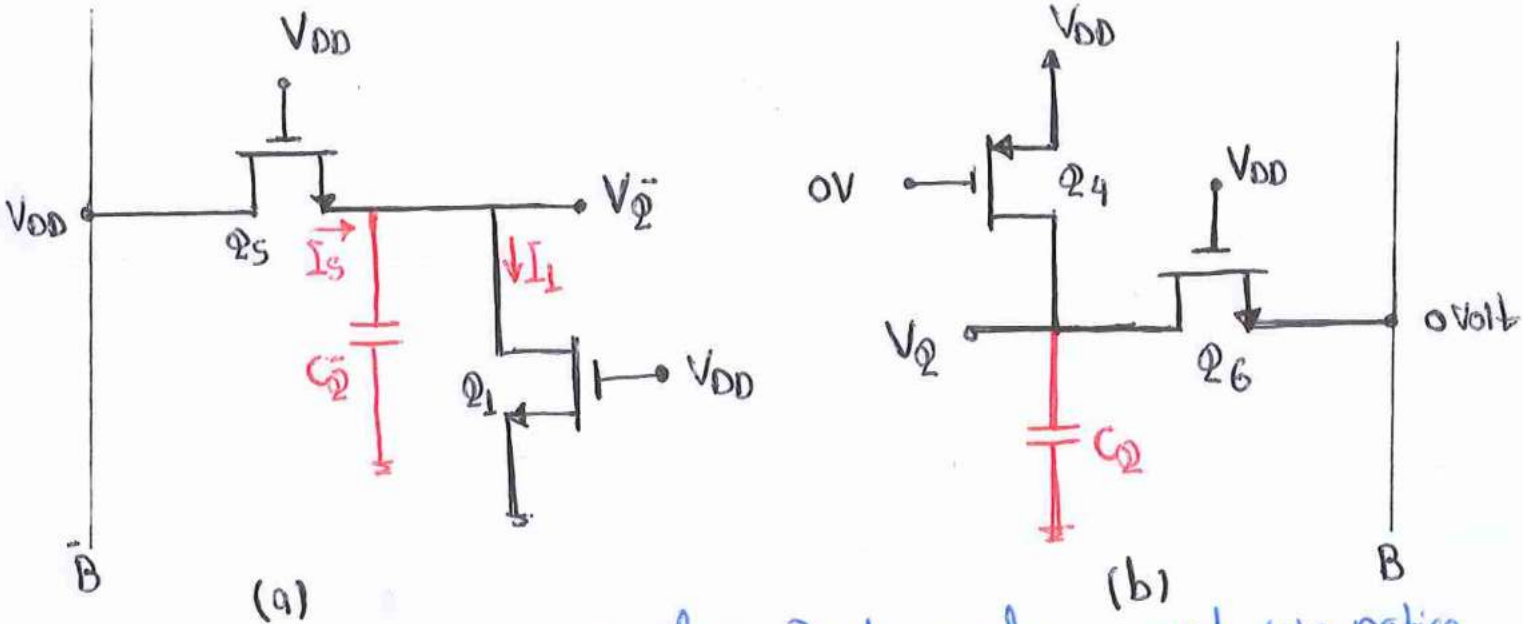
$$\Delta t = \frac{C_{\bar{B}}\, \Delta V}{I_S}$$

* Where:
  * $C_{\bar{B}}$: The capacitance for $\bar{B}$ line
  * ΔV : The increment change and it appear from the sense amplifer (0,1 ~ 0,2 V)

* Note That:
  * The sense amp. is op. Amp comparator circuit the input will be B & $\bar{B}$
    * If $B > \bar{B}$ output is 1
    * If $B < \bar{B}$ output is 0

2 Write operation:

* Let The SRAM cell Storage Logic 1 $V_Q = V_{DD}$, $V_{\bar{Q}} = 0$
* we need to write Zero So:
  * B Line = 0 V
  * $\bar{B}$ line = V_{DD}
  * W line = V_{DD}



* circuit (a) The same circuit in Read operation. and we notice That $V_{\bar{Q}}$ will not exceed $V_{tn}(Q_3)$. So we can't use it
* in circuit (b) Q_4 & Q_6 will be on, And The capacitor will start Discharge, and we should know that V_Q should be less That $V_{tn}(Q_1)$
* Q_4 in Sat. * Q_6 in Triode

$$I_4 = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_4 (V_{DD} - |V_{tp}|)^2$$

$$I_6 = \mu_n C_{ox} \left(\frac{W}{L}\right)_6 \left[(V_{DD} - V_{tn}) V_Q - \frac{1}{2} V_Q^2\right]$$

and $I_4 = I_6$

$$\therefore \frac{V_Q}{V_{DD} - V_{tn}} = 1 - \sqrt{1 - \frac{\mu_p}{\mu_n} \left(\frac{(W/L)_1}{(W/L)_6}\right.}$$

* So in SRAM

$$\frac{(W/L)_P}{(W/L)_n} \ll \frac{\mu_n}{\mu_p} \left[1 - \left(1 - \frac{V_Q}{V_{DD} - V_{tn}}\right)\right]^2$$

V_Q = (V_{Ln})

⇒ That's mean SRAM depend on Mobility

Example: In SRAM

$\mu_n C_{ox} = 50 \quad \mu A/V^2$

$2.5 \mu_p C_{ox} \leq \mu_n C_{ox}$

$\left(\frac{W}{L}\right)_n = 4/2$

$\left(\frac{W}{L}\right)_p = 10/2$

$(W/L)_{5,6} = 10/2$

$|V_t| = L$

$\gamma = 0,5\ V^{0,5}$

$V_{DD} = 5\ V$

$C_{bit\text{-}Line} = 1\ pF$ and $V_{\bar{Q}} = 0,6$ Volt

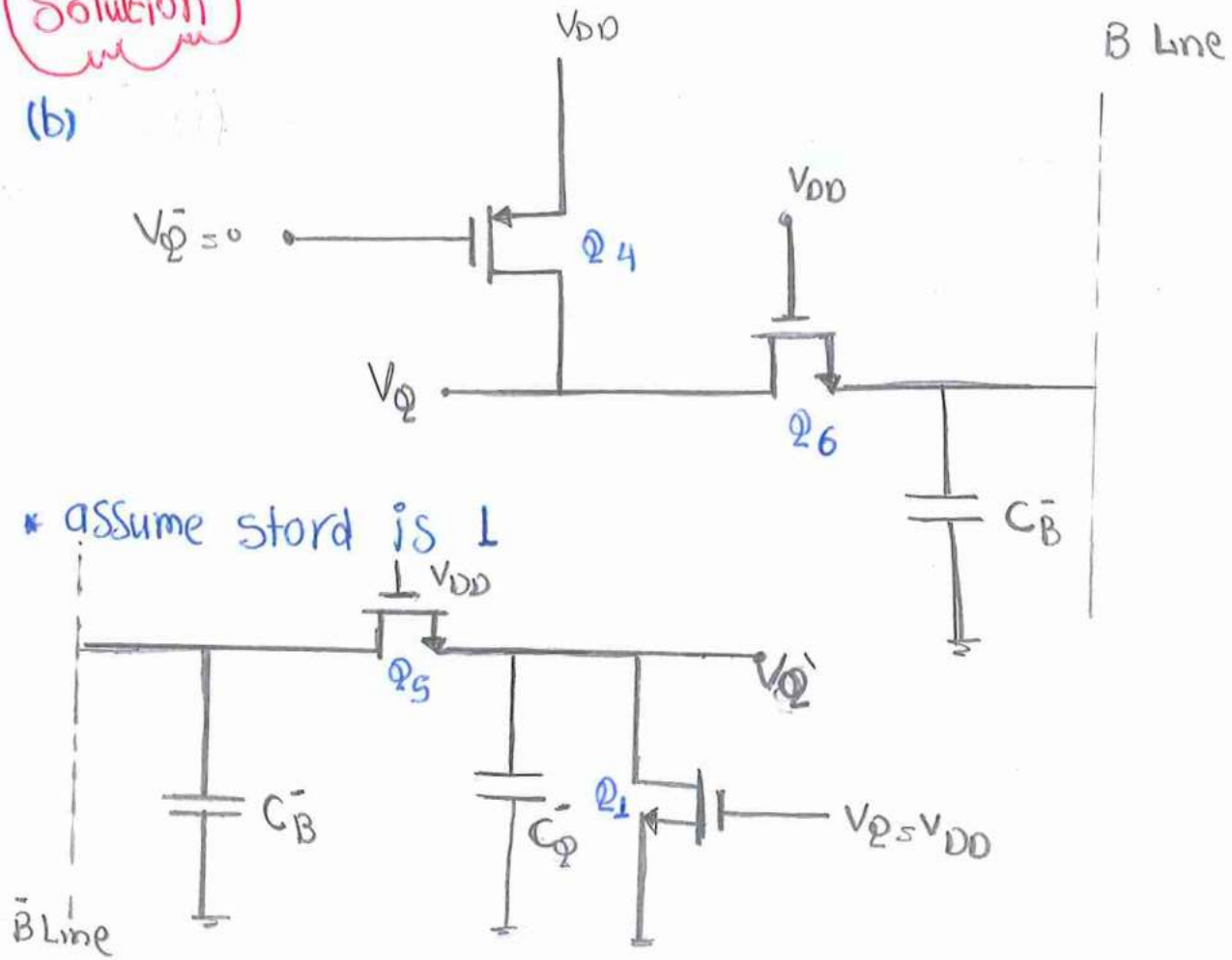
(a) Draw revent circuit in (Read & write operation)

(b) Find delay time (Read) of SRAM. assume initial Stord is L

(c) $\frac{(W/L)_P}{(W/L)_Q}$ for maximum Area.

Solution

(b)



* $Q_6 \longrightarrow$ off

$V_S = V_D = V_G = V_{DD}$

* $\bar{B}$ Must be 0,2 Volt and detected by sense Amplifier.

(Discharge Q_5 and Q_1)

(Q_5) : $V_{DS} = V_{DD}$ & (Q_1): $V_D < \frac{V_{DD}}{2}$

$$\frac{V_{\bar{Q}}}{V_{DD} - V_{tn}} = 1 - \frac{1}{1 + \frac{(W/L)_5}{(W/L)_1}}$$

$$\therefore I_1 = \mu_n C_{ox} \left(\frac{W}{L}\right)_1 \left[(V_{DD} - V_t) V_{\bar{Q}} - \frac{V_{\bar{Q}}^2}{2} \right]$$

$$I_5 = \frac{1}{2} K_{ns} \left[V_{DD} - V_{\bar{Q}} - V_{tS} \right]^2$$

and V_t has body effect $V_{tS} = V_{t_0} + \gamma \left[\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F} \right]$

$$\therefore V_{tS} = 1 + 0,5 \left[\sqrt{V_{\bar{Q}} + 2 \cdot 0,6} - \sqrt{2\phi_f} \right]$$

$$\therefore I_5 = 0,5 \, mA$$

$$\therefore \Delta t = \frac{C_{\bar{B}} \cdot \Delta V}{I_5} = \frac{1 * 10^{-12} * 0,2}{0,5 * 10^{-3}} = 0,4 \, nS$$

D A 6T SRAM cell is fabricated in a 0.13-μm CMOS process for which $V_{DD} = 1.2$ V, $V_t = 0.4$ V, and $\mu_n C_{ox} = 500\ \mu A/V^2$. The inverters utilize $(W/L)_n = 1$. Each of the bit lines has a 2-pF capacitance to ground. The sense amplifier requires a minimum of 0.2-V input for reliable and fast operation.

(a) Find the upper bound on W/L for each of the access transistors so that V_Q and $V_{\bar{Q}}$ do not change by more than V_t volts during the read operation.
(b) Find the delay time Δt encountered in the read operation if the cell design utilizes minimum-size access transistors.
(c) Find the delay time Δt if the design utilizes the maximum allowable size for the access transistors.

(a) $$\frac{(W/L)_5}{(W/L)_1} = \frac{1}{\left(1 - \frac{V_t}{V_{DD} - V_t}\right)^2} - 1 = \frac{1}{\left(1 - \frac{0,4}{1,2 - 0,4}\right)^2} - 1$$

$$\therefore \frac{(W/L)_5}{(W/L)_1} = 3$$

(b) $$\Delta t = \frac{C_B \cdot \Delta V}{I_5}$$

$$I_5 = \frac{1}{2} K_n' \left(\frac{W}{L}\right)_5 \left(V_{DD} - V_t - V_{\bar{Q}}\right)^2$$

$$\therefore \frac{(W/L)_5}{(W/L)_1} = \frac{1}{\left(1 - \frac{V_{\bar{Q}}}{V_{DD} - V_t}\right)^2} - 1$$

$$1 = \frac{1}{\left(1 - \frac{V_{\bar{Q}}}{1,2 - 0,4}\right)^2} - 1$$

$$\therefore V_{\bar{Q}} = 0,23\ V$$

$\therefore I_5 = \frac{1}{2}(500*10^{-6})(1)(1,2-0,4-0,23)^2$

$= 81,225\ \mu A$

$\therefore \Delta t = \frac{2*10^{-12}*0,2}{81,225*10^{-6}} = 4,93\ ns$

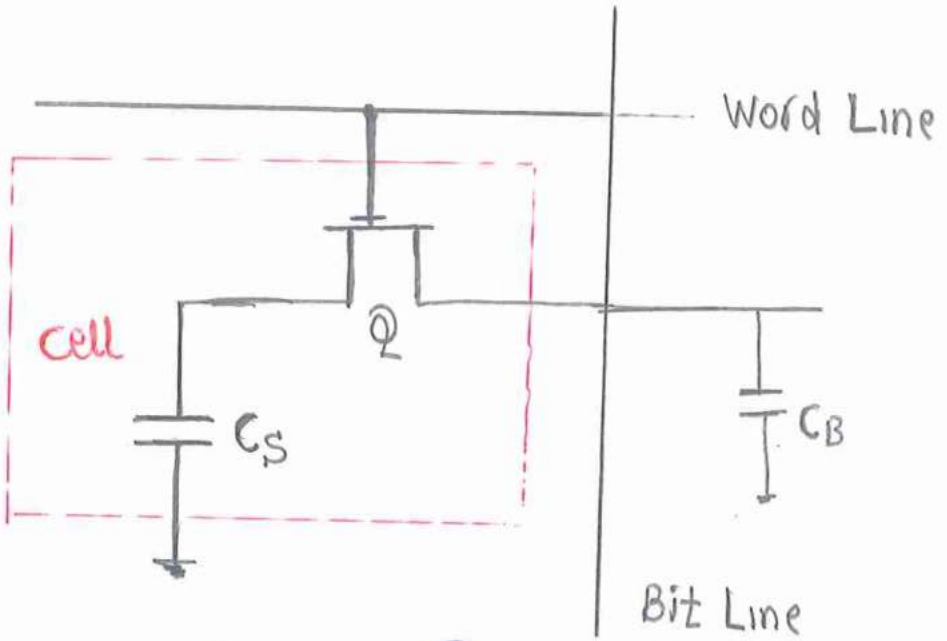
(c) $V_{\bar{Q}} = V_{tn} = 0,4\ V$ & $(W/L)_5 = 3$

$\therefore I_5 = \frac{1}{2}(500*10^{-6})*3(1,2-0,4-0,4)^2$

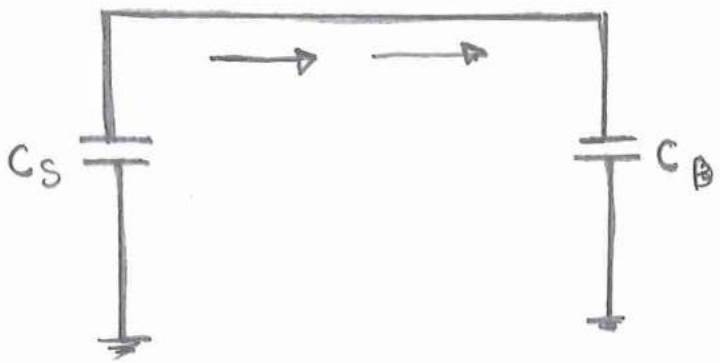
$= 120\ \mu A$

$\Delta t = \frac{C_B \Delta V}{I_5} = \frac{2*10^{-12}*0,2}{120*10^{-6}} = 3,34\ ns$

b Dynamic memory cell: (DRAM)



* The one Transistor dynamic RAM Cell
  * all Storge capacitors are Activated
  * Bit Line charged Full $\frac{V_{DD}}{2}$
  * connection between C_S, C_B toword C_B



* $Q = CV$

$$C_S V_S + C_B \frac{V_{DD}}{2} = (C_B + C_S) V_{Final}$$

"initial state" "final state"

$$V_{Final} = \frac{V_{DD}}{2} + \Delta V$$

$$\Delta V = \frac{C_S}{C_B + C_S} * \left(V_{CS} - \frac{V_{DD}}{2}\right)$$

$$\therefore \Delta V \simeq \frac{C_S}{C_B} \left(V_{CS} - \frac{V_{DD}}{2}\right)$$

* If we stord 1 , So $V_{CS} = V_{DD} - V_t$

* If we stord 0 , So $V_{CS} = 0$

Example:

In Dynamic memory cell

$C_S = 50M$

$C_B = 500MF$

$V_t = 0,9\ V$

$V_{DD} = 1,4\ V$

If Reading 1 $\longrightarrow$ $V_S = 1,4 - 0,4 = V_{DD} - V_t = L$

$$\Delta V = \frac{C_S}{C_B} \left(V_S - \frac{V_{DD}}{2}\right)$$

If Reading Zero

$V_S = 0$

$\therefore \Delta V = -\frac{C_S}{C_B} * \frac{V_{DD}}{2}$

$\Delta V = \frac{-50}{500} * \frac{1,4}{2}$

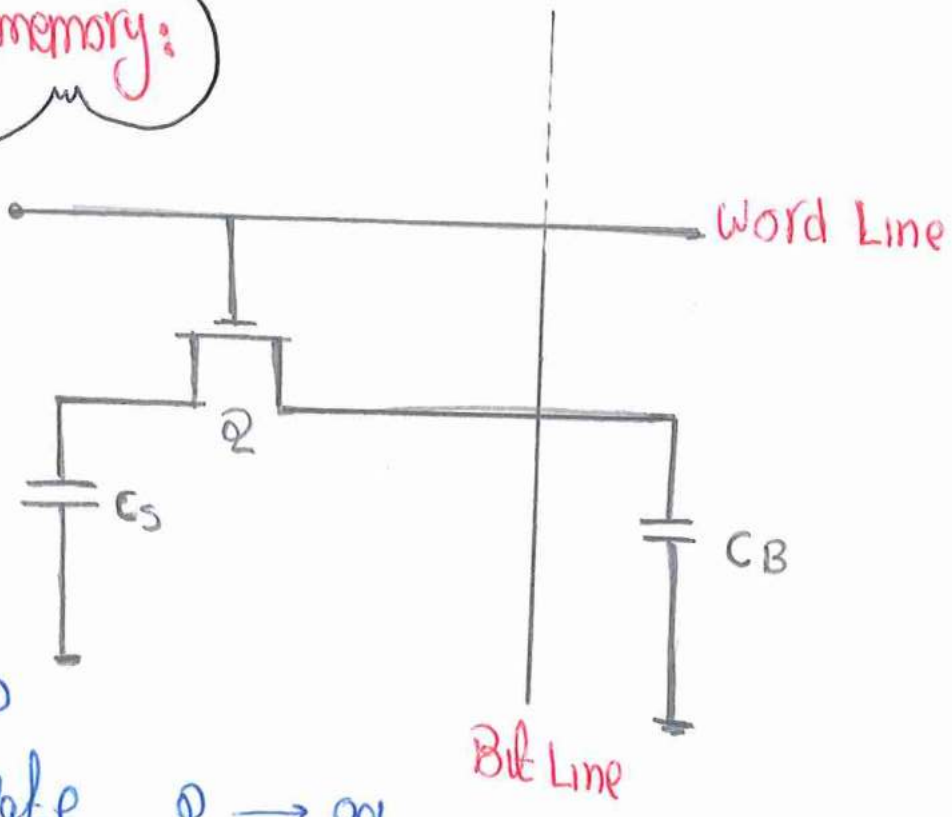
If $\Delta V > 0,2$

Sense Amplifer conduct

$\Delta V < 0,2$

no detect

Write in Dynamic memory:



- V_{DD} at bit Line
- C_B charge to V_{DD}
- word Line activate Q → on

- V_{cs} charge $V_{DD} - V_t$ at ONE

- at zero charge $V_S = 0$

Read in Dynamic memory:

* precharge bit line B to $\frac{V_{DD}}{2}$
* Activate wordline
* capacitor and bit line share charge
  * If capacitor was discharge (C_B), bit line decrease.
  * If capacitor was charged (C_B), bit line increase.
* Sense Amp. will connect to bit line to determine If 0 or 1

16.30 For a particular DRAM design, the cell capacitance $C_S = 35$ fF and $V_{DD} = 1.2$ V. Each cell represents a capacitive load on the bit line of 0.8 fF. Assume a 20-fF capacitance for the sense amplifier and other circuitry attached to the bit line. What is the maximum number of cells that can be attached to a bit line while ensuring a minimum bit-line signal of 25 mV? How many bits of row addressing can be used? If the sense-amplifier gain is increased by a factor of 4, how many word-line address bits can be accommodated?

$C_S = 35 * 10^{-15}$ F $V_{DD} = 1,2$

$\Delta V = 25$ mV

Each cell has 0,8 fF

∴ total bit capacitance 0,8n fF & 20fF capacitance is attached

∴ $C_B = 0,8n + 20$

∴ $\Delta V = \frac{C_S}{C_S + C_B} \left(\frac{V_{DD}}{2}\right)$

$0,025 = \frac{35 * 10^{-15}}{35 * 10^{-15} + (0,8n + 20) * 10^{-15}} \left(\frac{1,2}{2}\right)$

∴ $n = 981,25$

∴ The max number of cell 1024

* number of bit $1024 = 2^{10}$

∴ number of bits used for rows = 10

* The sense amp gain increase by 4

∴ The change in voltage decrease by 4

$$\frac{0,025}{4} = \frac{35 * 10^{-15}}{(35 * 10^{-15}) + (0,8n + 20) * 10^{-15}} * \left(\frac{1,2}{2}\right)$$

∴ $n = 4131,25 > 4096$

∴ The max number of cell 4096

number of bit = $4096 = 2^{12} \longrightarrow 12$

The Sense - Amplifier :

The sense Amp is an essential to the proper operation in SRAM & DRAm.

* in Read 1 operation:

$$V_B = \frac{V_{DD}}{2} + \Delta V(1)\, e^{(G_m/C_B)\,t}$$

V_B: Bit line voltage

where $V_B \leq V_{DD}$

* in Read 0 operation:

$$V_B = \frac{V_{DD}}{2} - \Delta V(0)\, e^{(G_m/C_B)\,t}$$

$V_B \geq 0$

* $G_m = g_{m(n)} + g_{m(p)}$

* $g_{m_{(n)}} = K_n (V_{GS} - V_t)$ & $g_{m(p)} = K_p (V_{SG} - |V_{tp}|)$

* $K_n = K_n' \left(\frac{W}{L}\right)_n = \mu_n C_{ox} \left(\frac{W}{L}\right)_n$

Consider the sense-amplifier circuit of Fig. 16.20 during the reading of a 1. Assume that the storage cell provides a voltage increment on the B line of $\Delta V(1) = 0.1$ V. If the NMOS devices in the amplifiers have $(W/L)_n = 0.54\ \mu m/0.18\ \mu m$ and the PMOS devices have $(W/L)_p = 2.16\ \mu m/0.18\ \mu m$, and assuming that $V_{DD} = 1.8$ V, $V_{tn} = |V_{tp}| = 0.5$ V, and $\mu_n C_{ox} = 4\,\mu_p C_{ox} = 300\ \mu A/V^2$, find the time required for v_B to reach $0.9\,V_{DD}$. Assume $C_B = 1$ pF.

$\Delta V(1) = 0,1$ $\quad V_{DD} = 1,8$

$(\frac{W}{L})_n = 0,54/0,18$ $\quad V_t = 0,5$

$(\frac{W}{L})_p = \frac{2,16}{0,18}$ $\quad \mu_n C_{ox} = 4\mu_p C_{ox} = 300\ \mu A/V^2$

$V_B = 0,9\ V_{DD}$ & $C_B = 1pf$

* $g_{m(n)} = \mu_n C_{ox} (\frac{W}{L})_n (V_{GS} - V_t)$

$= 300 * \frac{0,54}{0,18} * (0,9 - 0,5) = 0,36\ mA/V$

$g_{m(p)} = \mu_p C_{ox} (\frac{W}{L})_p (V_{SG} - V_{tp}) = 75 * \frac{2,16}{0,18} (0,9 - 0,5) = 0,36\ mA/V$

$G_m = g_{m(n)} + g_{m(p)} = 0,72\ mA/V$

$V_B = \frac{V_{DD}}{2} + \Delta V(1)\, e^{(\frac{G_m}{C_B})t}$

$0,9 * 1,8 = 0,9 + 0,1 * e^{(\frac{0,72 * 10^{-3}}{1 * 10^{-12}})t}$

$\therefore t = 2,8\ ns$

A particular version of the regenerative sense amplifier of Fig. 16.20 in a 0.13-μm technology uses transistors for which $|V_t| = 0.4$ V, $k_n' = 4k_p' = 500\ \mu A/V^2$, $V_{DD} = 1.2$ V, with $(W/L)_n = 0.26\ \mu m/0.13\ \mu m$ and $(W/L)_p = 1.04\ \mu m/0.13\ \mu m$. For each inverter, find the value of G_m. For a bit-line capacitance of 0.4 pF, and a delay until an output of $0.9V_{DD}$ is reached of 1 ns, find the initial difference voltage required between the two bit lines. If the time can be relaxed by 1 ns, what input signal can be handled? With the increased delay time and with the input signal at the original level, by what percentage can the bit-line capacitance, and correspondingly the bit-line length, be increased? If the delay time required for the bit-line capacitances to charge by the constant current available from the storage cell, and thus develop the difference-voltage signal needed by the sense amplifier, was 2 ns, what does it increase to when longer lines are used?

$$g_{m(n)} = K_n'\left(\frac{W}{L}\right)(V_{GS} - V_t) = 500 * 10^{-6}\left(\frac{0.26}{0.13}\right)\left(\frac{1.2}{2} - 0.4\right) = 0.2\ mA/V$$

$$g_{m(p)} = K_p'\left(\frac{W}{L}\right)\left(\frac{V_{DD}}{2} - V_t\right) = \frac{500 * 10^{-6}}{4}\left(\frac{1.04}{0.13}\right)(0.6 - 0.4) = 0.2\ mA/V$$

$$\therefore G_m = g_{m(n)} + g_{m(p)} = 0.4\ mA/V$$

* The bit line voltage :

$$V_B = \frac{V_{DD}}{2} + \Delta V(1)\, e^{\left(\frac{G_m}{C_B}\right)t}$$

$$0.9\,V_{DD} = \frac{V_{DD}}{2} + \Delta V\, e^{\left(\frac{0.4 * 10^{-3}}{0.4 * 10^{-12}}\right)(1 * 10^{-9})}$$

$$\therefore \Delta V = 0.176\ Volt$$

* The initial Difference Voltage between two bit.

$2 * \Delta V = 2 * 0,176 = 0,352 V$

* If time relaxed by 1ns

$\therefore t = 1ns + 1ns = 2ns$

$\therefore 0,9 V_{DD} = \frac{V_{DD}}{2} + \Delta V e^{\left(\frac{Gm}{C_B}\right) * t}$

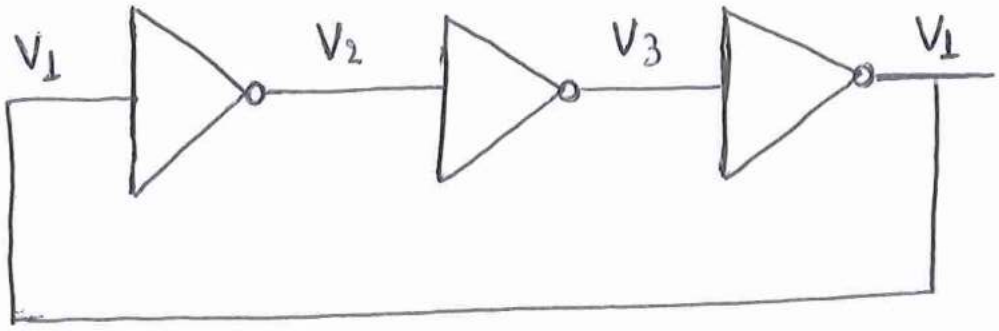
$0,9 * 1,2 = \frac{1,2}{2} + \Delta V * e^{\left(\frac{400 * 10^{-6}}{0,4 * 10^{12}}\right)(2 * 10^{-9})}$

$\therefore \Delta V = 0,065 V$

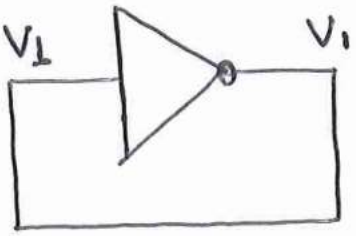
$\therefore$ The initial Diff Volt between two bit

$2 * \Delta V = 0,13 V$

Ring oscillator

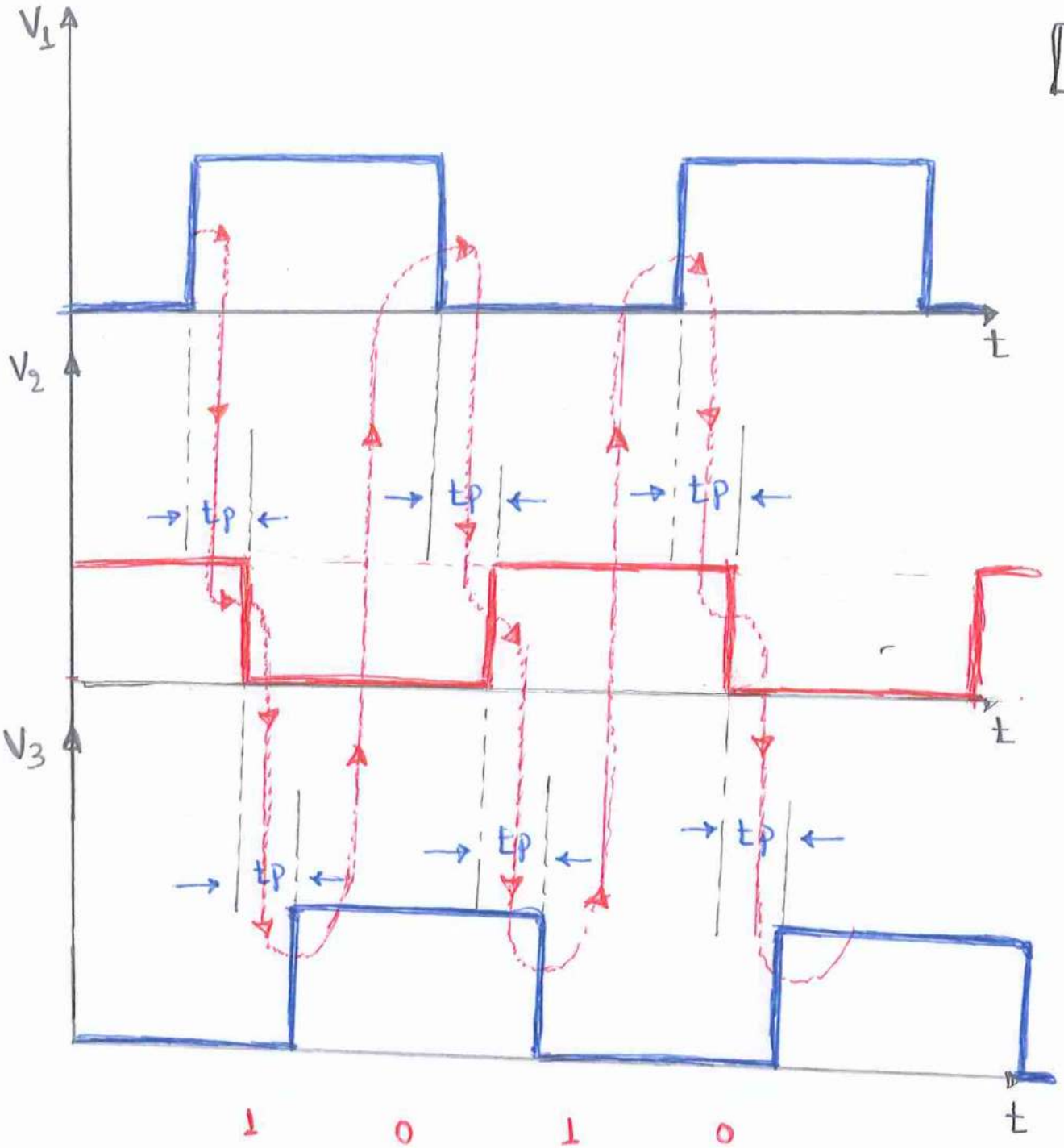


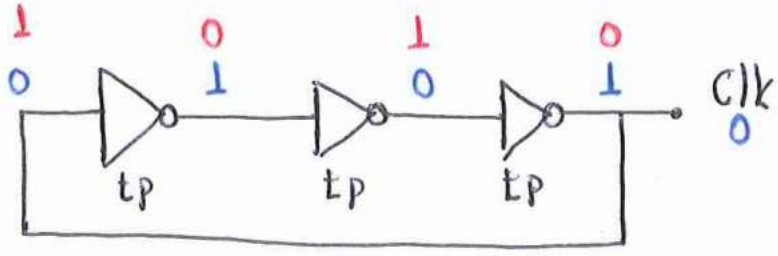
* Ring oscillator used for generate the clock pulse we always used odd number of inverters
* we can't used one inverter in Ring oscillator because the output will equal the input.

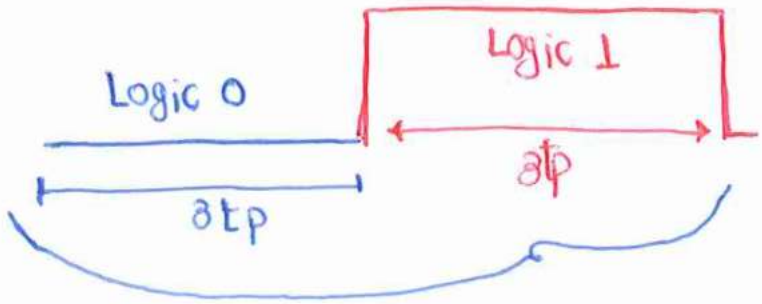


* Frequency of oscillation:

$$f = \frac{1}{2NTp}$$







$\therefore T = 6\,t_p$

$\therefore f = \frac{1}{2Nt_p}$

Example:

a ring oscillator $N = 5$ & $t_{PLH} = 6\,ns$

$t_{PHL} = 4\,ns$

(a) Sketch one of the output wave form

(b) Find the frequency of oscillation.

(c) The percentage of the cycle during output High.

(a)

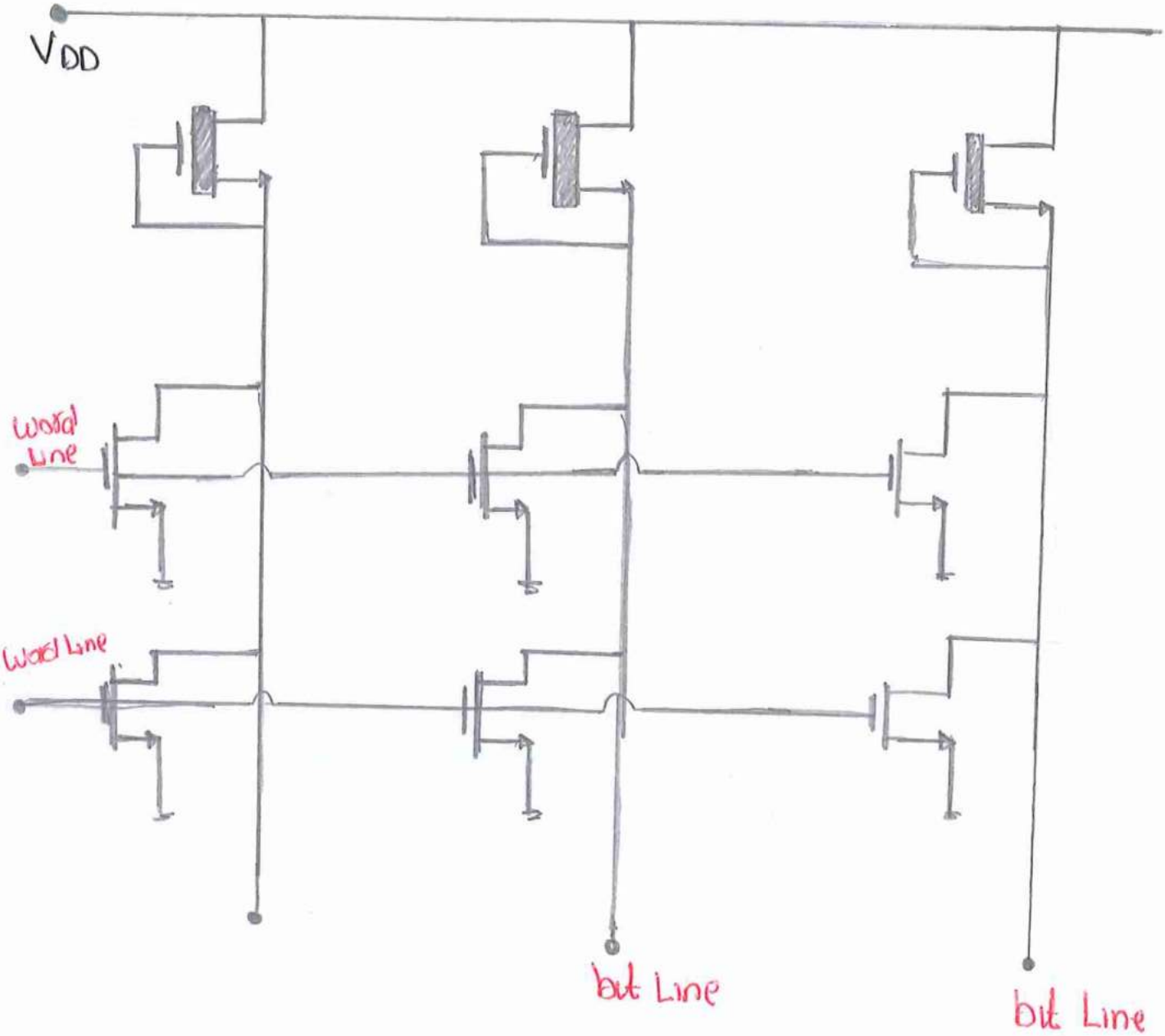
(b) $t_p = \frac{t_{PLH} + t_{PHL}}{2} = 5\,ns$

$$f = \frac{1}{2N t_p} = \frac{1}{2 * 5 * 5 * 10^{-9}} = 20\,MHz$$

(c) $\text{percentage} = \frac{t_{PHL}}{t_p} * 100 = \frac{4}{5} * 100 = 80\,\%$

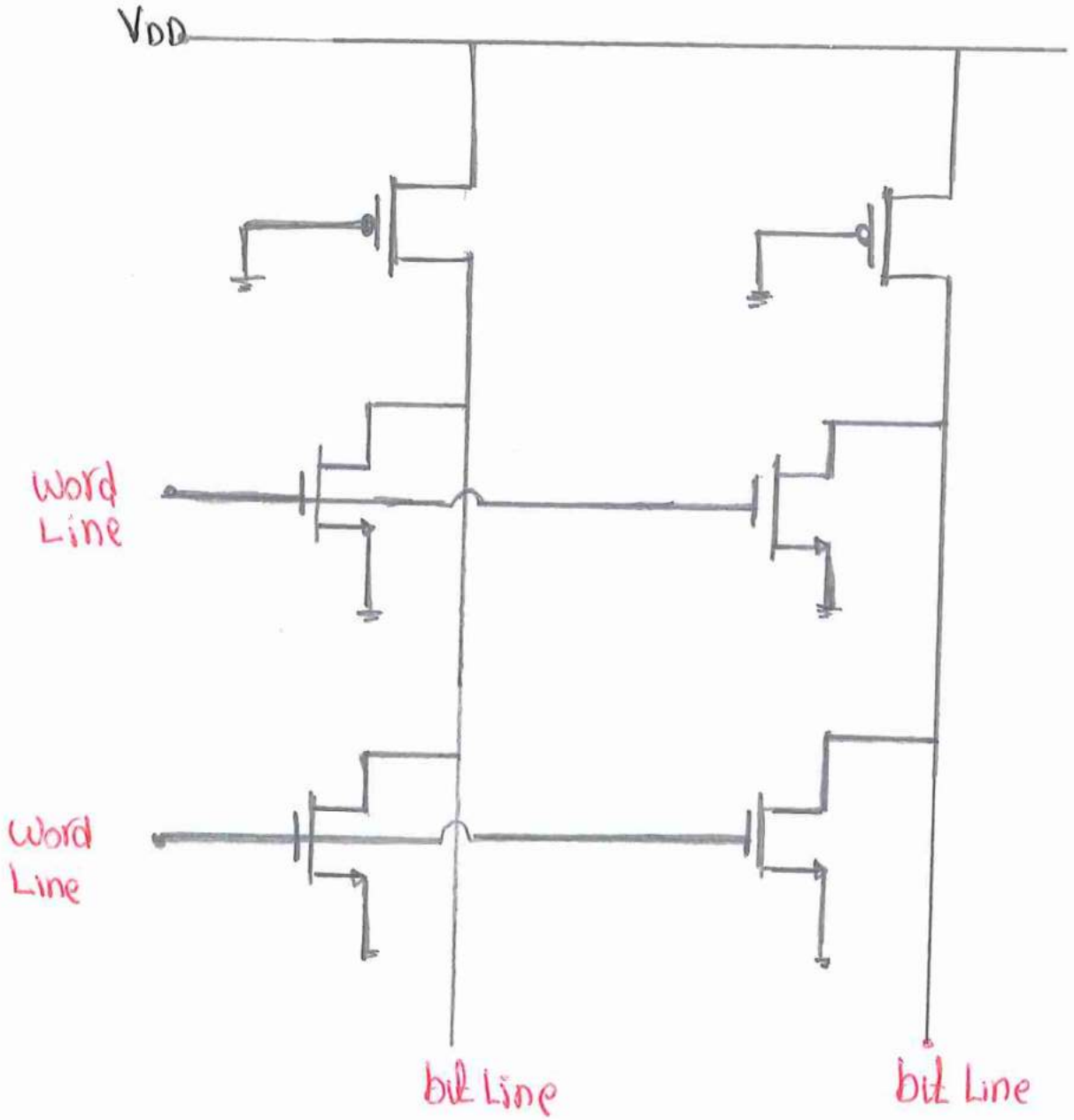
Read only memory (ROM) :

1. NMOS NOR ROM :
   - enhancement Load
   - Depletion Load.



- كل الخطوط العمودية وهي الخارجة بالقراءة (but line) .
- كل الخطوط العرضية والتي تحمل معها على المعلومات (word Line) .

2 P-seudo NOR ROM:



* هي نفس الاسم مع الـ Depletion مع تغيير فقط بـ PMOS
متصل الـ Gate فيها بالـ Ground

Example:

Design a 4 word x 4bit NMOS NOR ROM to produce output of 1011, 1111, 0110 and 1001 when rows 1, 2, 3 & 4 respectively are addressed.