Kuwait University
2020

ELECTRONICS III

Memory Circuits

Chapter 16 - Part (1)

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Memory circuit

Latches:

Latches is a temporary storage device That has two Stable States (Bi-stable), It's a basic form of memory.

* ويتم تخزين المعلومات الرقمية فى مخزن مؤقت (Temporary storage)
وهذا المخزن له وضعين استقرار (Bi-stable) إما أن يحمل القيمة 0 أو 1

Filp Flop:

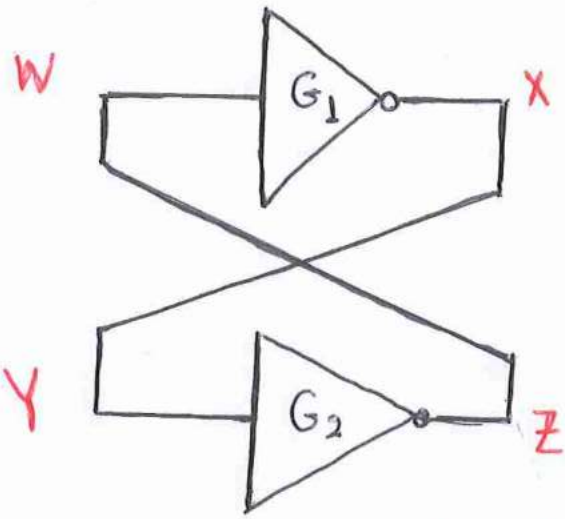
* تستخدم أيضا فى تخزين البيانات ولكن تختلف عن Latches فى طريقة التخزين.

Note That:

Both Devices are able to Store binary information (0 or 1), but Latches don't need Clock pulse to store

Latches and flip-flops:

Latch consists of Two cross coupled inverters G_1 and G_2 forming positive feedback.



which have Two Stable States (Bistable).

- If X = high(VoH) ⟶ Y = high & Z = Low

  so Z = W ⟶ Low & X = High

  High ← X وبالتالى يظل على هذا الحال

- If X = Low = Y ⟶ & Z = high

  Z = W = high ⟶ & X = Low

State can change only when Triggered

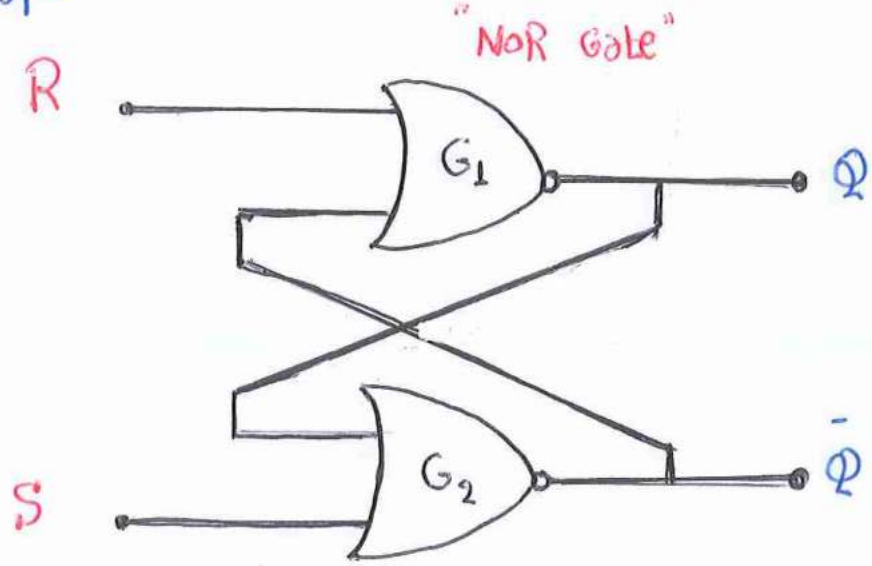
Flip flop = Latch + Triggering device

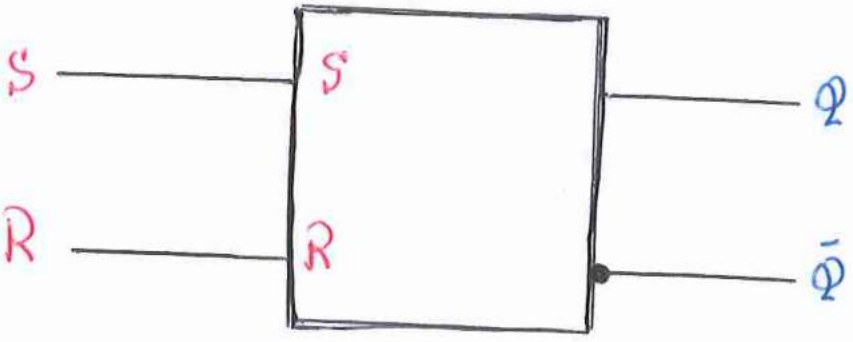
which called "Asynchronous". However. flip flop need clock pulse to store information which called "synchronous"

Type of Memory circuit:

SR flip-flop:

The simple type of flip-flop is Set/Reset (SR) flip-flop.



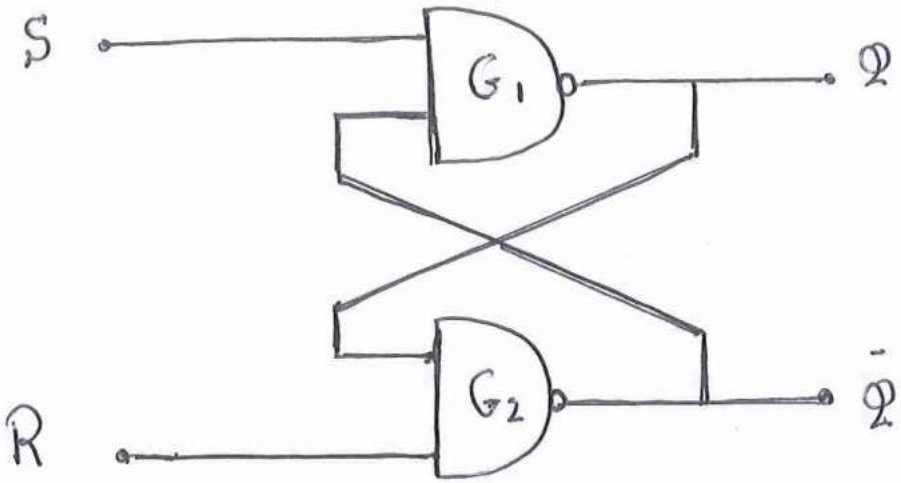


Truth Table:

inputs		outputs Q_{n+1}	outputs $\bar{Q}_{n+1}$	
S	R	Q	$\bar{Q}$	
0	0	No change		"Hold"
0	1	0	1	"Reset"
1	0	1	0	"set"
1	1	??	??	"Not used" invaild state

- If $S=0$, $R=1$ then the output Q will be forced to "0" while $\bar{Q}$ will forced to "1"
- If $S=1$, $R=0$ then the output Q will be forced to "1" while $\bar{Q}$ will forced to "0"
- If $R=S=1$ both output nodes will be forced to "0" which conflict with the complementarity of Q and $\bar{Q}$.

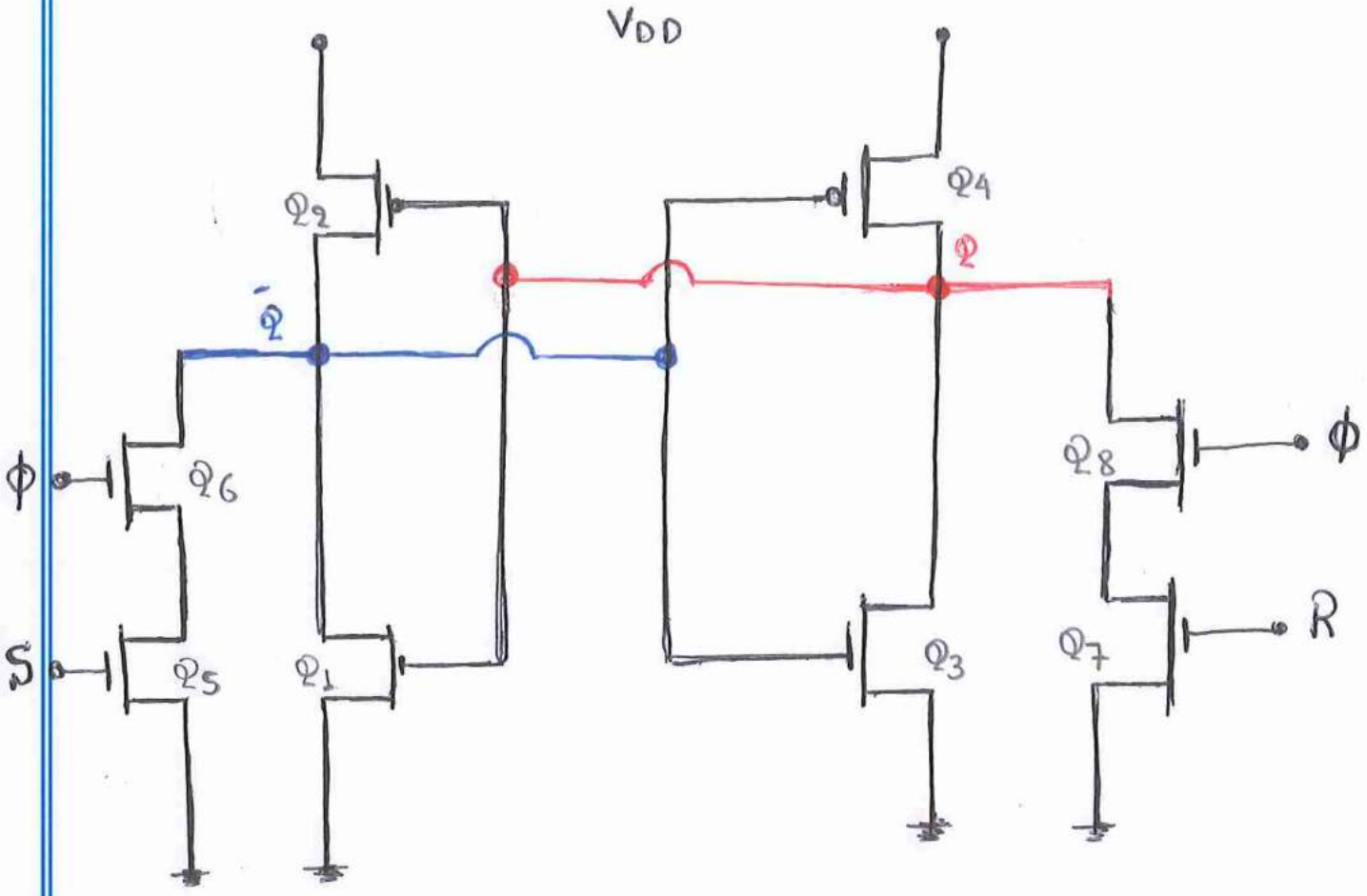
- SR flip-flop using two cross coupled NAND gates.



R	S	Q	$\bar{Q}$	
0	0	not used		
0	1	0	1	"Reset"
1	0	1	0	"set"
1	1	Hold		

- If S=1 & R=0 Then The output $\bar{Q}$ forced to "1" and The output Force $G_1 \rightarrow Q = 0$ (Reset)
- If S=0 & R=1 Then The output Q forced to "1" and The output $\bar{Q} = 0$ (set)
- If S=1 & R=1 The output will be Hold

operation of The CMOS SR flip-flop:

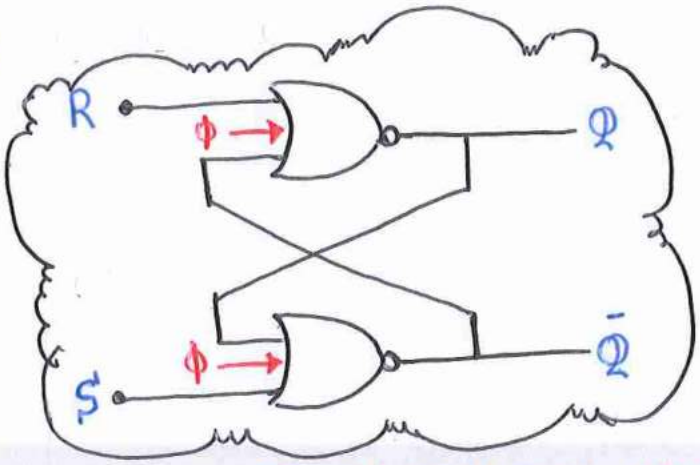


- The flip-flop is in "reset" state [$Q = 0$, $\bar{Q} = 1$] and we need to put it in "set" state.

S = High = V_{DD} & R = Low = 0

and ϕ = high = V_{DD}

- So, Q_5 & Q_6 ⟶ ON



* The Voltage $\bar{Q}$ will go down = 0 and this make the inverter $[Q_3 \& Q_4] \longrightarrow Q = V_{DD}$ = High

* The output Q will fed the input for inverter of $[Q_1 \& Q_2]$ and this causing output $\bar{Q}$ go down=0

* Q_5 & Q_6 used to pull the node $\bar{Q}$ down to Voltage below the Threshold of (Q_3 & Q_4) inverter and this is essential for the regenerative process to begin.

So we should know the minimum (W/L) ratio that Q_5 & Q_6 must have to meet this requirement.

* An estimate of the minimum width required for the set pulse can be obtained from $V_{\bar{Q}}$ reduced from V_{DD} to $V_{DD}/2$, and V_Q rise from zero to $V_{DD}/2$

The CMOS SR flip-flop in Fig. 16.4 is fabricated in a 0.18-μm process for which $\mu_n C_{ox} = 4\mu_p C_{ox} = 300\ \mu A/V^2$, $V_{tn} = |V_{tp}| = 0.5$ V, and $V_{DD} = 1.8$ V. The inverters have $(W/L)_n = 0.27\ \mu m/0.18\ \mu m$ and $(W/L)_p = 4(W/L)_n$. The four NMOS transistors in the set–reset circuit have equal W/L ratios.

(a) Determine the minimum value required for this ratio to ensure that the flip-flop will switch.

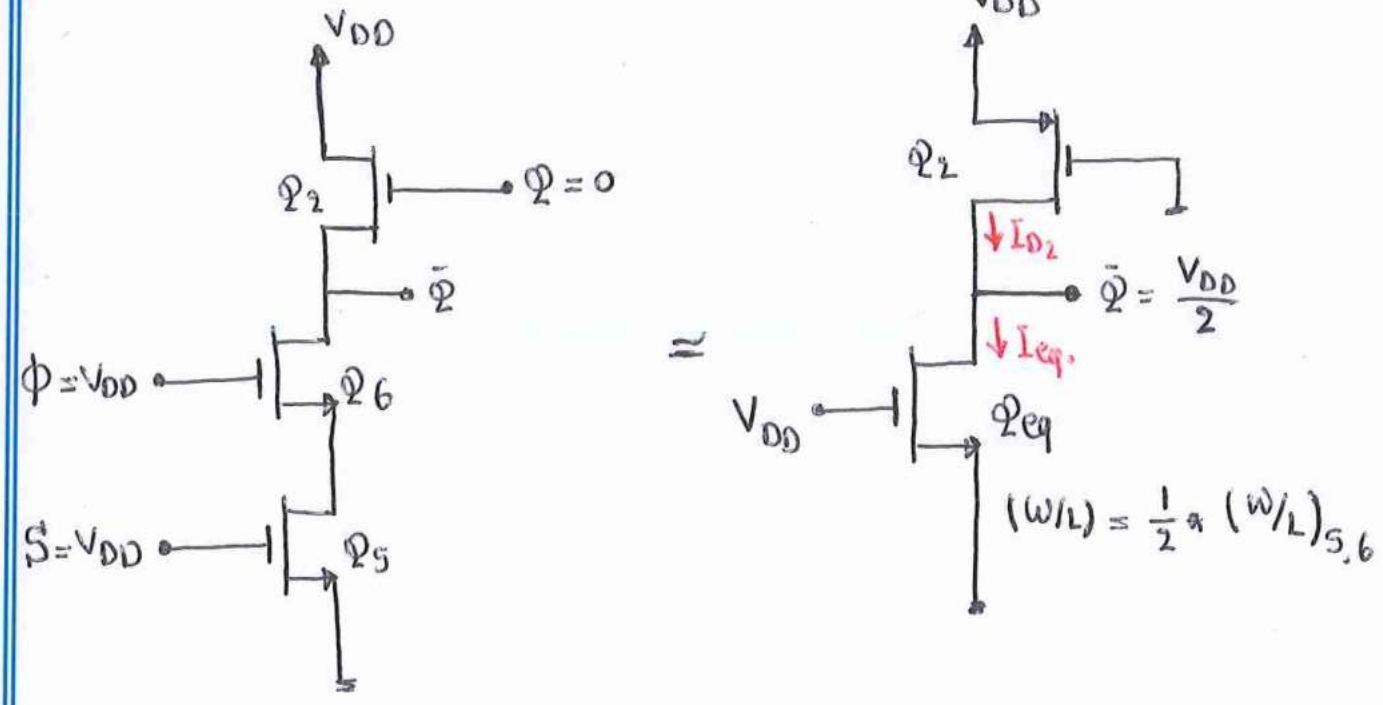
(b) Also, determine the minimum width the set pulse must have for the case in which the W/L ratio of each of the four transistors in the set–reset circuit is selected at twice the minimum value found in (a). Assume that the total capacitance between each of the Q and $\overline{Q}$ nodes and ground is 20 fF.

* The flip-flop will switch from $Q = 0$ & $V_{\bar{Q}} = V_{DD}$ (reset) to $[Q = 1$ & $\bar{Q} = 0]$ (set)

So Q_5 and Q_6 will be ON

$Q_1 \longrightarrow$ off

$Q_2 \longrightarrow$ ON



our task to find $(\frac{W}{L})$ for Q_5 and Q_6

and $\bar{Q} = V_{OL}$ is Lower Than $\frac{V_{DD}}{2}$ [Threshold of Q_3, Q_4]

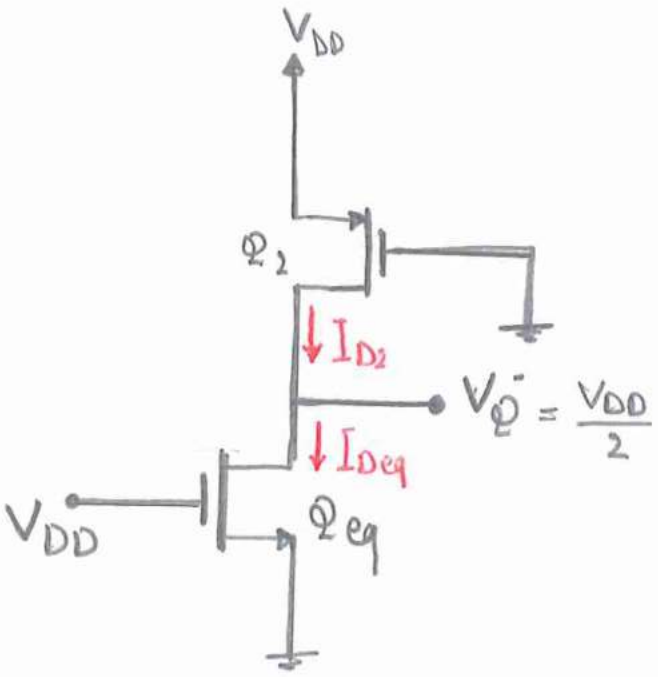
$$(W/L) = \frac{1}{2}(W/L)_5 = \frac{1}{2}\left(\frac{W}{L}\right)_6$$

$$I_{Deq} = I_{D2}$$

* $V_Q = 0$ to be set (1)

* $S = V_{DD}$ until $V_Q' = \frac{V_{DD}}{2}$

↳ Threshold of Transistor



(For Q_2):

$$V_{SD} = V_S - V_D = V_{DD} - \frac{V_{DD}}{2} = \frac{V_{DD}}{2} = \frac{1,8}{2} = 0,9$$

$$V_{SG} = V_S - V_G = V_{DD} - 0 = V_{DD}$$

$$\therefore V_{SD(sat)} = V_{SG} - |V_{tp}| = V_{DD} - 0,5 = 1,3 \text{ Volt}$$

$$\therefore V_{SD} < V_{SD_{sat}} \longrightarrow \text{Triode}$$

$$\therefore I_{D_2} = K_p'\left(\frac{W}{L}\right)\left[(V_{SG} - |V_t|)V_{SD} - \frac{V_{SD}^2}{2}\right]$$

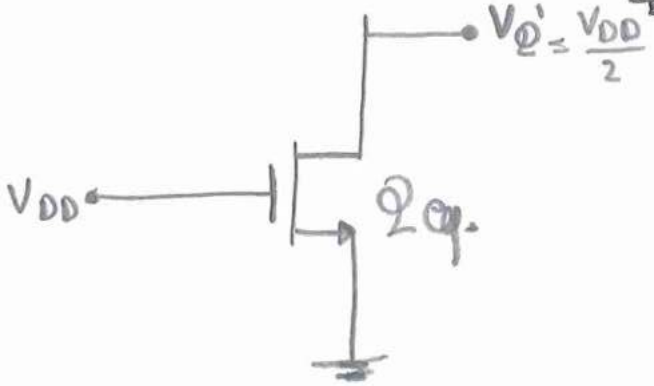
(For Q_5 & Q_6):

$$(W/L)_{eq} = \frac{1}{2}\left(\frac{W}{L}\right)_n$$

$V_G = V_{DD}$

$V_S = 0$

$V_D = \frac{V_{DD}}{2}$



$\therefore V_{GS} = V_G - V_S = 1,8\ V$

$V_{DS} = V_D - V_S = \frac{V_{DD}}{2} - 0 = 0,9\ Volt$

$V_{DS(sat)} = V_{GS} - V_t = 1,8 - 0,5 = 1,3\ Volt$

$\therefore V_{DS} < V_{DS\,sat}$ $\therefore$ Triode

$\therefore I_{Deq} = K_n'\left(\frac{W}{L}\right)_{eq}\left[(V_{GS}-V_t)V_{DS} - \frac{V_{DS}^2}{2}\right]$

$$I_{Deq} = I_{D_2}$$

$$K_n'\left(\frac{W}{L}\right)_{eq}\left[(V_{GS}-V_t)V_{DS} - \frac{V_{DS}^2}{2}\right] = K_p'\left(\frac{W}{L}\right)_p\left[(V_{SG}-|V_t|)V_{SD} - \frac{V_{SD}^2}{2}\right]$$

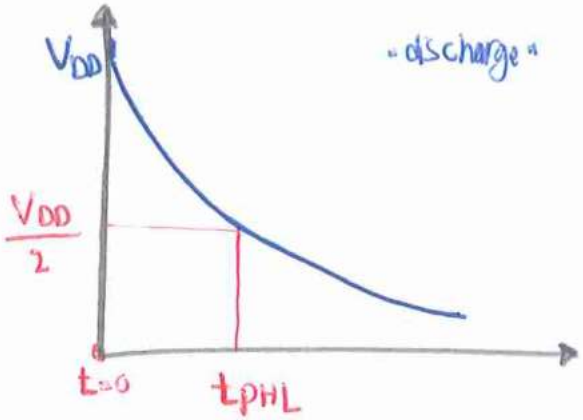
$\therefore 300 * \frac{1}{2}\left(\frac{W}{L}\right)_5\left[(1,8-0,5)\left(\frac{1,8}{2}\right) - 0,5\left(\frac{1,8}{2}\right)^2\right] = 75\left(\frac{1,08}{0,18}\right)\left[(1,8-0,5)\left(\frac{1,8}{2}\right) - 0,5\left(\frac{1,8}{2}\right)^2\right]$

$\therefore \left(\frac{W}{L}\right)_5 = 3$ "The minimum value"

$\therefore W = 3 * L = 3 * 0,18 = 0,54\ \mu m$

$\therefore \left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_6 = \frac{0,54}{0,18}$

(b) Determine the minimum width the set pulse must have for the case in which the W/L ration at twice the min. Value and C = 20 ff.

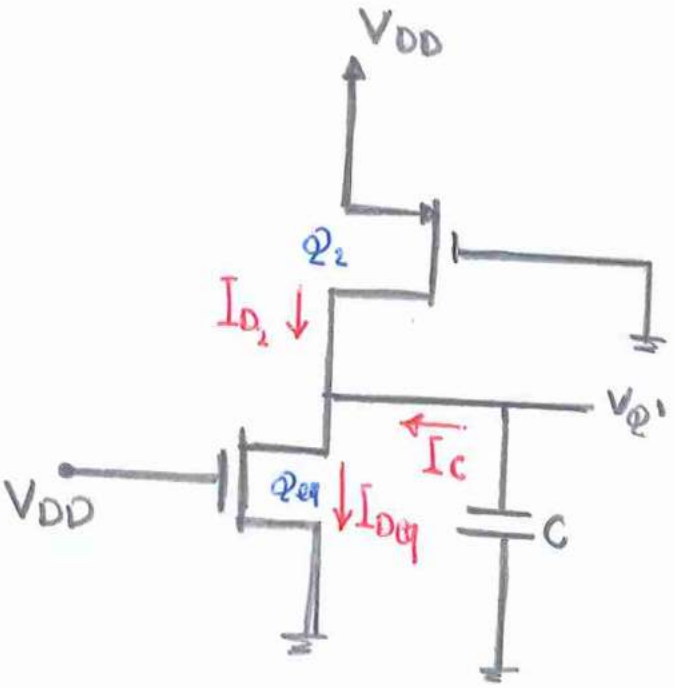


* $T_{min} = t_{PHL} + t_{PLH}$
* $\left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_6 = \frac{1,08}{0,18}$

$$I_C + I_{D_2} = I_{Deq}$$

$$I_C = I_{Deq} - I_{D_2}$$

at $t=0$ ⇒ $V_{Q'} = V_{DD}$



For Q_2:

$V_S = V_{DD}$

$V_D = V_{Q'} = V_{DD}$

$V_{SD} = V_S - V_D = 0$

$V_{SD_{sat}} = V_{SG} - |V_{tp}|$

$\therefore V_{SD} < V_{SD_{sat}}$ Q_2 Triode.

$$I_D = K_p'\left(\frac{W}{L}\right)\left[(V_{SG} - V_{tp})V_{SD} - \frac{V_{SD}^2}{2}\right]$$

But $V_{SD} = 0$

$\therefore I_{D_2} = 0$ $\therefore Q_2 = 0$

For Q_{eq} :

$V_D = V_{DD}$

$V_S = 0$

$V_G = V_{DD}$

$\therefore V_{GS} = V_G - V_S = V_{DD}$

$V_{DS} = V_D - V_S = V_{DD}$

$\therefore V_{DS_{sat}} = V_{GS} - V_t = V_{DD} - V_t$

$\therefore V_{DS} > V_{DS(sat)}$ $\therefore$ Saturation.

$\therefore I_{D_{eq}} = \frac{1}{2} K_n' \left(\frac{W}{L}\right)_n (V_{GS} - V_t)^2$

$I_{D_{eq}} = \frac{1}{2} * 300 * \frac{1}{2} \left(\frac{W}{L}\right)_{min} (1,8 - 0,5)^2$

$\left(\frac{W}{L}\right)_{min} \rightarrow \left(\frac{1,08}{0,18}\right)$

$\therefore I_{D_{eq}} = 760,5\ \mu A$

$\therefore I_{C(0)} = 760,5\ \mu A$

$t = t_{PHL}$ & $V_2' = \frac{V_{DD}}{2}$

Q_2 , Q_{eq} are Triode

For Q_2:

$$\therefore I_{D_2} = K_p' \left(\frac{W}{L}\right) \left[(\underbrace{V_{SG}}_{V_{DD}} - |V_{tp}|) V_{SD} - \frac{V_{SD}^2}{2} \right]$$

$$\therefore I_{D_2} = 344{,}25$$

For Q_{eq}: $\rightarrow \frac{1}{2}\left(\frac{1{,}08}{0{,}18}\right)$

$$I_{Deq} = K_n' \left(\frac{W}{L}\right)_{eq} \left[(\underbrace{V_{GS}}_{V_{DD}} - V_t) \underbrace{V_{DS}}_{\frac{V_{DD}}{2}} - \frac{V_{DS}^2}{2} \right]$$

$$\therefore I_{Deq} = 688{,}5$$

$$\therefore I_C(t_{PHL}) = 688{,}5 - 344{,}25 = 344{,}25\,MA$$

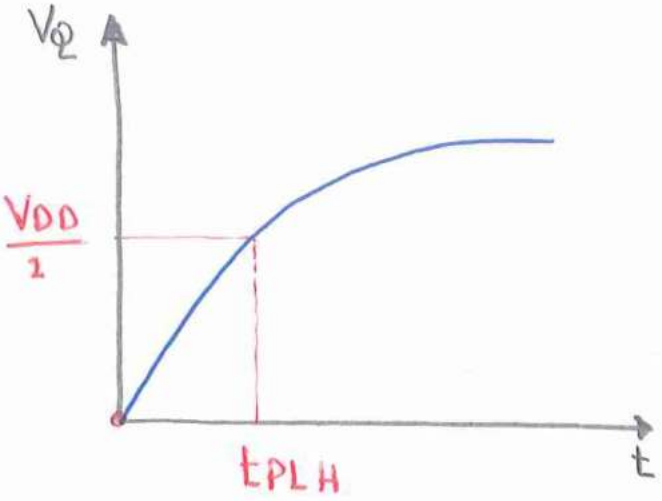
$$I_{C\,ave} = \frac{I_C(0) + I_C(t_{PHL})}{2} = 552{,}4\,MA$$

$$t_{PHL} = \frac{C * \left(\frac{V_{DD}}{2}\right)}{I_{ave.}} = 32{,}6\,PS$$

- For t_{PLH} : (For output Q_3 , Q_4)

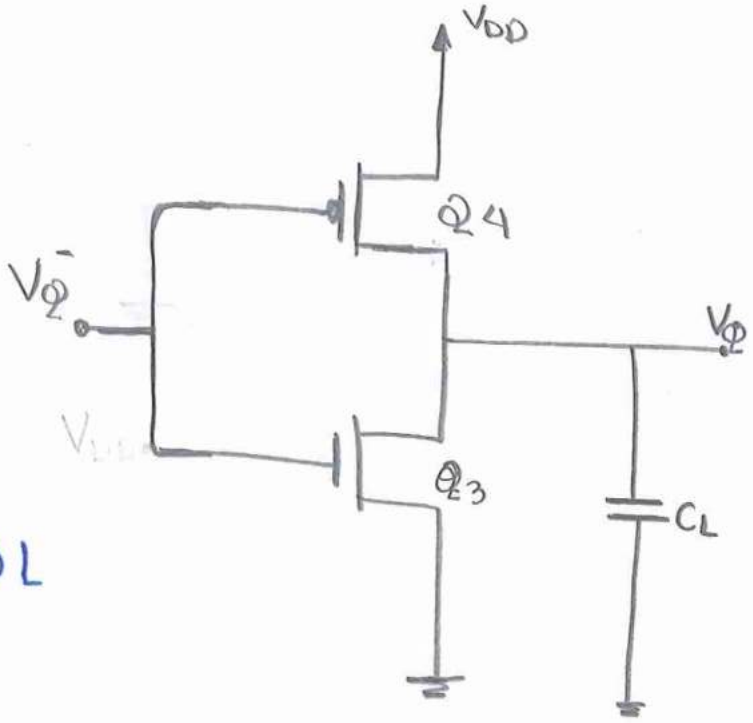
$V_Q = 0 \quad , \quad t = 0$

$V_Q = \frac{V_{DD}}{2} \quad , \quad t = t_{PLH}$



$$t_{PLH} = \frac{\alpha_p C}{K_p' \left(\frac{W}{L}\right)_p * V_{DD}}$$

$$\alpha_p = \frac{2}{\left[\frac{1}{4} - \frac{3|V_{tp}|}{V_{DD}} + \left(\frac{|V_{tp}|}{V_{DD}}\right)^2\right]}$$



$$\therefore \alpha_p = \frac{2}{1{,}75 - \frac{3 * 0{,}5}{1{,}8} + \left(\frac{0{,}5}{1{,}8}\right)^2} = 2{,}01$$

$$\therefore t_{PLH} = \frac{2{,}01 * 20 * 10^{-15}}{75 * 10^{-6} * \left(\frac{1{,}08}{0{,}18}\right) * 1{,}8} = 49{,}7\ PS$$

$$\therefore T_{min} = t_{PLH} + t_{PHL}$$

Example

For the SR flip-flop find the minimum $(\frac{W}{L})$ for both Q_5 & Q_6 so that switching is achieved when input S and ϕ are at $(\frac{V_{DD}}{2})$.

when $S \& \phi = \frac{V_{DD}}{2}$

$\therefore Q_{eq}$ $V_{GS} = \frac{V_{DD}}{2}$, $V_{DS} = \frac{V_{DD}}{2}$

$\therefore Q_{eq}$ in Saturation.

for Q_2:

$$V_{SD} = V_{DD} - V_{\bar{Q}} = \frac{V_{DD}}{2}$$

$$V_{SG} = V_{DD}$$

$\therefore Q_2$ in Triode

$$\left(\frac{W}{L}\right)_{eq} = \frac{1}{2}\left(\frac{W}{L}\right)_{5,6}$$

$$I_{D_{eq}} = I_{D_2}$$

$$\frac{1}{2}K_n'\left(\frac{W}{L}\right)_{eq}\left(\frac{V_{DD}}{2} - V_t\right)^2 = K_p'\left(\frac{W}{L}\right)_2\left[(V_{DD} - V_t)\frac{V_{DD}}{2} - \frac{1}{2}\left(\frac{V_{DD}}{2}\right)^2\right]$$

$\therefore \left(\frac{W}{L}\right)_5 = 14,34$

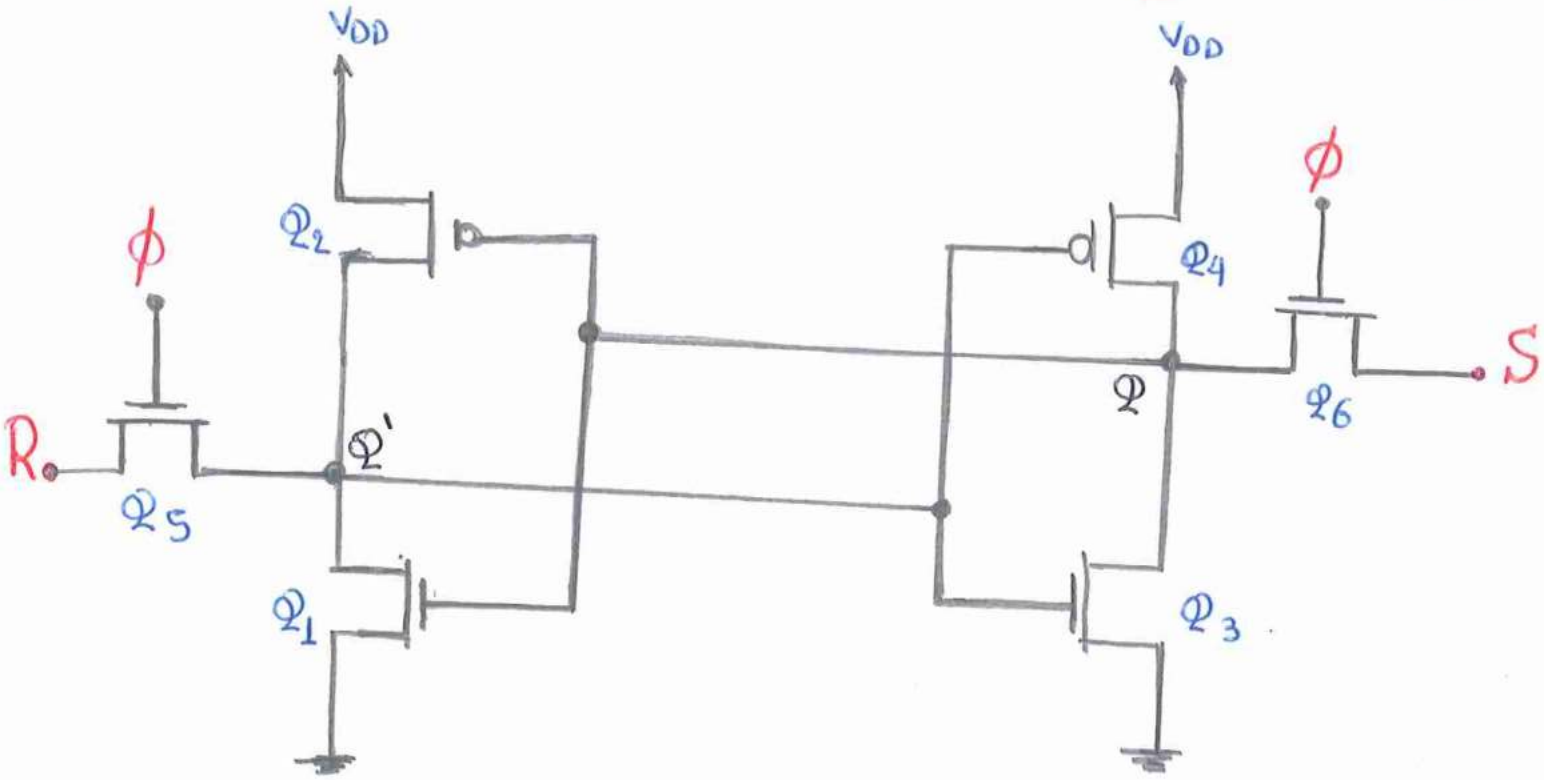
$\therefore W = L * 14,34$

$= 0,18 * 14,34$

$W = 2,58 \mu m$

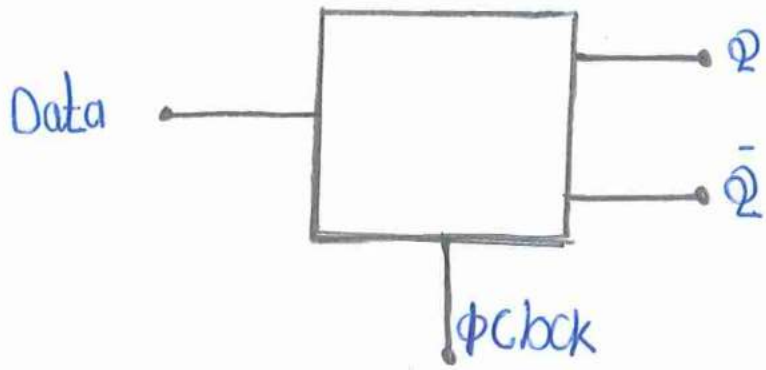
$\therefore \left(\frac{W}{L}\right)_5 = \frac{2,58\ \mu m}{0,18\ \mu m}$

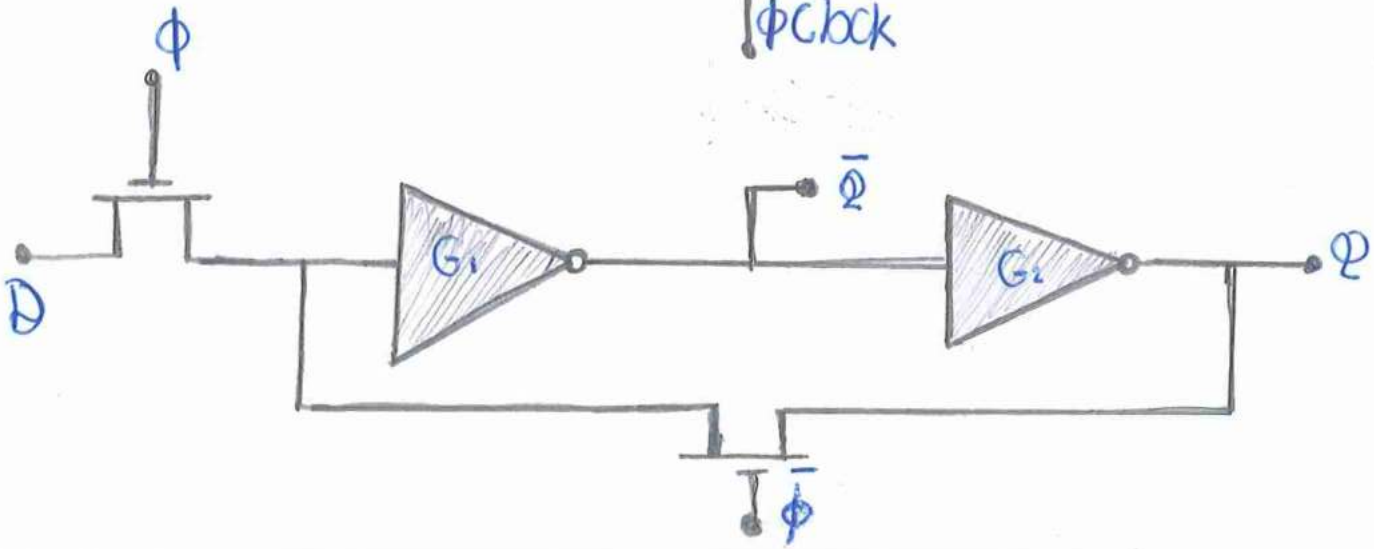
Clocked SR Flip-Flop : (Pass-Transistor) [6T CMOS SR-Flip flop]



2 D Flip-Flop circuit :

"Block Diagram"





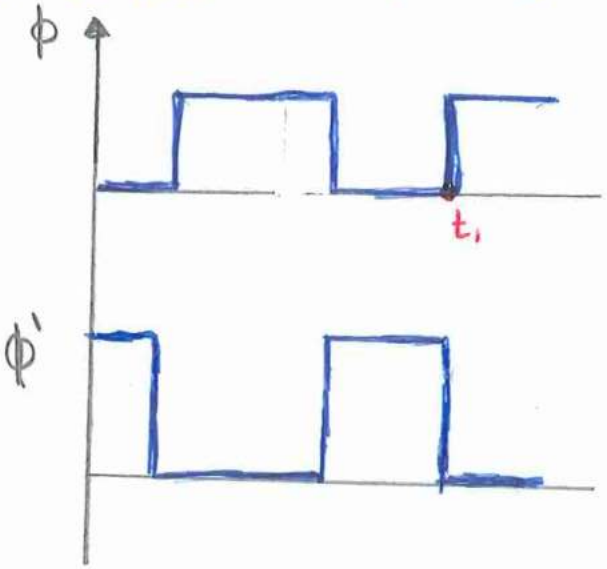
- The D Flip-Flops is consisted of two cascaded inverters with positive Feedback Loops.

* at t less than Zero (before working):
  * ϕ Low . so D isolated From Circuit

* at t more than Zero (During working):
  * ϕ high ⟶ (Feedback Loop will be open)
  * The output for G_1 is $\bar{D}$

and The output For G_2 is D

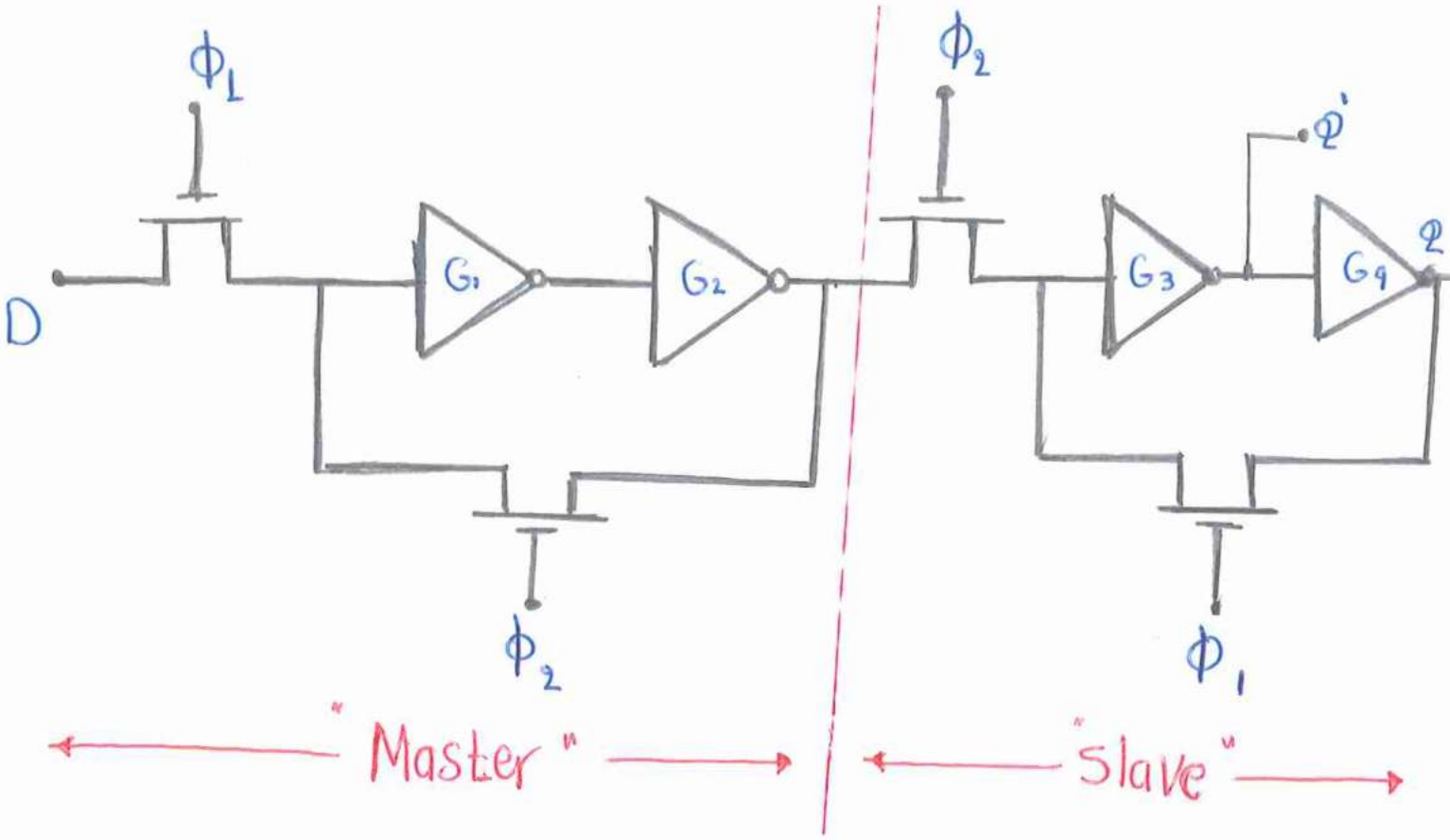
* at $t = t_1$
  * ϕ Low ⟶ (Feedback closed)
  * input isolated $Q = D$



Note:

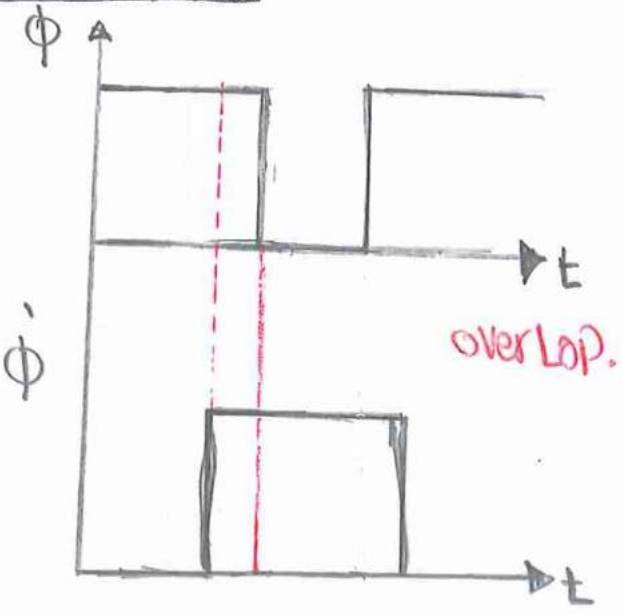
- no over Lap between ϕ, ϕ'
- we can change Input but we can't change output.

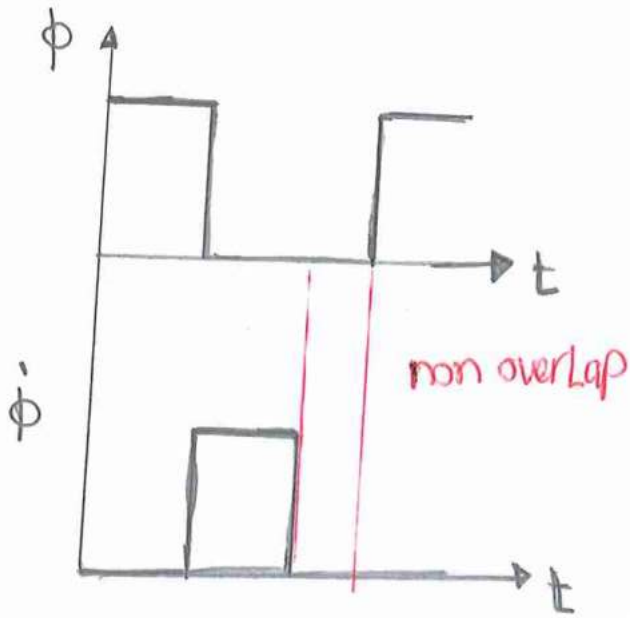
D Flip-Flop (Master-Slave):



- two cascaded D Flip-flop to avoide overLap between ϕ and ϕ' so we used ϕ_1 and ϕ_2

Note That:





⇨ Master - Slave Flip - Flop no overLap.

operation For Master-slave Flip flop:

a Case 1 :

* ϕ_1 high , ϕ_2 Low

input Data D transfered to output of Master to Slave

b Case 2 :

* ϕ_1 Low and ϕ_2 high

Master Isolated From input Line

c Case 3 :

* ϕ_1 = High , ϕ_2 = Low (It's happen during non overlap)

No change in output

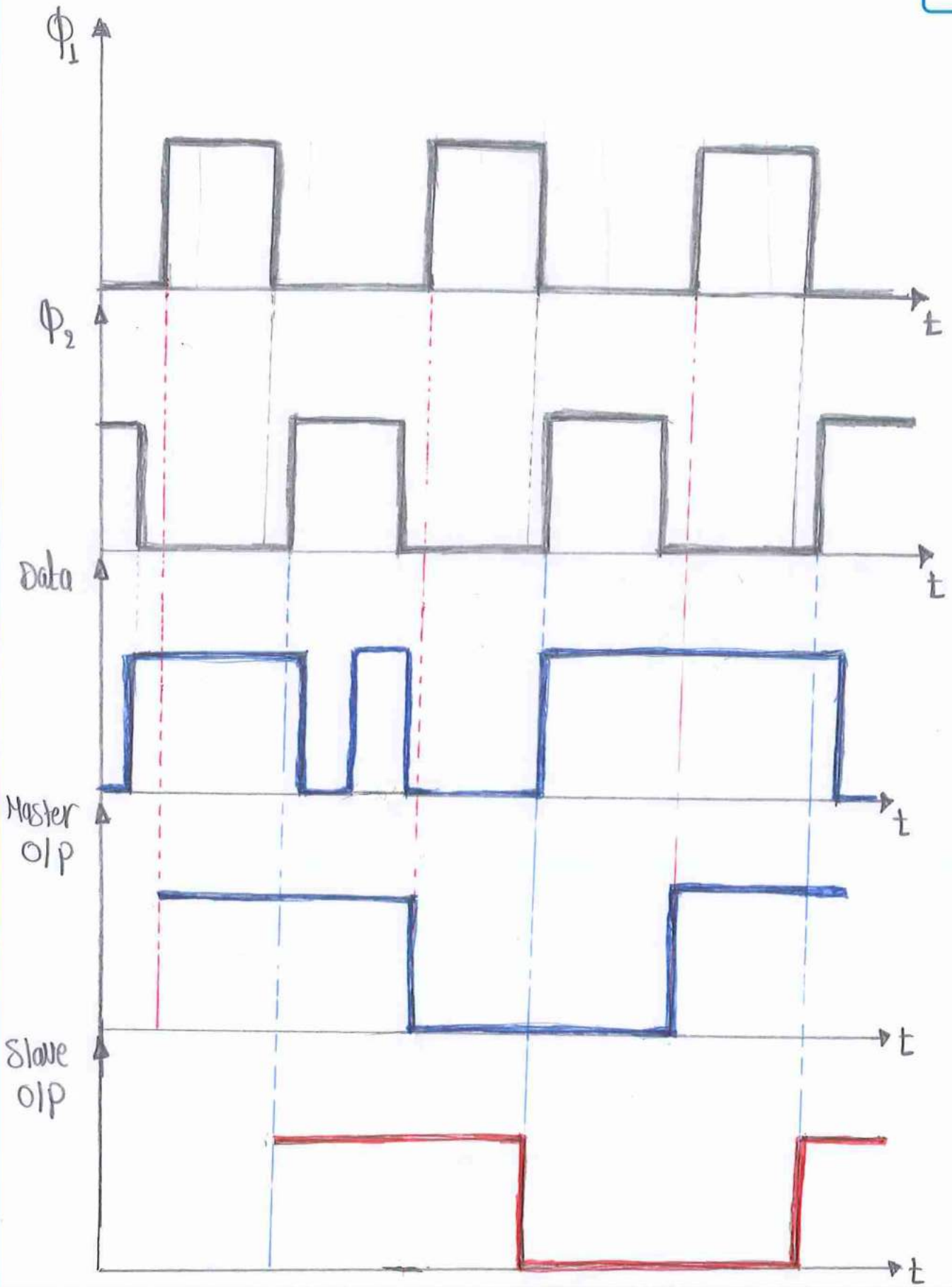
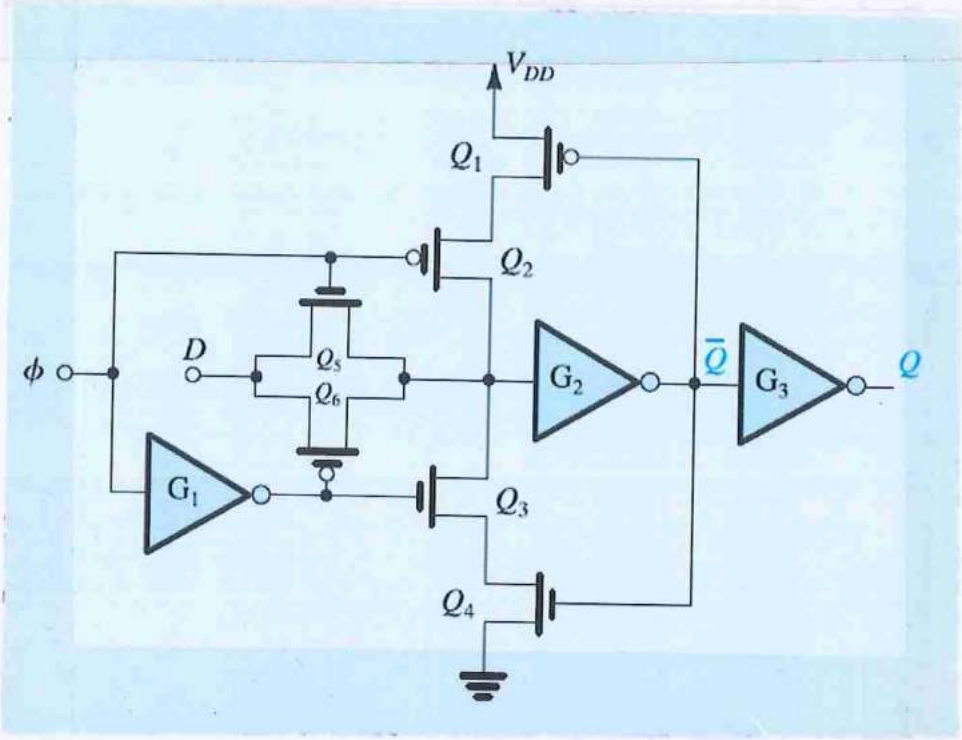

ϕ_1
t
ϕ_2
t
Data
t
Master o/p
t
Slave o/p
t

Figure below shows a commonly used circuit of a D flip-flop that is triggered by the negative-going edge of the clock φ.

a. For φ high, what are the values of $\bar{Q}$ and Q in terms of D? Which transistors are conducting?
b. If D is high and φ goes low, which transistors conduct and what signals appear at $\bar{Q}$ and at Q? Describe the circuit operation.
c. Repeat (b) for D low with the clock φ going low.
d. Does the operation of this circuit rely on charge storage?



(a) ϕ = High

* Q_5 & Q_6 will be ON [High signal applied to gate]
* Q_2 will be off
* D The input for G_2, so $\bar{Q} = \bar{D}$ and $Q = D$
* If : D = High Q_1 ON & Q_4 off

D = Low Q_1 off & Q_4 ON

(b) ϕ = Low

D = High

* Q_2 & Q_3 ON

* Q_5 & Q_6 off , So G_2 is High

∴ $\bar{Q}$ = Low and Q = High

* Q_1 ON & Q_4 off

(c) ϕ = Low

D = Low

* Q_5 & Q_6 off

* Q_2 & Q_3 ON

* If D is Low G_2 is Low , $\bar{Q}$ is High and Q is Low

* Q_1 off & Q_4 ON