Kuwait University
2020

ELECTRONICS III

PSEUDO-NMOS Logic Circuits

Chapter 15 - Part (2)

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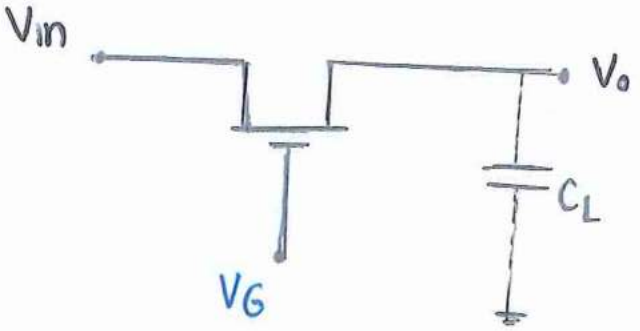
Pass - Transistor Logic circuit:

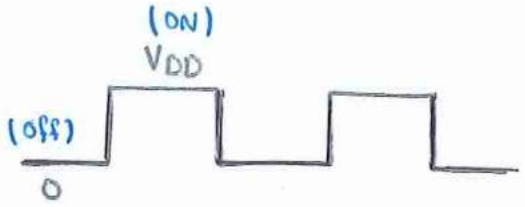
(NMOS)

$V_{tn} > 0$ (+ve)



$V_{GS} = V_G - V_S$

(Clock)



* For NMOS V_{GS} should be more than V_t to be ON
* So to work $V_G = V_{DD}$ From clock

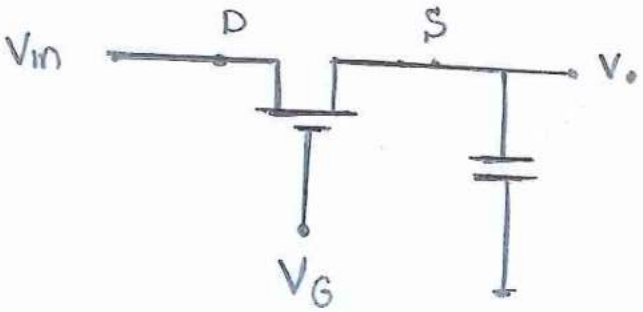
∴ $V_G = 0$ (NMOS off)

$V_G = V_{DD}$ (NMOS ON)

* In NMOS The Drain Take The max. Volt
* C_L ⟶ gate capacitance

If V_{in} = high:

$V_{GS} > V_t$



* C_L will charge

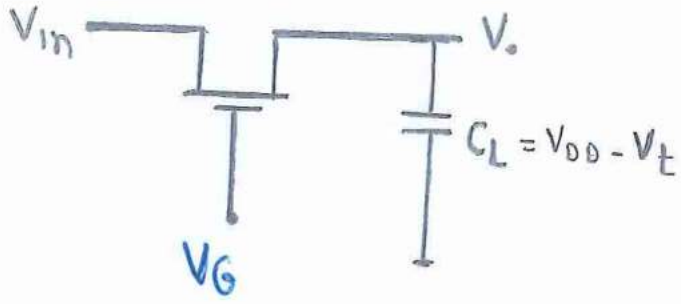
So The capacitor will charge till $V_{DD}-V_t$ at This time

* $V_{GS} = V_G - V_S = V_{DD} - V_{DD} + V_t = V_t$

For V_{in} = LOW

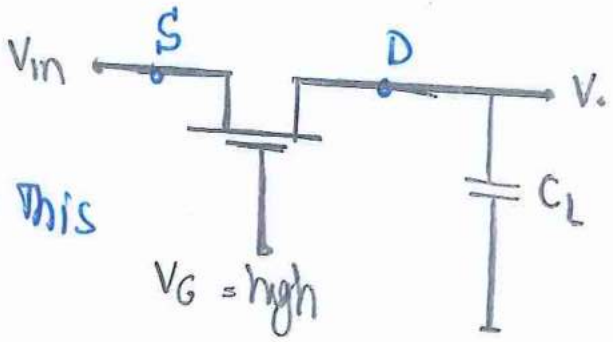
* If V_G = Low

The switch will be off



* If V_G = high

The capacitor will discharge in this case



وفي capacitor الـ V_{GS} بتساوي بقيم

$V_{GS} = V_G - V_S = V_{DD} - 0 = V_{DD}$

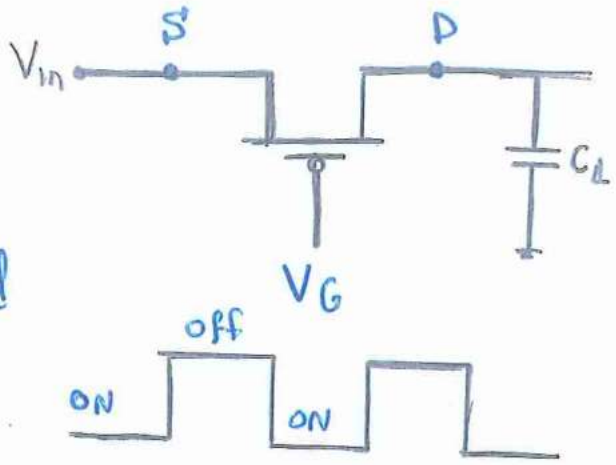
So The capacitor will Discharge till to zero.

In NMOS:

The charge go to ($V_{DD}-V_t$) "weak 1" "V_{OH}"

The Discharge go to (zero) "strong 0" "V_{OL}"

* For PMos :



$V_{SG} = V_S - V_G$

So to work the Clock should be Low (zero)

$V_{tp} < 0$ (-ve) * in PMos the Source take the max. Volt.

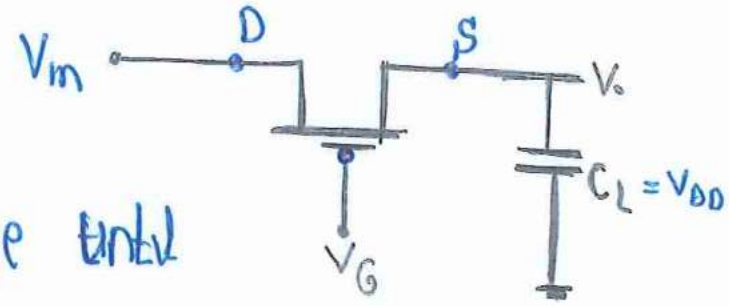
For V_{In} = high

In P Mos the source take the higher Voltage

So $V_{SG} = V_{DD} - 0 = V_{DD}$ (ON)

The capacitor will change to V_{DD}

V_{In} = Low



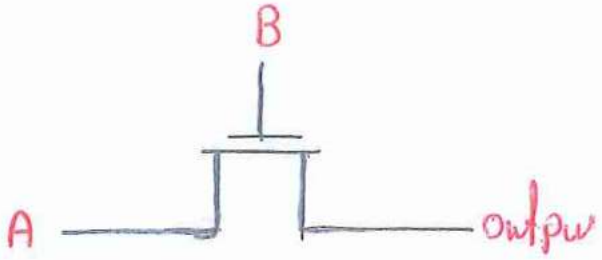
The capacitor will Discharge until reaching $-V_{tp}$

Strong 1 & weak zero

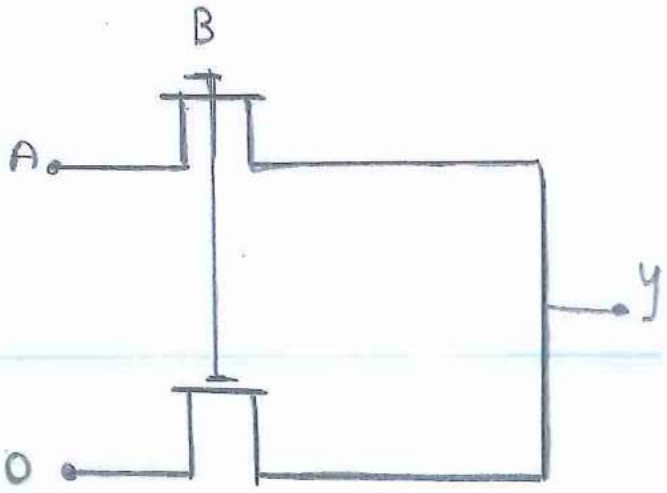
Pass-Transistor Logic circuits

1 N-Mos Pass-Trans. Logic:

output = A B



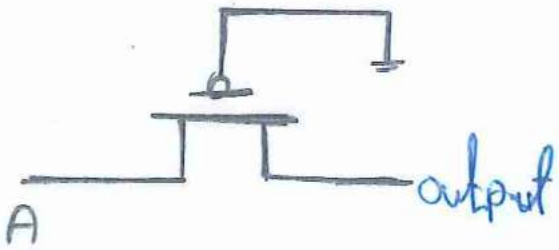
A	B	output
0	0	0
0	1	0
1	0	0
1	1	1



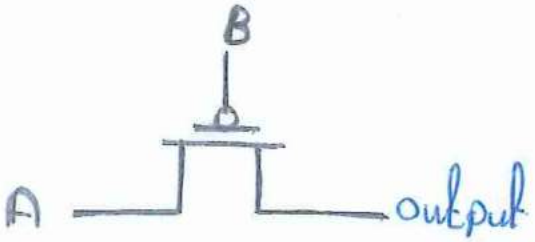
$Y = A*B + 0*B = AB$

2 P-Mos Pass-Trans. Logic:

output = $A * (\bar{0}) = A$

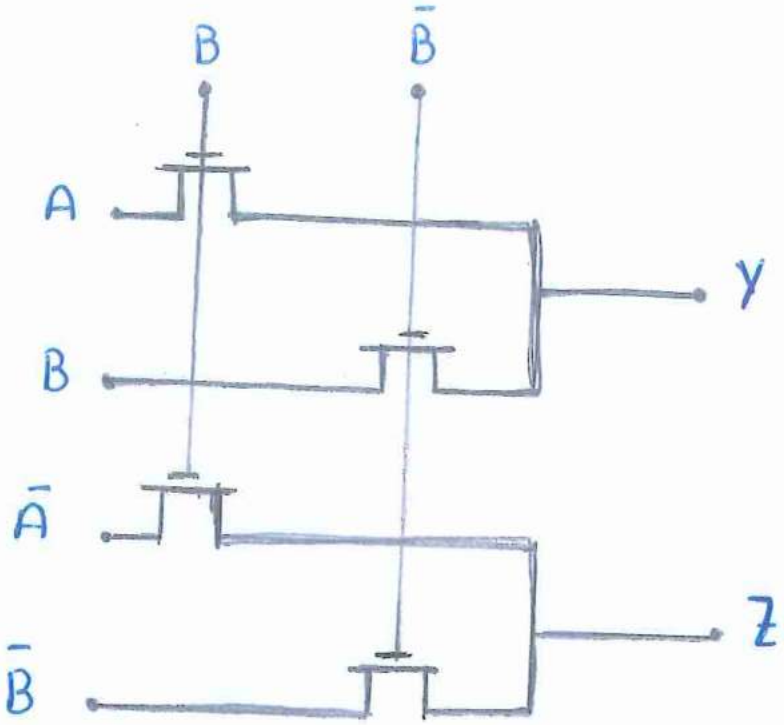


output = $A * \bar{B}$



Example:

a



$$y = A * B + B * \bar{B}$$

$$\therefore y = AB$$

$$Z = \bar{A}B + \bar{B}\bar{B}$$

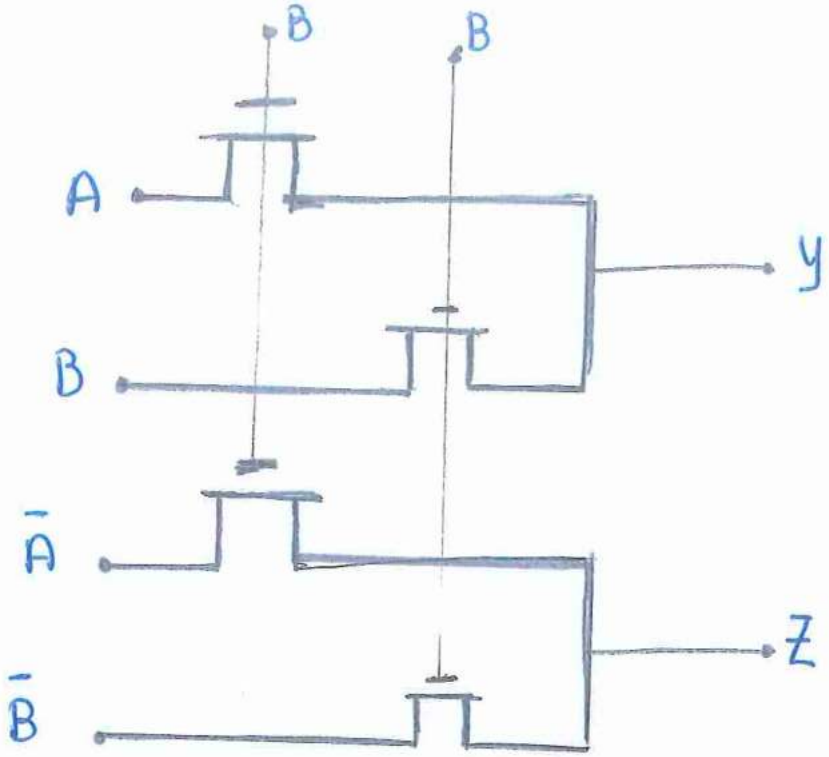
$$\therefore Z = \bar{A}B + \bar{B}$$

$$Z = \overline{(A + \bar{B})B}$$

$$Z = \overline{AB + B\bar{B}}$$

$$Z = \overline{AB}$$

B



$y = A\bar{B} + BB$

$y = A\bar{B} + B$

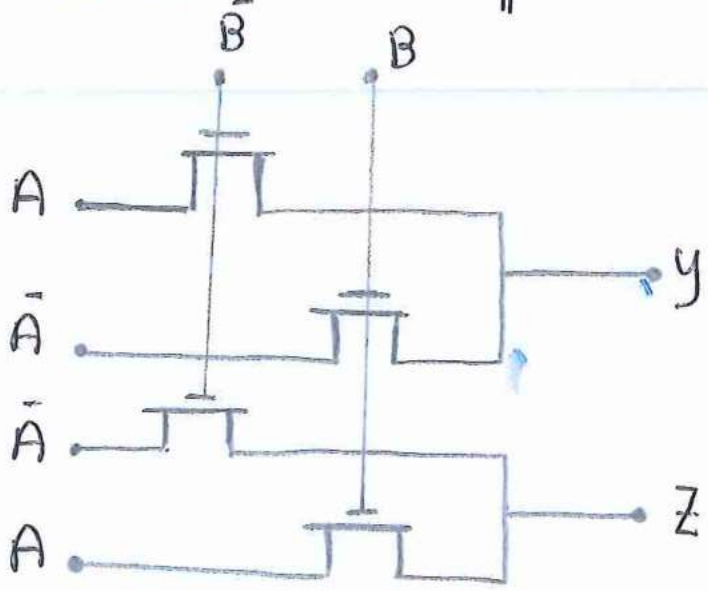
$\therefore y = (\bar{A}+B)\bar{B} = \bar{A}\bar{B} + B\bar{B}$

$\therefore y = A + B$ (OR)

$Z = \bar{A}\bar{B} + \bar{B}B$

$Z = \overline{A+B}$ (NOR)

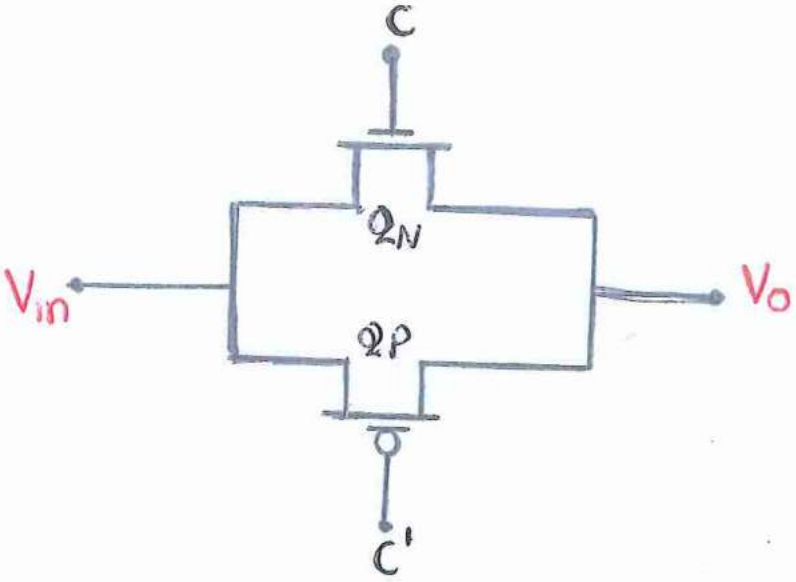
C

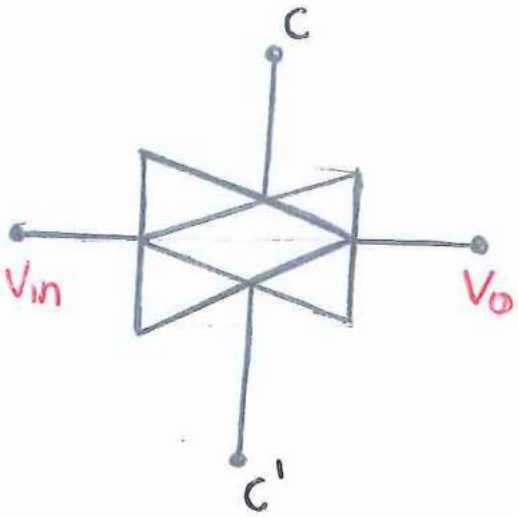


$y = A\bar{B} + \bar{A}B$ (XOR)

$Z = \bar{A}\bar{B} + AB$ (XNOR)

CMOS Transmission Gate:



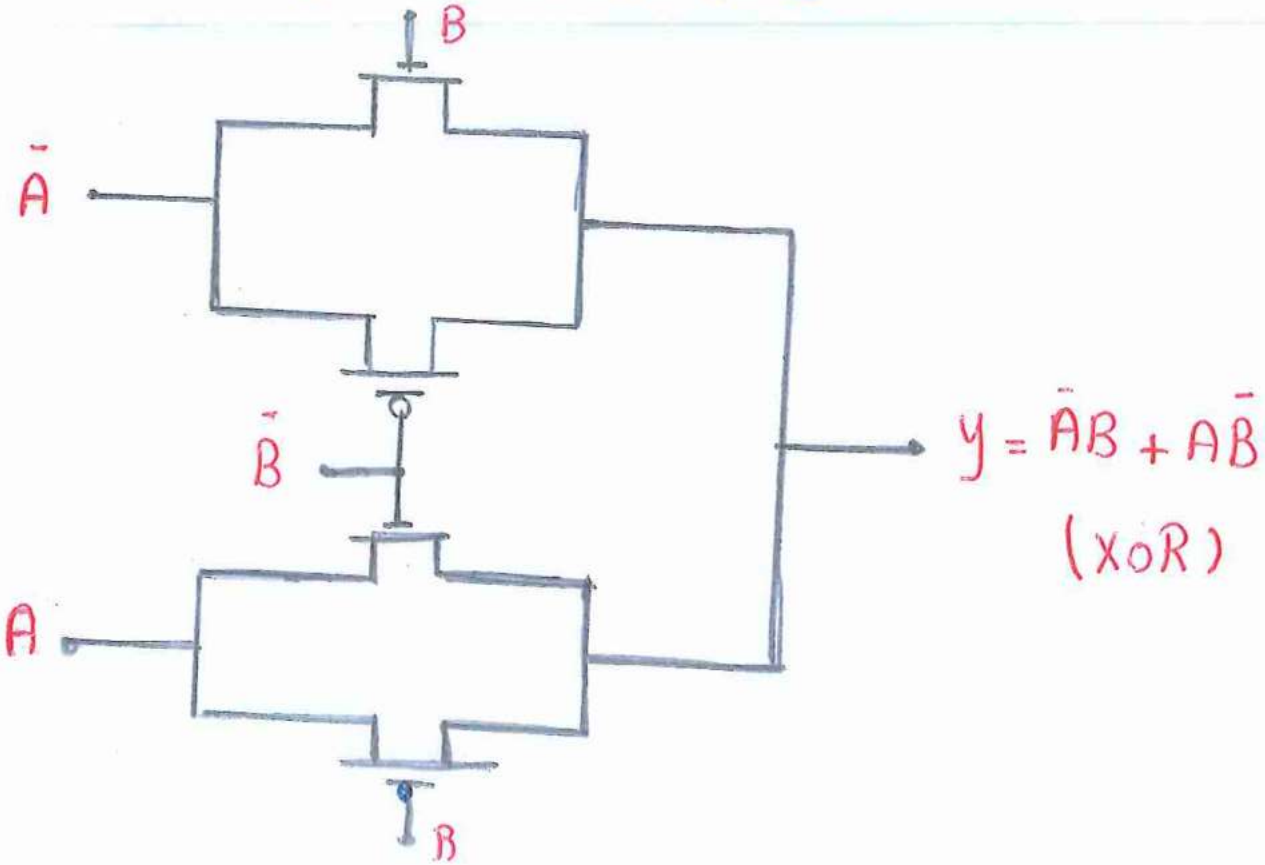


In NMOS T.G :

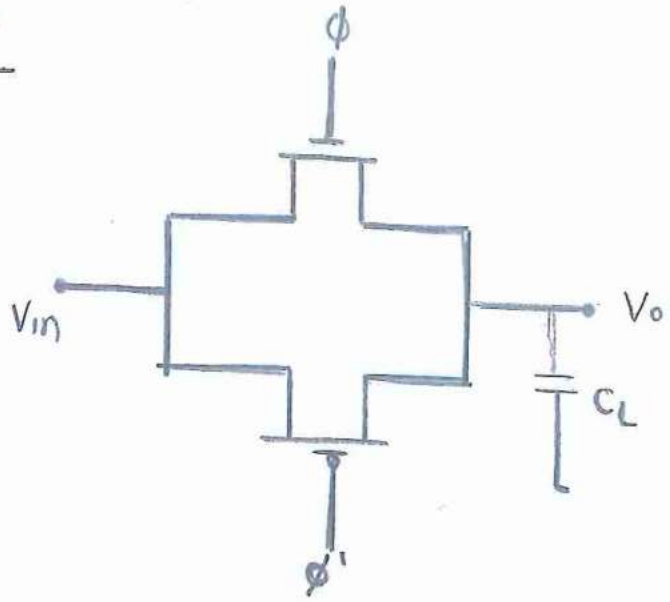
$$V_{omax} = C - V_{tn}$$

$$V_{omin} = 0$$

and $V_{in} = V_o$ when $C = 1$



For CMOS pass gate:



- For V_{in} = high

For NMOS

The $C_L = V_{DD} - V_t$

For PMOS

$C_L = V_{DD}$

- For V_{in} = Low

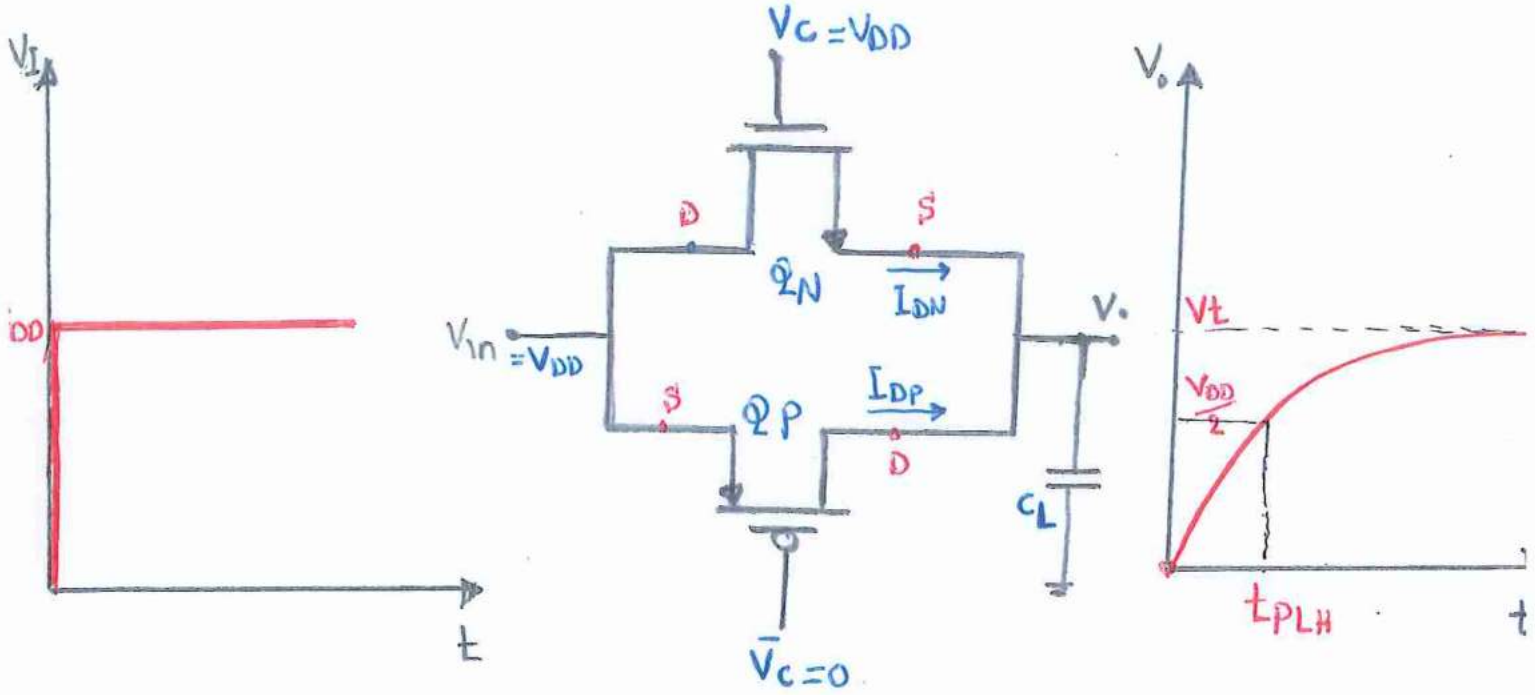
NMOS $V_o = 0$

PMOS $V_o = -V_{tp}$

So in CMOS give Strong 0 & Strong 1

operation with CMOS: (as switch)

a The input going to High:



* For N Mos:

$V_D = V_G = V_{DD}$ ∴ Mosfet alway in Sat.

$V_{GS} = V_G - V_S = V_{DD} - V_o$

$\therefore I_{DN} = \frac{1}{2} K_n (V_{GS} - V_{tn})^2$

$\therefore I_{DN} = \frac{1}{2} K_n (V_{DD} - V_o - V_{tn})^2$

and The Body effect appear on V_{tn}

For PMOS:

$$V_{SG} = V_S - V_G = V_{DD} - 0 = V_{DD}$$

$$V_{SD} = V_{DD} - V_o$$

* So no body effect ($V_S = V_{DD}$) constant.

current in saturation:

For Sat. $V_{SD} \geq V_{SG} - |V_{tp}|$

$$\therefore (V_{DD} - V_o) \geq V_{SG} - |V_{tp}|$$

$$\therefore V_{DD} - V_o \geq V_{DD} - |V_{tp}|$$

$$\therefore V_o \leq |V_{tp}|$$

So The current in Triode: $V_o > |V_{tp}|$

- Total charge current:

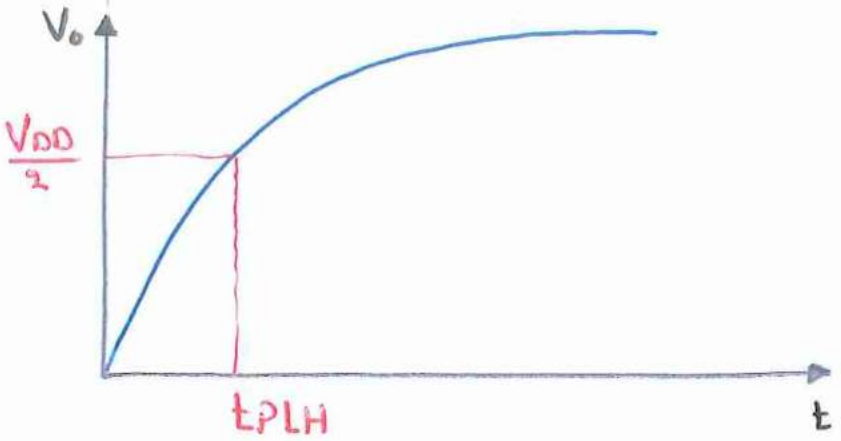
$$I_{charge} = I_{DN} + I_{DP} \quad \text{until} \quad V_o = (V_{DD} - V_{tn})$$

If ($V_o > V_{DD} - V_{tn}$): Q_N will be off

Q_P ON Till $V_o = V_{DD}$

a) The input going to high: (t_{pLH})

* $t = 0$



⊙ For Q_N:

$V_o = 0$

$V_{DS} = V_{DD}$

$V_{GS} = V_{DD}$

$\therefore I_{DN}(0) = \frac{1}{2} k_n (V_{DD} - V_{tn})^2$

* (No Body effect) $V_{tn} = V_{t_o}$

⊙ For Q_P:

$V_{SG} = V_{DD} - 0$

$V_{SD} = V_{DD} - 0$

$\therefore$ MOSFET in saturation as $V_{SG} = V_{SD}$

$\therefore I_{DP}(0) = \frac{1}{2} k_p (V_{DD} - |V_{tp}|)^2$

* (No body effect) $|V_{tp}| = V_{tn}$

* $t = t_{pLH}$

$V_o = \frac{V_{DD}}{2}$, $t = t_{pLH}$

⊙ For Q_N:

$V_o = V_S = \frac{V_{DD}}{2}$, $V_{GS} = V_{DD} - V_o = \frac{V_{DD}}{2}$

$$I_{DN}(t_{PLH}) = \frac{1}{2} K_n (V_{DD} - V_o - V_{tn})^2$$

Body effect appear:

$$V_{tn} = V_{tn0} + \gamma \left(\sqrt{\frac{V_{DD}}{2} + 2\phi_f} - \sqrt{2\phi_f} \right)$$

⊙ for Qp:

$V_{SG} = V_{DD} - 0$

$V_{SD} = V_{DD} - \frac{V_{DD}}{2} = \frac{V_{DD}}{2}$

$V_{SD} < V_{SG} - |V_{tp}|$ ∴ Qp in Triode

$$I_{DP}(t_{PLH}) = K_p \left[(V_{DD} - |V_{tp}|)\left(\frac{V_{DD}}{2}\right) - \frac{(V_{DD} - V_o)^2}{2} \right]$$

- PMOS has no Body effect.

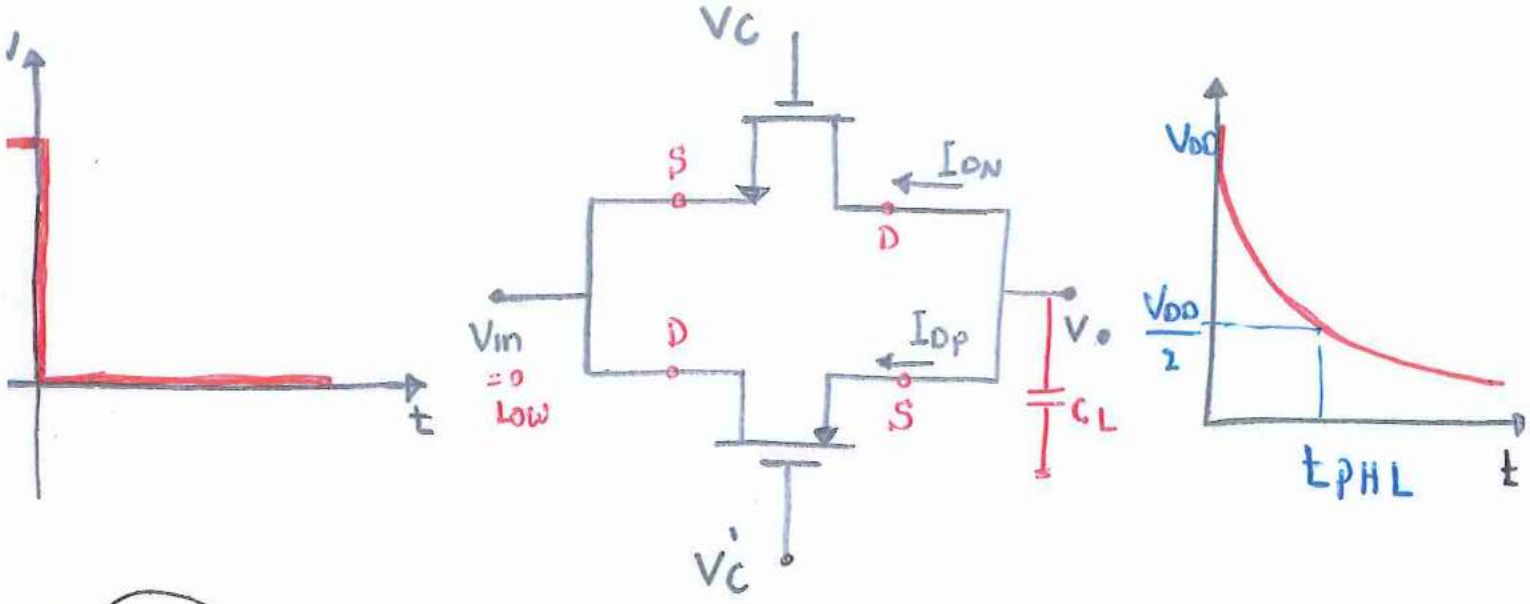
∴ $|V_{tp}| = V_{tn0}$

- $$I_{ave} = \frac{I_{DN}(t_{PLH}) + I_{DP}(t_{PLH}) + I_{DN}(0) + I_{DP}(0)}{2}$$

$$t_{PLH} = \frac{C * \frac{V_{DD}}{2}}{I_{ave}}$$

- $I_{change} = I_{DN}(t_{PLH}) + I_{DP}(t_{PLH})$

b The input going to Low: (t_{pHL})



* at $t=0$

Q_N & Q_P are ON

- Q_N has no body effect ($V_S = V_B = 0$)
- Q_P has body effect ($V_S = V_o$) varying from V_{DD} to zero

$$V_{tp} = |V_{tp0}| + \gamma \left[\sqrt{|V_{DD} - V_o| + 2\phi_f} - \sqrt{2\phi_f} \right]$$

and Q_P stop conducting at $V_o = |V_{tp}|$

Q_N conduct till $V_i = 0 = V_{OL}$

(t_{pHL}):

* at $t=0$ (Q_N) in "sat."

$V_O = V_{DD}$

$V_{DS} > V_{GS} - V_t$

$V_{DD} > V_{DD} - V_t$

↳ no body effect ($V_S = 0$)

$I_{DN(0)} = \frac{1}{2} K_n' \left(\frac{W}{L}\right) (V_{DD} - V_{t_0})^2$

For (Q_p)

$V_{SD} > V_{SG} - |V_{tp}|$

$V_{DD} > V_{DD} - |V_{tp}|$

$\therefore I_{DN(0)} = \frac{1}{2} K_n (V_{DD} - V_{t_0})^2$

$I_{DP(0)} = \frac{1}{2} K_p (V_{DD} - V_{t_0})^2$

$I_{charge(0)} = I_{DN(0)} + I_{DP(0)}$

* at $t = t_{pHL}$

$V_O = \frac{V_{DD}}{2}$

⊙ For Q_N:

$V_{DS} < V_{GS} - V_t$ ⟶ no body effect

$\frac{V_{DD}}{2} < V_{DD} - V_t$.

at Triode

$\therefore I_{DN}(t_{PHL}) = k_n'\left(\frac{W}{L}\right)\left[(V_{DD}-V_t)\frac{V_{DD}}{2} - \frac{1}{2}\left(\frac{V_{DD}}{2}\right)^2\right]$

⊙ For Q_P:

$V_{SD} > V_{SG} - |V_{tp}|$

$\frac{V_{DD}}{2} > \frac{V_{DD}}{2} - |V_{tp}|$

⟶ with body effect

at Sat.

$V_t = V_{to} + \gamma\left[\sqrt{V_{BS} + 2\phi_F} - \sqrt{2\phi_F}\right]$

and $V_{BS} = V_{DD} - \frac{V_{DD}}{2} = \frac{V_{DD}}{2} = V_o$

$I_{DP}(t_{PHL}) = \frac{1}{2}K_p\left(\frac{V_{DD}}{2} - |V_t|\right)^2$

* $I_{ave} = \frac{I(0) + I(t_{PHL})}{2}$ & $t_{PHL} = C\frac{V_{DD/2}}{I_{ave}}$

The transmission gate of Fig. 15.21(a) and 15.21(b) is fabricated in a CMOS process technology for which $k_n' = 50\ \mu A/V^2$, $k_p' = 20\ \mu A/V^2$, $V_{tn} = |V_{tp}|$, $V_{t0} = 1$ V, $\gamma = 0.5\ V^{1/2}$, $2\phi_f = 0.6$ V, and $V_{DD} = 5$ V. Let Q_N and Q_P be of the minimum size possible with this process technology, $(W/L)_n = (W/L)_p = 4\ \mu m/2\ \mu m$. The total capacitance at the output node is 70 fF. Utilize as many of the results of Example 15.3 as you need.

(a) What are the values of V_{OH} and V_{OL}?

(b) For the situation in Fig. 15.21(a), find $i_{DN}(0)$, $i_{DP}(0)$, $i_{DN}(t_{PLH})$, $i_{DP}(t_{PLH})$, and t_{PLH}.

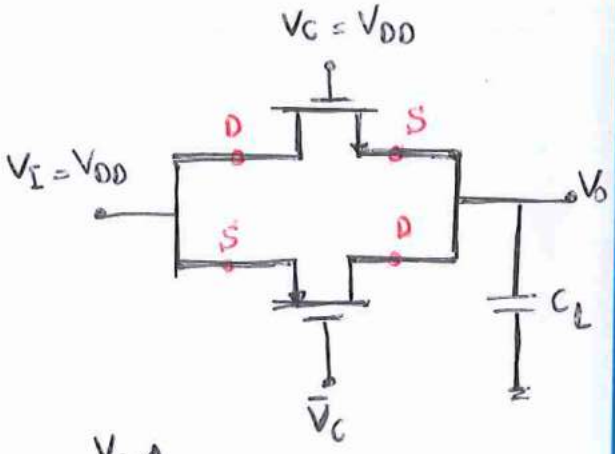
(c) For the situation depicted in Fig. 15.21(b), find $i_{DN}(0)$, $i_{DP}(0)$, $i_{DN}(t_{PHL})$, $i_{DP}(t_{PHL})$, and t_{PHL}. At what value of v_O will Q_P turn off?

(d) Find t_p.

(a) $V_{OH} = V_{DD} = 5V$

$V_{OL} = 0$

(b)



at $t=0$

$I_{DP}(0) = \frac{1}{2} K_p' \left(\frac{W}{L}\right)_p (V_{DD} - V_{tp})^2$

$= \frac{1}{2} * 20 * \frac{4}{2} (5-1)^2$

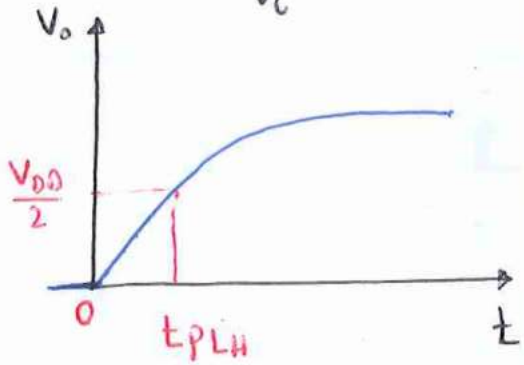
$I_{DP}(0) = 320\mu A$

$I_{DN}(0) = \frac{1}{2} K_n' \left(\frac{W}{L}\right)_n (V_{DD} - V_{to})^2$

$= \frac{1}{2} * 50 * \frac{4}{2} (5-1)^2$

$= 800\mu A$

$I_C(0) = I_{DP}(0) + I_{DN}(0) = 1120\mu A \longrightarrow (1)$



V_{tn}:

$$V_{tn} = V_{to} + \gamma\left[\sqrt{V_o + 2\phi_f} - \sqrt{2\phi_f}\right]$$

$$= 1 + 0,5\left[\sqrt{\frac{5}{2} + 0,6} - \sqrt{0,6}\right]$$

$$V_{tn} = 1,493\ V$$

$$I_{DN}(t_{PLH}) = \frac{1}{2} k_n (V_{DD} - V_o - V_{tn})^2$$

$$= \frac{1}{2} * 100 (5 - 2,5 - 1,493)^2$$

$$= 50,7\ \mu A$$

V_{tp}:

$$|V_{tp}| = V_{tn} = 1,493\ V$$

$$I_{DP}(t_{PLH}) = K_p\left[(V_{DD} - V_t)(V_{DD} - V_o) - \frac{(V_{DD} - V_o)^2}{2}\right]$$

$$= 20 * \frac{4}{2}\left[(5-1)\frac{5}{2} - \frac{1}{2} * \left(\frac{5}{2}\right)^2\right]$$

$$= 275\ \mu A$$

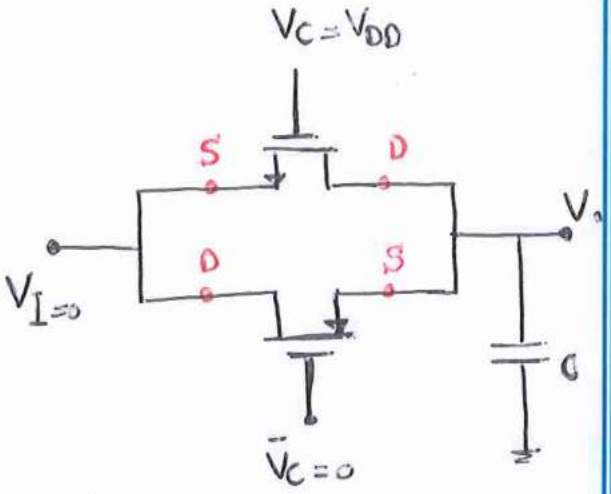
$$I_C(t_{PLH}) = 50 + 275 = 325\ \mu A$$

$$I_{C\,ave} = \frac{1120 + 325}{2} = 722,5\ \mu A$$

$$t_{PLH} = \frac{C\left(\frac{V_{DD}}{2}\right)}{I_{Cave}}$$

$$= \frac{10fF * 2.5}{772.5 * 10^{-6}} = 0.249\,nS$$

(C)



$$I_{DN(0)} = \frac{1}{2} K_n'\left(\frac{W}{L}\right)(V_{DD} - V_{t_0})^2$$

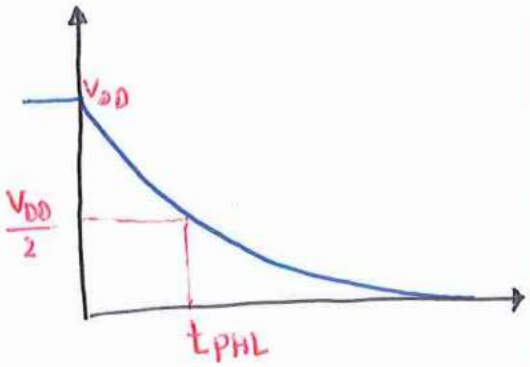
$$= \frac{1}{2} * 50 * \frac{4}{2}(5-1)^2$$

$$= 800\,\mu A$$

$$I_{DP(0)} = \frac{1}{2} K_p'\left(\frac{W}{L}\right)_P (V_{DD} - V_{t_0})^2$$

$$= \frac{1}{2} * 20 * \frac{4}{2}(5-1)^2$$

$$= 320\,\mu A$$



$\therefore I_{C(0)} = I_{DP(0)} + I_{DN(0)} = 1120\,\mu A$

at $t = t_{PHL}$

$$I_{DN(t_{PHL})} = K_n'\left(\frac{W}{L}\right)\left[(V_{DD} - V_{t_0})\frac{V_{DD}}{2} - \frac{\left(\frac{V_{DD}}{2}\right)^2}{2}\right]$$

$$= 688.2\,\mu A$$

V_{tp}:

$$|V_{tp}| = V_{to} + \gamma \left[\sqrt{V_{DD} - V_o + 2\phi_f} - \sqrt{2\phi_f} \right]$$

$$= 1 + 0,5 \left[\sqrt{5 - 0 + 0,6} - \sqrt{0,6} \right]$$

$$= 1,49 \text{ V}$$

$$I_{DP(tPHL)} = \frac{1}{2} * 20 * \frac{4}{2} \left[2,5 - 1,49 \right)^2$$

$$= 20 \text{ MA}$$

$$I_{C(ave)} = \frac{1120 + 708}{2} = 914 \text{ MA}$$

$$t_{PHL} = \frac{C * \frac{V_{DD}}{2}}{I_{ave}} = 0,192 \text{ nS}$$

- The transistor Qp will be off when the output voltage is $V_o = |V_{tp}|$

$$|V_{tp}| = V_{to} + \gamma \left[\sqrt{V_{DD} - |V_{tp}| + 2\phi_f} - \sqrt{2\phi_f} \right]$$

$$\left(|V_{tp}| - 1 + \frac{1}{2}\sqrt{0,6} \right)^2 = \frac{1}{2} \left(5 - |V_{tp}| + 0,6 \right)$$

$$(|V_{tp}|)^2 - 0,976 |V_{tp}| - 1,024 = 0$$

$\therefore |V_{tp}| = 1,6\,V$

(d) $t_p = \dfrac{t_{pHL} + t_{pLH}}{2}$

$= \dfrac{0,24 + 0,19}{2}$

$t_p = 0,22\,nS$

Consider the NMOS transistor switch in the circuits of Figs. 15.17 and 15.18 to be fabricated in a technology for which $\mu_n C_{ox} = 50\ \mu A/V^2$, $\mu_p C_{ox} = 20\ \mu A/V^2$, $|V_{t0}| = 1\ V$, $\gamma = 0.5\ V^{1/2}$, $2\phi_f = 0.6\ V$, and $V_{DD} = 5\ V$, where ϕ_f is a physical parameter. Let the transistor be of the minimum size for this technology, namely, 4 μm/2 μm, and assume that the total capacitance between the output node and ground is $C = 50\ fF$.

(a) For the case with v_I high (Fig. 15.17), find V_{OH}.
(b) If the output feeds a CMOS inverter whose $(W/L)_p = 2.5\,(W/L)_n = 10\ \mu m/2\ \mu m$, find the static current of the inverter and its power dissipation when its input is at the value found in (a). Also find the inverter output voltage.
(c) Find t_{PLH}.
(d) For the case with v_I going low (Fig. 15.18), find t_{PHL}.
(e) Find t_p.

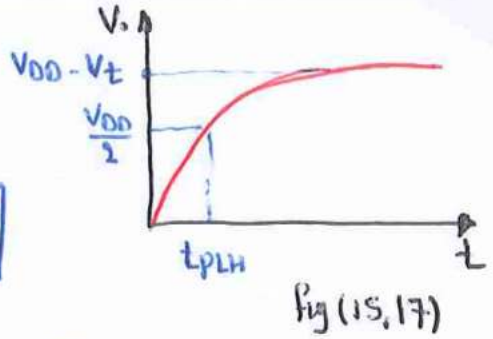


Fig (15.17)

(a) $V_{OH} = V_{DD} - V_t$

$$V_t = V_{t0} + \gamma\left[\sqrt{V_{OH} + 2\phi_f} - \sqrt{2\phi_f}\right]$$

$$V_t = V_{t0} + \gamma\left[\sqrt{V_{DD} - V_t + 2\phi_f} - \sqrt{2\phi_f}\right]$$

$$V_t = 1 + 0.5\left[\sqrt{5 - V_t + 0.6} - \sqrt{0.6}\right]$$

$\therefore V_t = 1.6$ Volt

$\therefore V_{OH} = V_{DD} - 1.6 = 3.4\ V$

(b) $I_{DP} = \frac{1}{2} K_p' \left(\frac{W}{L}\right)_p (V_{DD} - V_{OH} - V_t)^2$

$= \frac{1}{2} * 20 * \frac{10}{2} (5 - 3.4 - 1)^2 = 18\ \mu A$

$P_D = I_{DP} V_{DD}$

$= 5 * 18$

$= 90 \mu W$

(c)

at $t = 0$

$V_O = 0$

$V_t = V_{to} = 1\,V$

at $t = t_{PLH}$

$V_O = 2,5$

$V_t = ??$

$$I_{D(0)} = \frac{1}{2} * 50 * \frac{4}{5} (5-1)^2 = 800 \mu A$$

$$V_t (at\ V_O = 2,5) = 1 + 0,5 (\sqrt{2,6+0,6} - \sqrt{0,6}) = 1,49\,V$$

$$I_{D(t_{PLH})} = \frac{1}{2} * 50 * \frac{4}{2} (5 - 2,5 - 1,49)^2 = 50 \mu A$$

$$\therefore I_{Dave} = \frac{800 + 50}{2} = 425 \mu A$$

$$\therefore t_{PLH} = \frac{C * (\frac{V_{DD}}{2})}{I_{Dave}} = \frac{50 * 10^{-15} * 2,5}{425 * 10^{-6}} = 0,29\,ns$$

(d)

$$I_{D(0)} = \frac{1}{2} * 50 * \frac{4}{2} (5-1)^2 = 800 \mu A \qquad V_t = V_{to}$$

at $t = t_{pHL}$ Q in triode

$$I_D(t_{pHL}) = 50 * \frac{4}{2}\left[(5-1)2,5 - \frac{2,5^2}{2}\right]$$

$$= 688\,\mu A$$

$$\therefore I_{D\,avg} = \frac{800+688}{2} = 744\,\mu A$$

$$t_{pHL} = \frac{50 * 10^{-15} * 2,5}{744 * 10^{-6}} = 0,17\,ns$$

(e) $$t_p = \frac{t_{pHL}+t_{pLH}}{2} = 0,23\,ns$$

Example:

a Transmission gate circuit is fabricated in CMOS proce technology for which $K_n' = 4K_p' = 300\ \mu A/V^2$

$|V_{to}| = 0,5$ Volt

$\gamma = 0,3$

$2\phi_F = 0,85$ V

$V_{DD} = 1,8$ Volt

Let Q_N & Q_P have $(W/L)_n = (W/L)_p = 1,5$ and the total capacitance at the output node is 15 Ff.

(a) What are the value of V_{OH} and V_{OL}.

$V_{OH} = V_{DD} = 1,8$ V

$V_{OL} = 0$

(b) Find $I_{DN(0)}$, $I_{DP(0)}$, $I_{DN}(t_{PHL})$, $I_{DP}(t_{PHL})$ & t_{PHL}

$$I_{DN(0)} = \frac{1}{2} K_n' \left(\frac{W}{L}\right) (V_{DD} - V_t)^2$$

$$\therefore I_{DN(0)} = 380,3\ \mu A$$

$$I_{DP(0)} = \frac{1}{2} K_p' \left(\frac{W}{L}\right) (V_{DD} - |V_t|)^2 = 95,1\ \mu A$$

$t = t_{PLH}$ @ $V_o = \frac{V_{DD}}{2}$

V_{tn} (Body effect) $= V_{tno} + \gamma \left[\sqrt{\frac{V_{DD}}{2} + 2\phi_f} - \sqrt{2\phi_f} \right]$

$\therefore V_{tn} = 0,62$ Volt

$I_{DN}(t_{PLH}) = \frac{1}{2} K_n \left(V_{DD} - \frac{V_{DD}}{2} - V_t \right)^2$

$\therefore I_{DN}(t_{PLH}) = 17,69$ MA

$I_{DP}(t_{PLH}) = K_p' \left(\frac{W}{L}\right) \left[(V_{DD} - V_t)\left(\frac{V_{DD}}{2}\right) - \frac{1}{2}\left(\frac{V_{DD}}{2}\right)^2 \right]$

$= 86,1$ MA $\quad \left(\frac{V_{DD}}{2} > |V_{tp}| \right)$ Triode

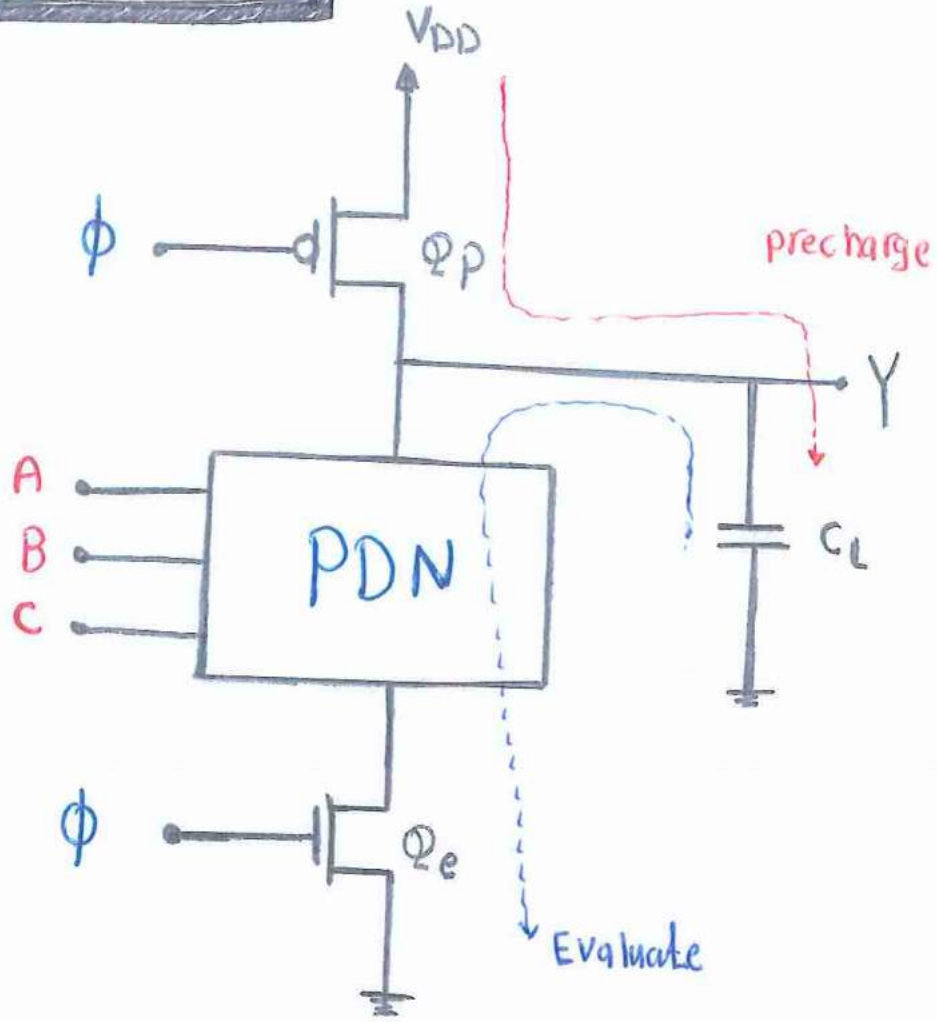
$\therefore I_{Dave} = \frac{I_{DN}(0) + I_{DP}(0) + I_{DN}(t_{PLH}) + I_{DP}(t_{PLH})}{2}$

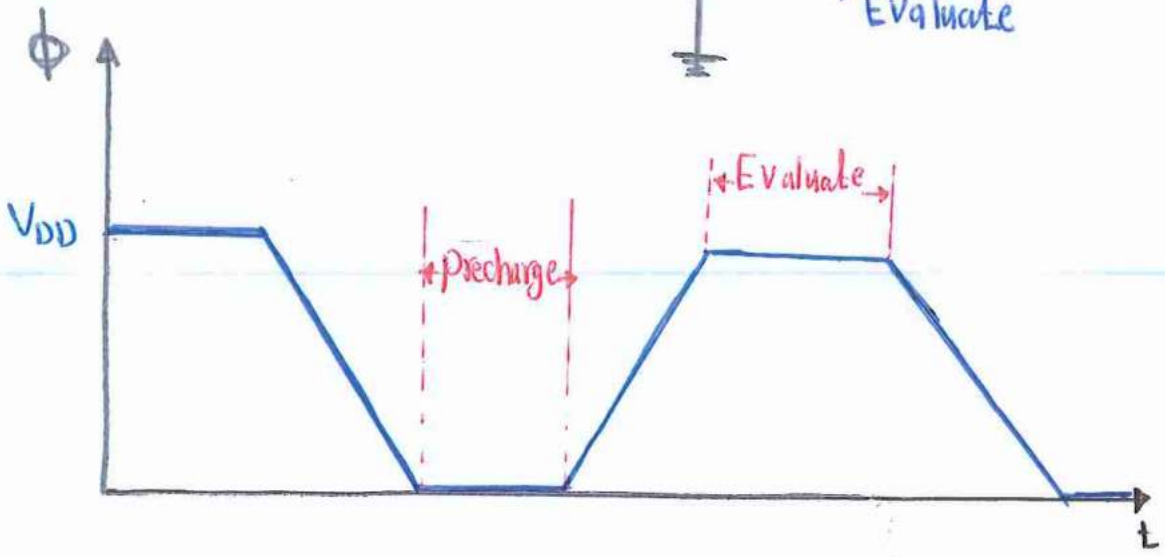
$= 290$ MA

$\therefore t_{PLH} = \frac{C * V_{DD}/2}{I_{Dave.}} = 0,097$ ns

Clock CMOS (Dynamic CMOS):

* $V_{OH} = V_{DD}$
* $V_{OL} = 0$
* to Avoide Static power dissipation
* to get Stronge Zero





* $\phi = 0$ (disable) (precharge) [Charge The capacitor]

Vo reach (rise) to It's high Level $V_{OH} = V_{DD}$ and Vo didn't depend on The input state.

Q_p ⟶ ON Q_e ⟶ off

* $\phi = 1$ (evaluation) "read" [discharge the capacitor]

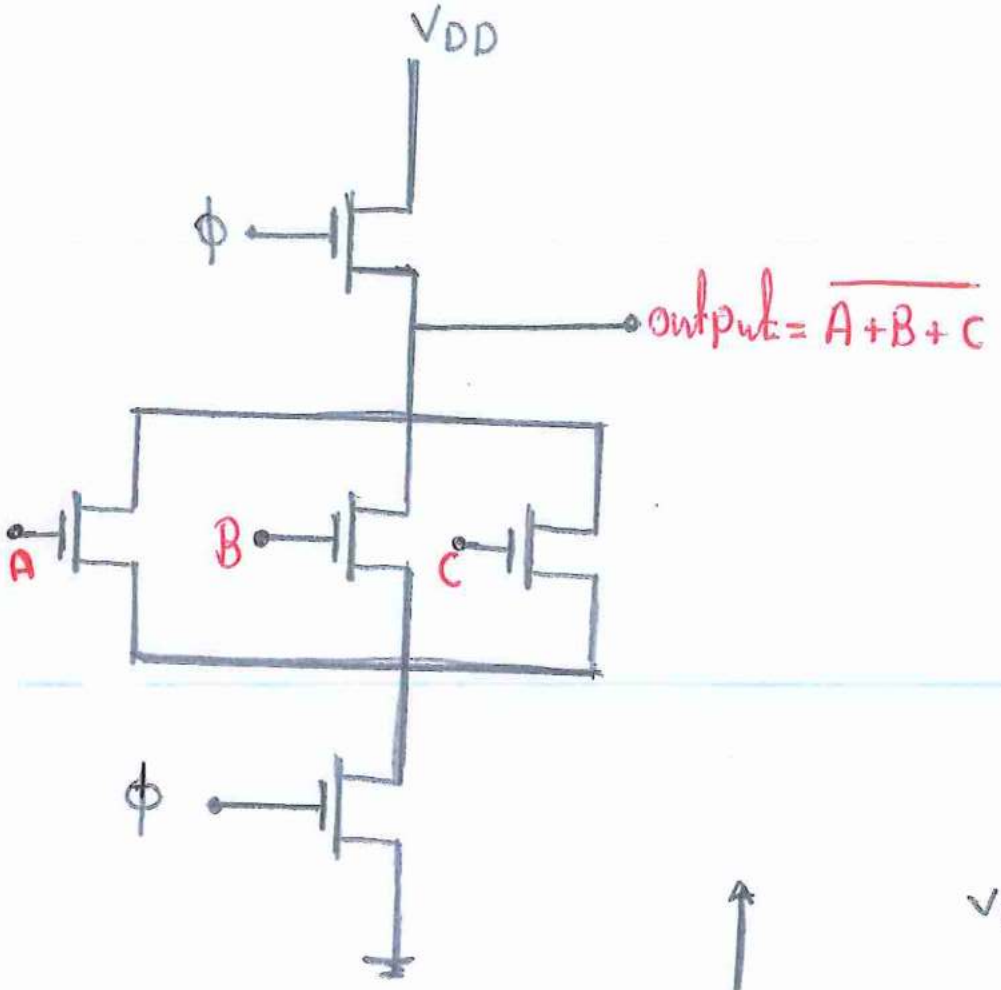
$Q_p \rightarrow$ off
$Q_e \rightarrow$ ON

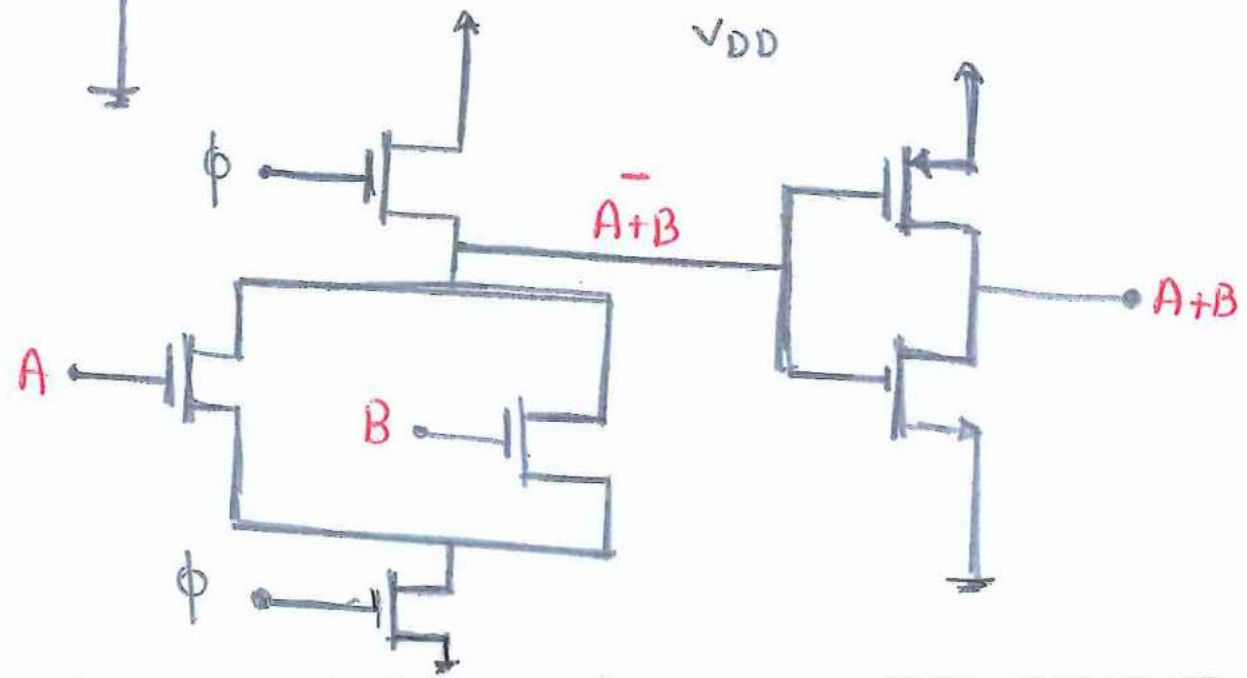
Vo depends on the input state

* between input / output

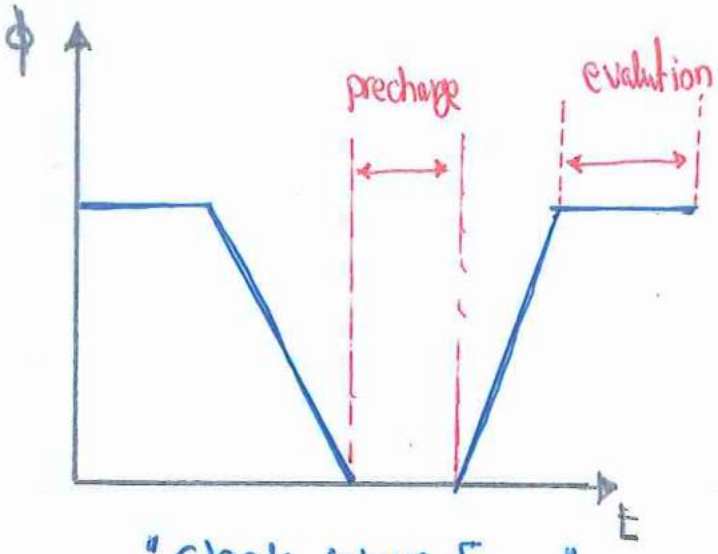
(tPHL) may be calculated

(tPLH) = 0 Vo precharge at V_{DD}

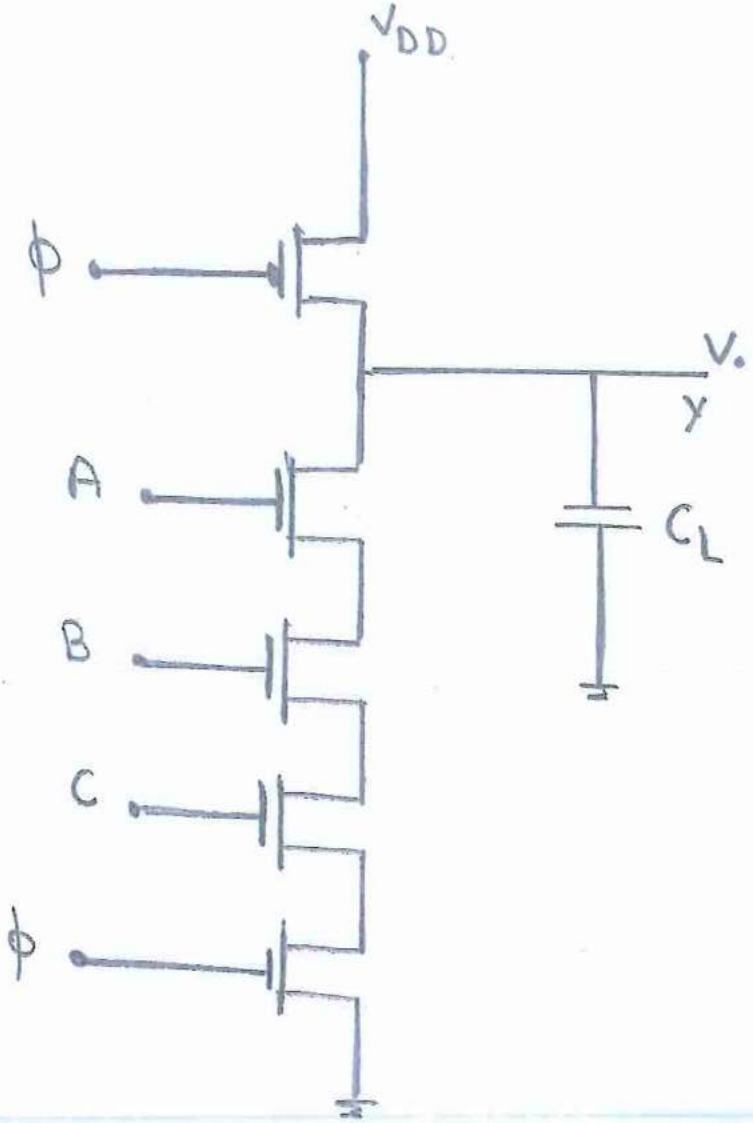




Dynamic NAND Gate:

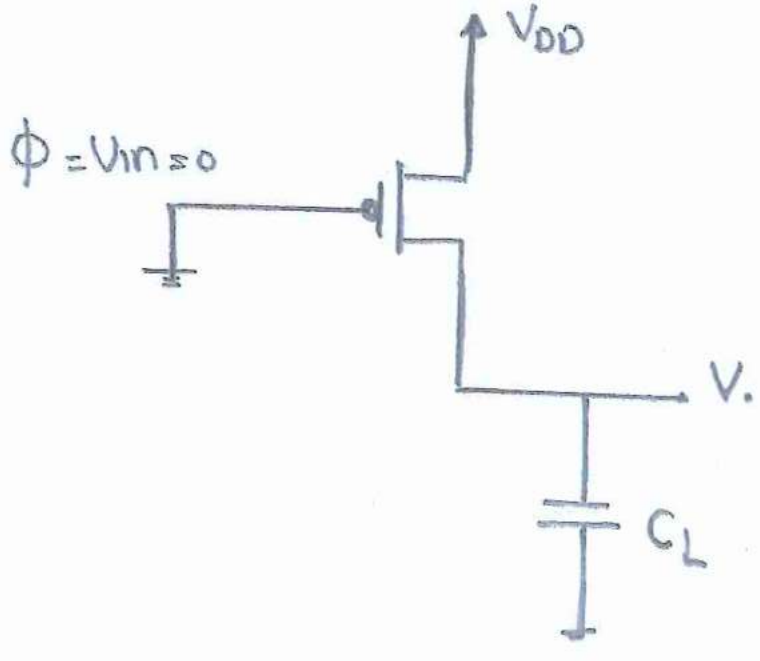


"Clock Wave Form"

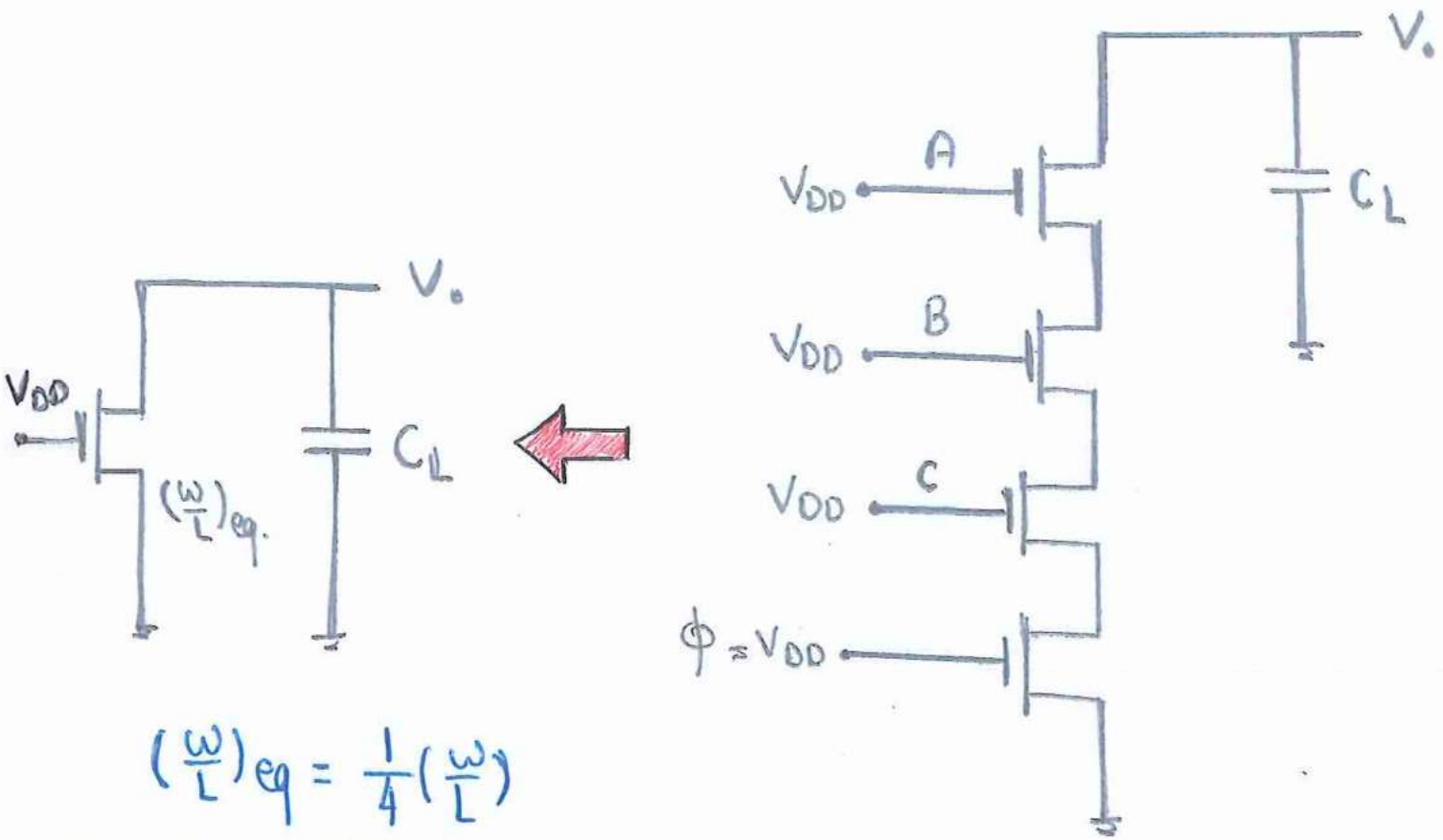


$$y = \overline{ABC}$$

For precharge: ($\phi = 0$)



evaluation: ($\phi = 1$)



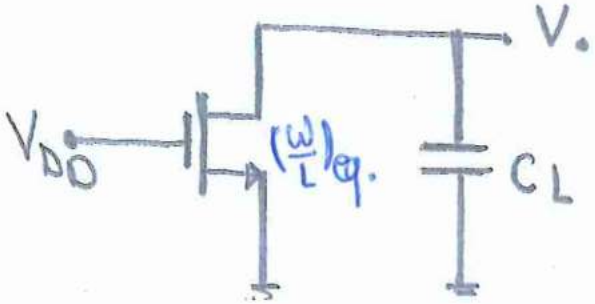
$$\left(\frac{W}{L}\right)_{eq} = \frac{1}{4}\left(\frac{W}{L}\right)$$

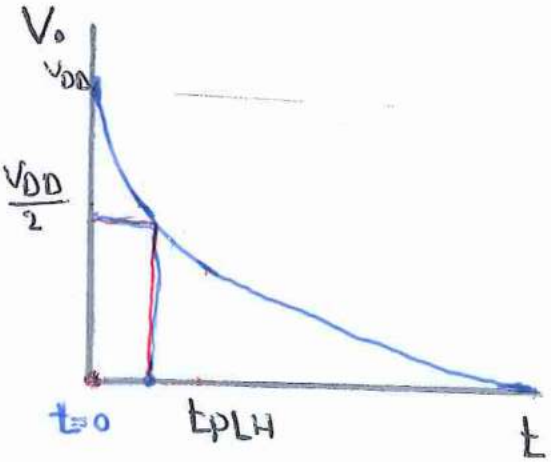
to Find t_{PLH}:

$$t_{PHL} = \frac{C\,\Delta V}{I_{ave}} = \frac{\frac{1}{2} C * V_{DD}}{I_{ave}}$$

to Find t_{PHL}:

at $t = 0 \longrightarrow V_O = 0$

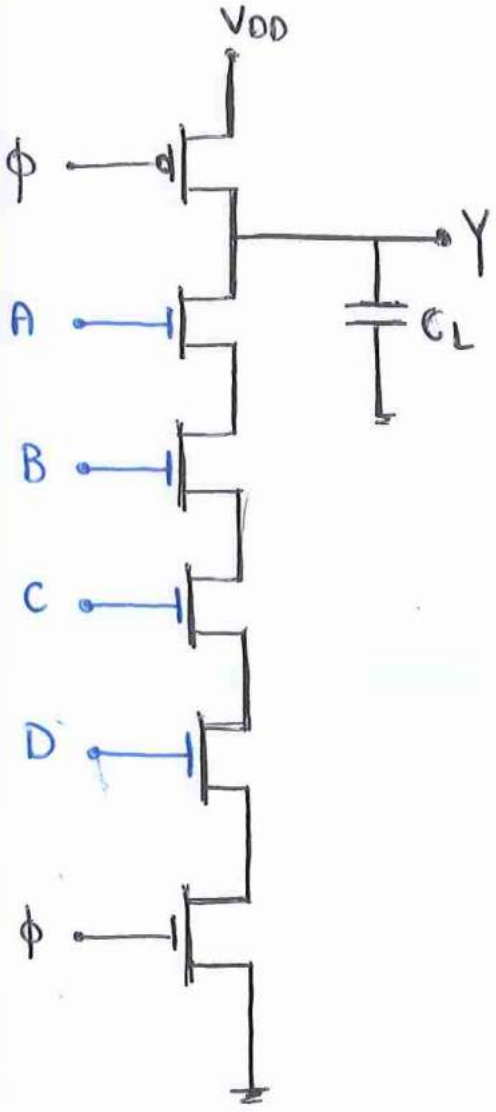




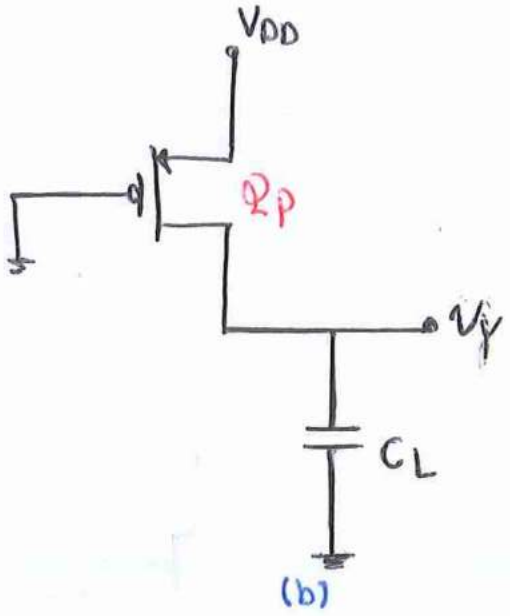
Consider the four-input, dynamic logic NAND gate shown in Fig. 15.29(a). Assume that the gate is fabricated in a 0.18-μm CMOS technology for which $V_{DD} = 1.8$ V, $V_t = 0.5$ V, and $\mu_n C_{ox} = 4\mu_p C_{ox} = 300\ \mu A/V^2$. To keep C_L small, NMOS devices with $W/L = 0.27\ \mu m/0.18\ \mu m$ are used (including transistor Q_e). The PMOS precharge transistor Q_p has $W/L = 0.54\ \mu m/0.18\ \mu m$. The total capacitance C_L is found to be 20 fF.

(a) Consider the precharge operation [Fig. 15.29(b)] with the gate of Q_p at 0 V, and assume that at $t = 0$, C_L is fully discharged. Calculate the rise time of the output voltage, defined as the time for v_Y to rise from 10% to 90% of the final voltage V_{DD}.

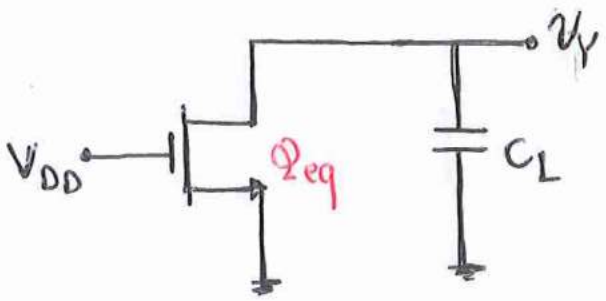
(b) For $A = B = C = D = 1$, find the value of t_{PHL}.



(A)



(b)



(C)

(a)

$V_Y = 0,1\,V_{DD} = 0,18V$

Qp will operate in Sat.

$$I_D(0,1V_{DD}) = \frac{1}{2} K_p' \left(\frac{W}{L}\right)_p (V_{DD} - |V_{tp}|)^2$$

$$= \frac{1}{2} * 75 * \frac{0,54}{0,18} (1,8 - 0,5)^2$$

$$= 190,1\ \mu A$$

at $V_Y = 0,9\,V_{DD} = 1,62$

Qp will be in Triode

$$I_D(0,9V_{DD}) = K_p \left(\frac{W}{L}\right)_p \left[(V_{DD} - |V_{tp}|)(V_{DD} - 0,9V_{DD}) - \frac{(V_{DD} - 0,9V_{DD})^2}{2} \right]$$

$$= 49\ \mu A$$

$$\therefore I_{ave} = \frac{190,1 + 49}{2} = 119,6\ \mu A$$

The rise time t_r will be

$$t_r = \frac{C\,\Delta V_Y}{I_{ave}} = \frac{C(0,9 - 0,1)V_{DD}}{I_{ave}}$$

$$t_r = 0,24\,ns$$

(b) When $A=B=C=D=1$ all NMOS will be conducting during evaluation phase.

$$Q_{eq} = \left(\frac{W}{L}\right)_{eq} = \frac{1}{5}\left(\frac{W}{L}\right) = \frac{1}{5} * 1,5 = 0,3$$

at $V_Y = V_{DD} \rightarrow Q_{eq}$ will be operating in sat.

$$I_{D(V_{DD})} = \frac{1}{2} K_n' \left(\frac{W}{L}\right)_{eq} (V_{DD} - V_t)^2$$

$$= \frac{1}{2} * 300 * 0,3 (1,8-0,5)^2$$

$$= 76,1\ \mu A$$

at $V_Y = \frac{V_{DD}}{2}$ Q_{eq} will be operating in triode

$$I_D\left(\frac{V_{DD}}{2}\right) = K_n' \left(\frac{W}{L}\right)_{eq} \left[(V_{DD}-V_t)\frac{V_{DD}}{2} - \frac{1}{2}\left(\frac{V_{DD}}{2}\right)^2\right]$$

$$= 300 * 0,3 \left[(1,8-0,5)\left(\frac{1,8}{2}\right) - \frac{1}{2}\left(\frac{1,8}{2}\right)^2\right]$$

$$= 68,9\ \mu A$$

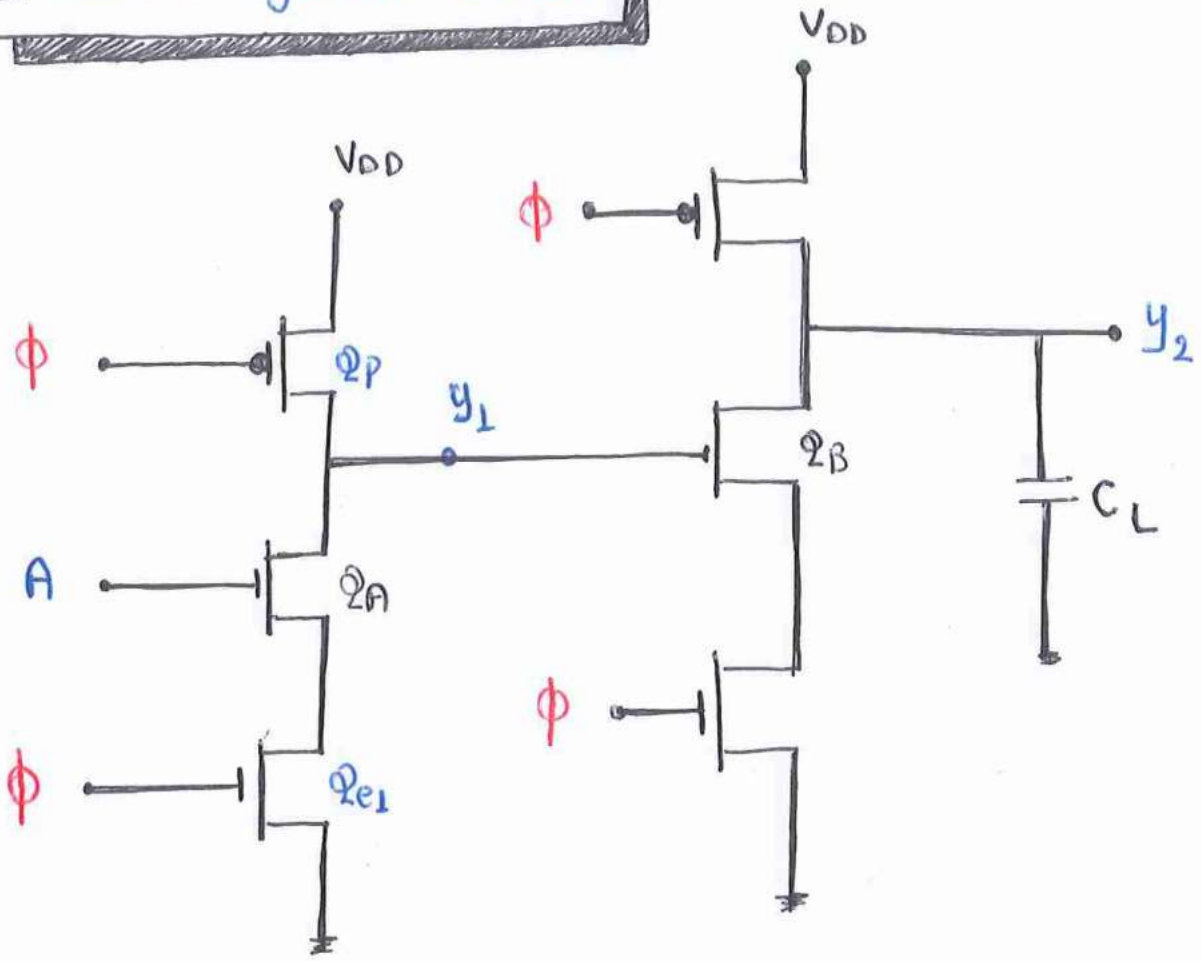
$$I_{ave} = \frac{76,1 + 68,9}{2} = 72,5\ \mu A$$

$$t_{PHL} = \frac{C\left(V_{DD} - \frac{V_{DD}}{2}\right)}{I_{ave}}$$

$$= \frac{20 * 10^{-19}(1,8-0,9)}{72,5 * 10^{-6}}$$

$$= 0,25 \text{ nS}$$

Cascade Dynamic CMOS:



* $y_1 = \bar{A}$ and $y_2 = A$

at $\phi = 0$ "Precharge condition":

$Q_p \longrightarrow$ ON

$Q_{e_1} \longrightarrow$ off

$V_{y_1} = V_{DD}$ and $V_{y_2} = V_{DD}$

- at $\phi = 1$ "Evaluation condition":

$Q_p \longrightarrow$ off

$Q_{e_1} \longrightarrow$ ON

$y_1 = high$

- If $V_{y_1} < V_{tn}$ $\therefore$ $Q_B \longrightarrow$ off

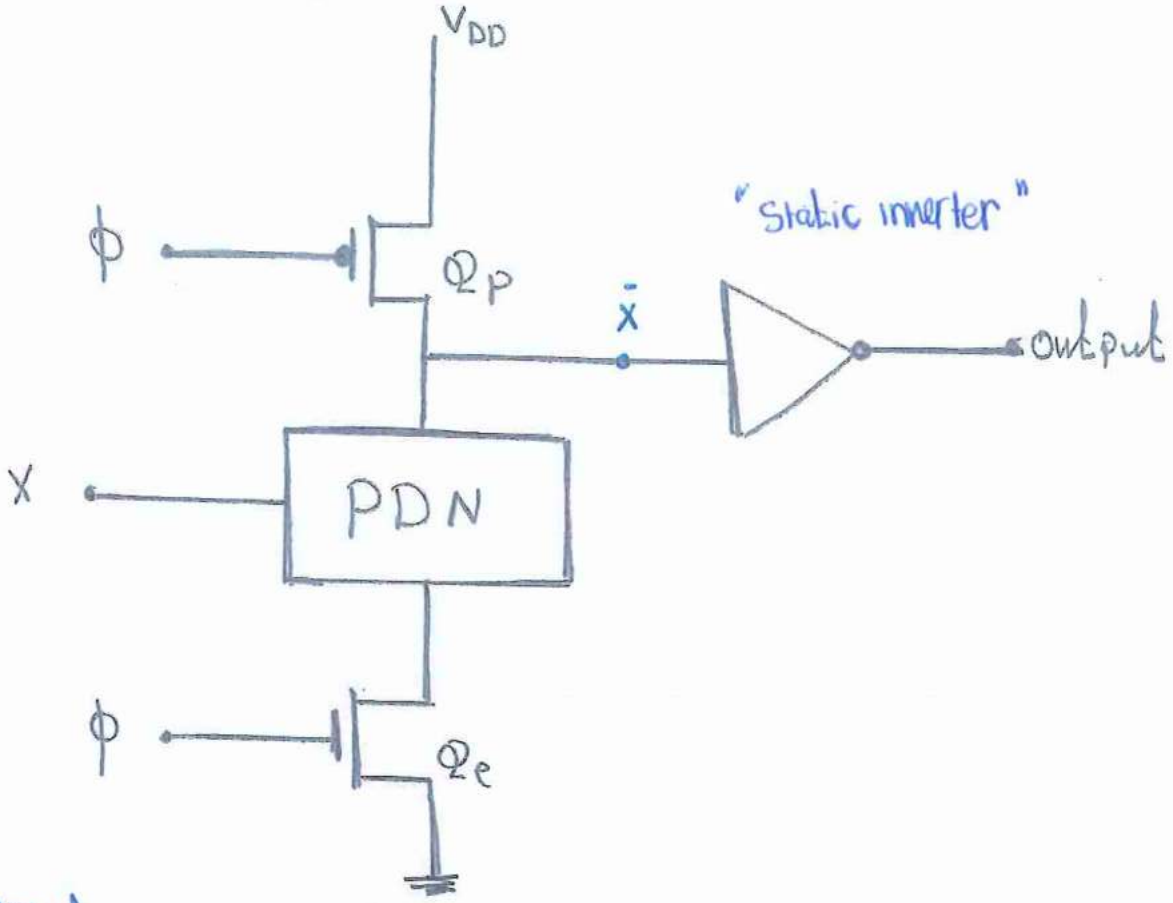
$\therefore V_{y_2} = 0$

- In cascade Dynamic CMOS During evaluation Q_B has to be stay ON If $V_{y_1} > V_{t_2}$ Q_2 ON

If $V_{y_1} < V_{t_2}$ Q_2 off

So we need to use buffer inverter at the output.

Domino CMOS (dynamic):



◎ During precharge:

$\phi = 0$

$\bar{x} = V_{DD}$

$\therefore$ output $= 0$ "good Logic 0"

◎ During evaluation:

X = high $\longrightarrow$ $\bar{x} = 0$

$\therefore$ output $= V_{DD}$ "good Logic 1"

Example:

Implement $Y = (A+B)C$ using two stages cascaded domino.