



Kuwait University
2020

ELECTRONICS III



PSEUDO-NMOS Logic Circuits

Chapter 15 - Part (1)



Eng. MohaMeD GHoNiM

96676657



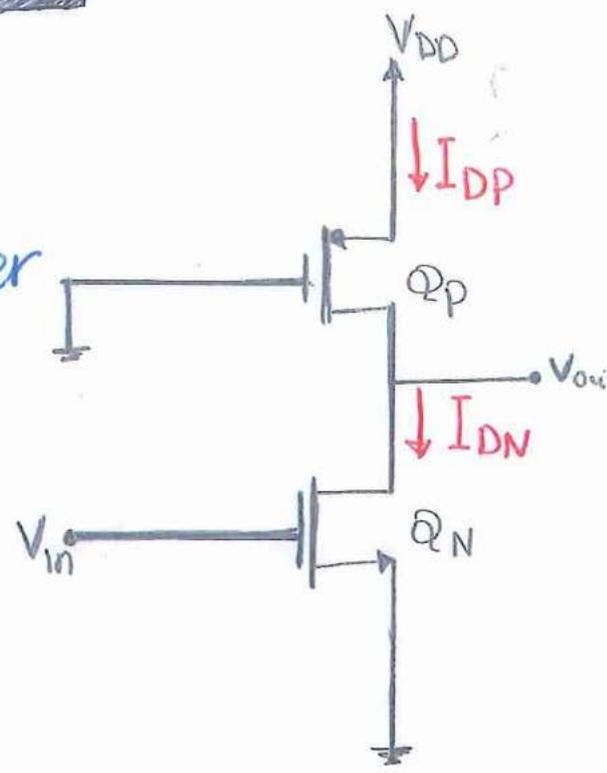
4

The Pseudo-NMOS inverter:

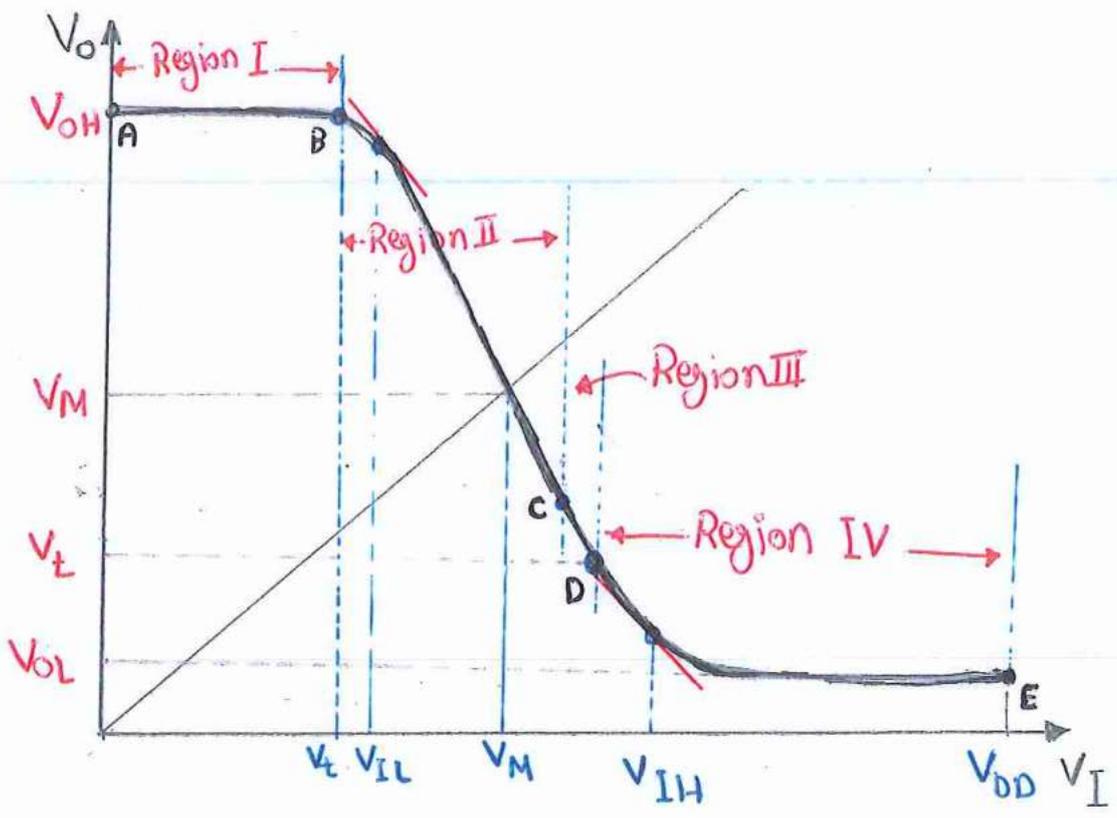
The Pseudo NMOS is similar to the depletion Load NMOS inverter

It has the advantage of being compatible with CMOS:

- (1) Faster
- (2) simple



The Voltage Transfer Characteristic (VTC):



Region	segment on VTC	Q_N	Q_P	Condition
Region I	A to B	off	Triode	$V_I < V_T$
Region II	B to C	saturation	Triode	$V_O \geq V_I - V_T$
Region III	C to D	Triode	Triode	$V_T \leq V_O \leq V_I - V_T$
Region IV	D to E	Triode	saturation	$V_O \leq V_T$

☐ in pseudo-NMOS inverter The Q_P always ON and Q_N can be off.

☐ For NMOS:

(1) in sat:

$$V_{DS} > V_{GS} - V_T$$

$$\therefore V_O > V_{in} - V_T$$

$$\therefore I_{DN} = \frac{1}{2} K_n' \left(\frac{W}{L}\right) (V_{in} - V_t)^2$$

(2) in Linear Region:

$$V_{DS} < V_{GS} - V_t$$

$$\therefore I_{DN} = K_n' \left(\frac{W}{L}\right) \left[(V_{in} - V_t) V_o - \frac{V_o^2}{2} \right]$$

$$\begin{bmatrix} V_{DS} = V_o \\ V_{GS} = V_{in} \end{bmatrix}$$

For P MOS:

(1) in Sat:

$$I_{DP} = \frac{1}{2} K_p' \left(\frac{W}{L}\right) (V_{DD} - V_{tp})^2$$

$$\begin{bmatrix} V_o = V_D \\ V_{DD} = V_S \\ \therefore V_{SD} = V_{DD} - V_o \\ V_{SG} = V_{DD} \end{bmatrix}$$

(2) in Linear:

$$I_{DP} = K_p' \left(\frac{W}{L}\right) \left[(V_{DD} - V_{tp})(V_{DD} - V_o) + \frac{(V_{DD} - V_o)^2}{2} \right]$$

operation Region in Pseudo:

1

Region I:

$$V_{in} < V_t$$

$$* V_{tn} = -V_{tp} = V_t$$

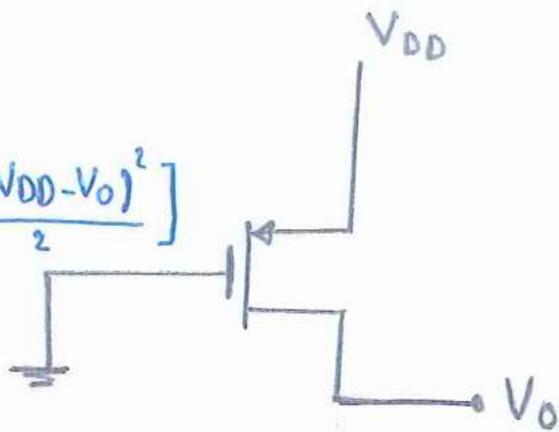
$$* K_R = \frac{K_n}{K_p} = \frac{K_n' \left(\frac{W}{L}\right)}{K_p' \left(\frac{W}{L}\right)}$$

Q_N is off , $I_{DN} = 0$

Q_P is ON (Triode)

$$I_{DP} = K_P \left[(V_{DD} - V_t)(V_{DD} - V_o) - \frac{(V_{DD} - V_o)^2}{2} \right]$$

$V_o = V_{DD} = V_{OH}$



2 Region II:

Q_N is sat. , $I_{DN} = \frac{1}{2} K_n (V_I - V_t)^2$

Q_P is Triode , $I_{DP} = K_P \left[(V_{DD} - V_t)(V_{DD} - V_o) - \frac{(V_{DD} - V_o)^2}{2} \right]$

$$I_{DN(sat)} = I_{DP(Linear)}$$

$$\frac{1}{2} K_n (V_I - V_t)^2 = K_P \left[(V_{DD} - V_t)(V_{DD} - V_o) - \frac{(V_{DD} - V_o)^2}{2} \right]$$

$\therefore V_o = V_t + \sqrt{(V_{DD} - V_t)^2 - K_R (V_I - V_t)^2}$

9 to find V_{IL} :

$$\text{Take } \frac{dV_o}{dV_i} = -1 \quad \Big|_{V_i = V_{IL}}$$

$$\therefore \frac{dV_o}{dV_i} = 0 + \frac{1}{2} \left[(V_{DD} - V_t)^2 - K_R (V_{in} - V_t)^2 \right]^{-1/2} \cdot (-2K_R (V_{IL} - V_t))$$

$$\therefore -1 = \left[(V_{DD} - V_t)^2 - K_R (V_{IL} - V_t)^2 \right]^{-1/2} \cdot (-K_R) (V_{IL} - V_t)$$

$$\therefore V_{IL} = V_t + \frac{V_{DD} - V_t}{\sqrt{K_R (K_R + 1)}}$$

b The Threshold Voltage (V_M): is definition by the value of V_i for which equal V_o or $\text{slop} = 1$.

$$V_o = V_{in} = V_M$$

$$\therefore V_M = V_t + \frac{V_{DD} - V_t}{\sqrt{K_R + 1}}$$

$$\rightarrow V_M = V_t + \sqrt{(V_{DD} - V_t)^2 - K_R (V_M - V_t)^2}$$

$$\therefore (V_M - V_t)^2 = (V_{DD} - V_t)^2 - K_R (V_M - V_t)^2$$

$$\therefore (V_M - V_t)^2 [1 + K_R] = (V_{DD} - V_t)^2 \quad \sqrt{\quad}$$

$$\therefore V_M - V_t = \frac{V_{DD} - V_t}{\sqrt{1 + K_R}}$$

3 Region III:

It's a short segment which has no importance

Q_N is Triode

Q_P is Triode

and $V_O = V_T$

4 Region IV:

Q_N is Triode, $I_{DN} = K_n [(V_{in} - V_T)V_O - \frac{V_O^2}{2}]$

Q_P is sat., $I_{DP} = \frac{1}{2} K_p [V_{DD} - V_T]^2$

$$I_{DN}(\text{Triode}) = I_{DP}(\text{sat.})$$

$$\therefore K_n [(V_{in} - V_T)V_O - \frac{V_O^2}{2}] = \frac{1}{2} K_p (V_{DD} - V_T)^2$$

$$\therefore V_O = (V_{in} - V_T) - \sqrt{(V_{in} - V_T)^2 - \left(\frac{1}{K_R}\right) (V_{DD} - V_T)^2}$$

9 To find V_{IH} :

$$\frac{dV_O}{dV_{in}} = (1 - 0) - \frac{1}{2} \left[(V_{IH} - V_T)^2 - \left(\frac{1}{K_R}\right) (V_{DD} - V_T)^2 \right]^{-1/2} * 2(V_{IH} - V_T)$$

7

$$-1 = 1 - \frac{1}{2} \left[(V_{IH} - V_t)^2 - \left(\frac{1}{KR}\right) (V_{DD} - V_t)^2 \right]^{\frac{1}{2}} + 2(V_{IH} - V_t)$$

$$V_{IH} = V_t + \frac{2}{\sqrt{3KR}} (V_{DD} - V_t)$$

to Find V_{OL} : (we put $V_{in} = V_{DD}$)

$$\therefore V_O = (V_{in} - V_t) - \sqrt{(V_I - V_t)^2 - \left(\frac{1}{r}\right) (V_{DD} - V_t)^2}$$

$$\therefore V_{OL} = (V_{DD} - V_t) - \sqrt{(V_{DD} - V_t)^2 - \frac{1}{r} (V_{DD} - V_t)^2}$$

$$V_{OL} = (V_{DD} - V_t) \left[1 - \sqrt{1 - \frac{1}{KR}} \right]$$

If the term $\frac{1}{KR} \ll 1$:

$$\therefore V_{OL} = (V_{DD} - V_t) [1 - \sqrt{1}]$$

$$\therefore V_{OL} = 0$$

Static current:

Low state: $V_{in} = V_{DD}$ & $V_O = V_{OL}$

$$I_{DN}(Triode) = I_{DP}(sat.)$$

$$\therefore I_{static} = \frac{1}{2} K_p (V_{DD} - V_t)^2$$

$$\therefore P_{static} = I_{static} * V_{DD}$$

b High state :

$$V_{in} = 0 \quad \& \quad V_o = V_{DD}$$

Q_N is off

Q_P is Triode

$$\therefore I_{DN} = I_{DP} = 0$$

$$\therefore I_{static} = 0$$

$$\therefore P_{static} = 0$$

Dynamic operation :

We will use The average current Method

$$t_{PLH} = \frac{\alpha_p C}{K_p V_{DD}}$$

$$\& \quad \alpha_p = \frac{2}{\left[\frac{7}{4} - 3 \left(\frac{V_t}{V_{DD}} \right) + \left(\frac{V_t}{V_{DD}} \right)^2 \right]}$$

$$t_{PHL} = \frac{\alpha_n C}{K_n V_{DD}}$$

$$\alpha_n = \frac{2}{\left[1 + \frac{3}{4} \left(1 - \frac{1}{K_R} \right) - \left(3 - \frac{1}{K_R} \right) \left(\frac{V_E}{V_{DD}} \right) + \left(\frac{V_E}{V_{DD}} \right)^2 \right]}$$

where $K_R = \frac{K_n}{K_p}$ and If K_R Large, so

we can say $\alpha_n = \alpha_p$

$$t_p = \frac{1}{2} [t_{PHL} + t_{PLH}]$$

Example:

consider a pseudo-NMOS inverter fabricated in a 0,25 μm

CMOS technology, $M_n C_{ox} = 115 \text{ MA/V}^2$, $M_p C_{ox} = 30 \text{ MA/V}^2$

$V_{tn} = -V_{tp} = 0,5$ and $V_{DD} = 2,5V$ and $\left(\frac{W}{L}\right)_n = \frac{0,375}{0,25}$ $\therefore r = 9$

Find:

(a) V_{OH} , V_{OL} , V_{IL} , V_{IH} , V_M , N_{MH} and N_{ML}

(b) $\left(\frac{W}{L}\right)_p$

(c) I_{state} and P_D

(d) t_{PLH} , t_{PHL} and t_p when $c = 7FF$.

(9) * $V_{OH} = V_{DD} = 2,5$

* $V_{OL} = (V_{DD} - V_t) [1 - \sqrt{1 - \frac{1}{r}}]$

∴ $V_{OL} = (2,5 - 0,5) [1 - \sqrt{1 - \frac{1}{9}}] = 0,11 \text{ Volt}$

* $V_{IH} = V_t + \frac{2}{\sqrt{3+r}} (V_{DD} - V_t)$

$V_{IH} = 0,5 + \frac{2}{\sqrt{3+9}} (2,5 - 0,5) = 1,27V$

* $V_M = V_t + \frac{V_{DD} - V_t}{\sqrt{r+1}}$

∴ $V_M = 0,5 + \frac{2,5 - 0,5}{\sqrt{9+1}} = 1,13 \text{ Volt}$

* $NM_H = V_{OH} - V_{IH} = 2,5 - 1,27 = 1,23 \text{ Volt}$

* $NM_L = V_{IL} - V_{OL} = 0,71 - 0,11 = 0,6 \text{ Volt}$

(b)

$\frac{K_n}{K_p} = g$

∴ $\frac{M_n C_{ox} * (\frac{W}{L})_n}{M_p C_{ox} * (\frac{W}{L})_p} = g$

$$\frac{115 * \frac{0,375}{0,25}}{30 * (\frac{W}{L})_p} = 9$$

$$\therefore (W/L)_p = 0,64$$

(c)

$$\begin{aligned} I_{\text{static}} &= \frac{1}{2} K_p (V_{DD} - V_t)^2 \\ &= 0,5 * 30 * 0,64 (2,5 - 0,5)^2 \\ &= 38,4 \text{ } \mu\text{A} \end{aligned}$$

$$P_D = I_{\text{static}} * V_{DD} = 38,4 * 2,5 = 96 \text{ } \mu\text{W}$$

(d)

$$\alpha_p = \frac{2}{\left[\frac{7}{4} - 3 \left(\frac{V_t}{V_{DD}} \right) + \left(\frac{V_t}{V_{DD}} \right)^2 \right]} = 1,68$$

$$\begin{aligned} \therefore t_{PLH} &= \frac{\alpha_p * C}{K_p * V_{DD}} \\ &= \frac{1,68 * 7 * 10^{-15}}{30 * 10^{-6} * 0,64 * 2,5} = 0,25 \text{ ns} \end{aligned}$$

$$\alpha_n = \frac{2}{\left[1 + \frac{3}{4} \left(1 - \frac{1}{r} \right) - \left(3 - \frac{1}{r} \right) \left(\frac{V_t}{V_{DD}} \right) + \left(\frac{V_t}{V_{DD}} \right)^2 \right]} = 1,54$$

$$t_{PHL} = \frac{\alpha_n C}{K_n V_{DD}} = 0,03 \text{ ns} \quad \psi \quad t_p = 0,14 \text{ ns}$$

Example:

Use PSEUDO IMPLEMENT TO DESIGN

(a) NOR Gate (4 input)

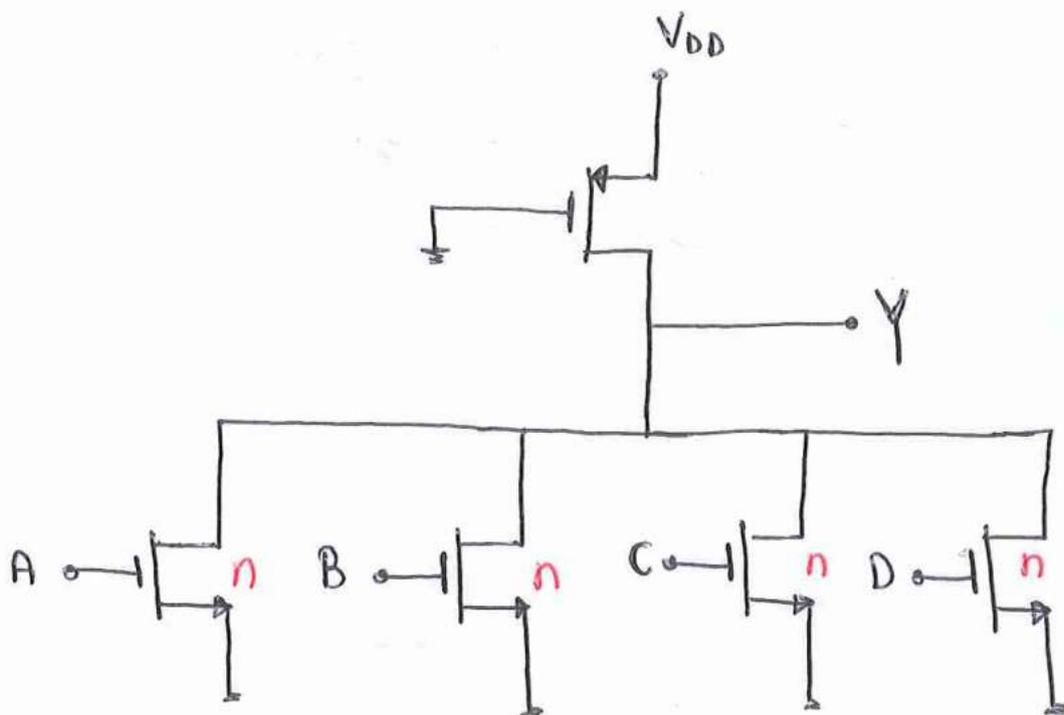
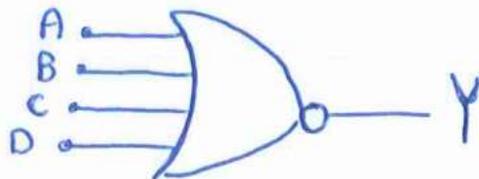
(b) NAND Gate (4 input)

$$(c) \bar{Y} = ABC\bar{C} + CDE + \bar{C}\bar{D}\bar{E}$$

(a)

$$Y = \overline{A+B+C+D}$$

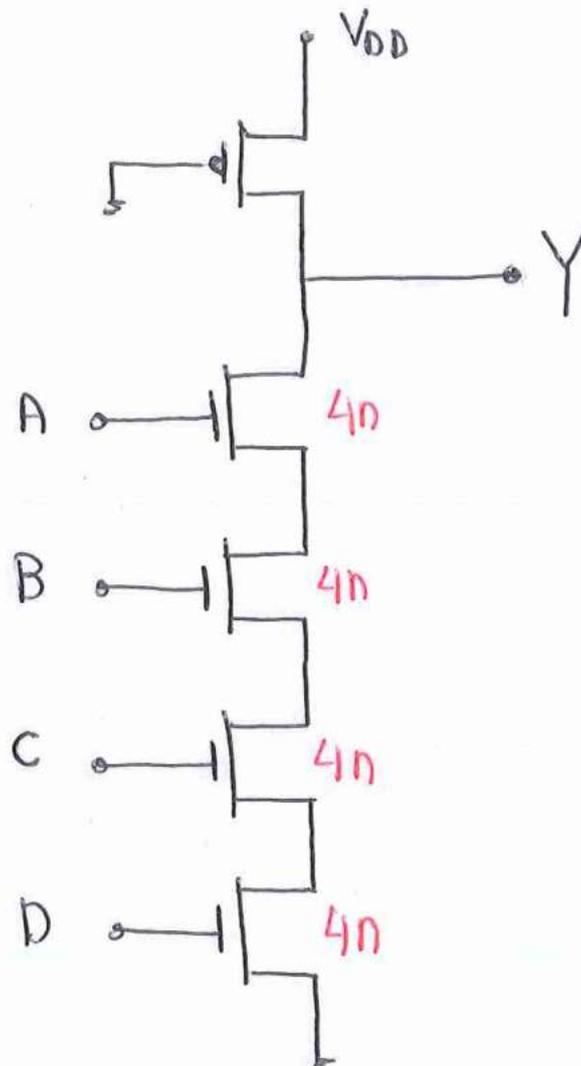
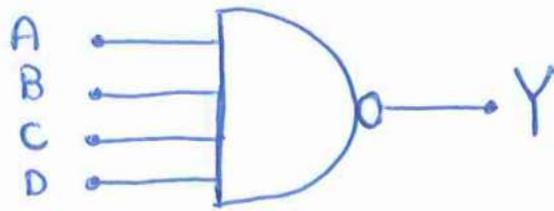
$$\bar{Y} = A+B+C+D$$



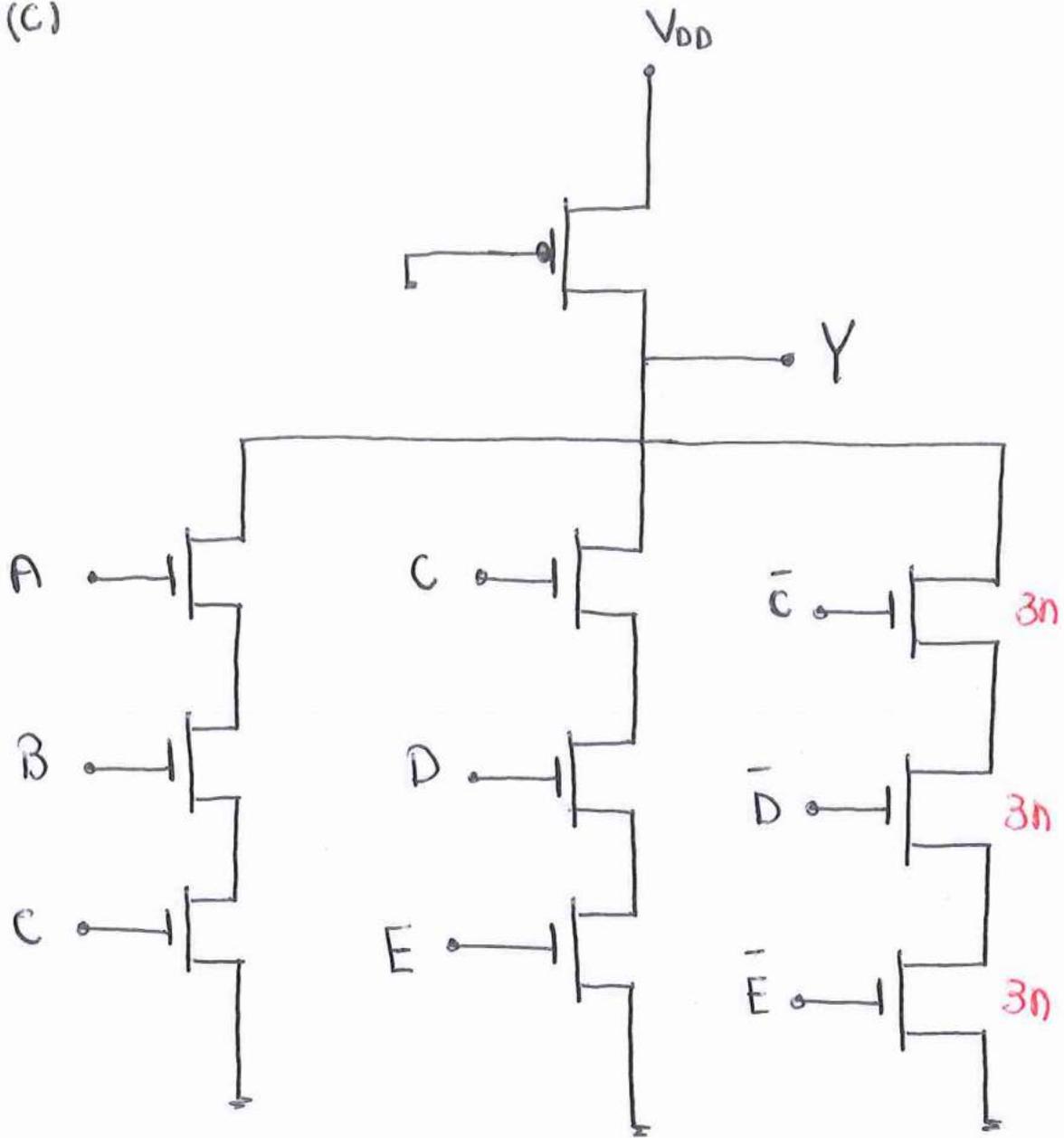
(b)

$$Y = \overline{ABCD}$$

$$\bar{Y} = ABCD$$



(C)



Note That:

For $K_R = \frac{k_n}{k_p}$ High: * (Low V_{OL} & Wide NML)

- * Large gate for $(\frac{w}{L})_p$
- * Large area and current of NMOS
- * Large static current and P_D
- * Low t_p

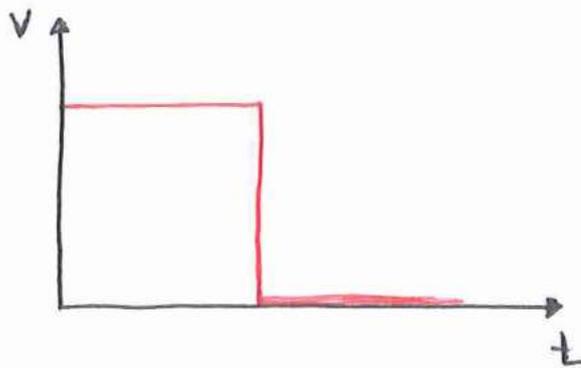
For $K_R = \frac{k_n}{k_p}$ Small: * (Large V_{OL} & Small NML)

- * Small area and capacitance
- * Small $(\frac{w}{L})_p$
- * Small I_{static} and P_D
- * Long t_{PLH}

K_R between 4 and 10

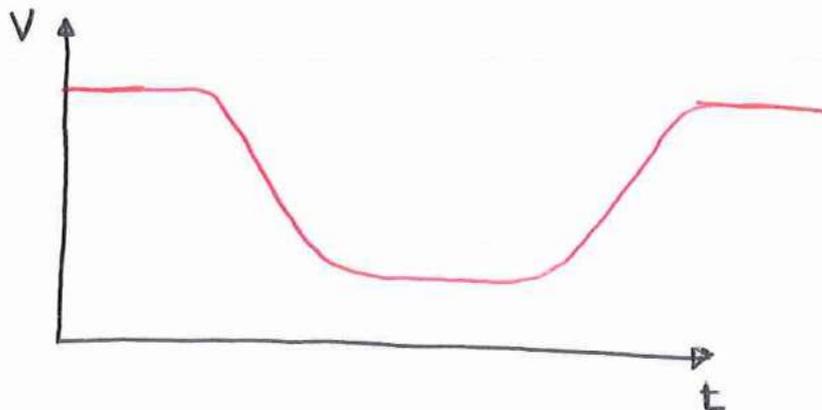


In Ideal inverter:



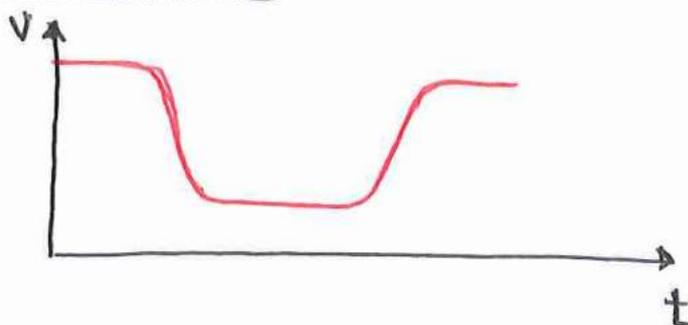
$t_{PHL} = t_{PLH} = 0$

In CMOS inverter:



$P_{static} = 0$

In Pseudo inverter:



$P_{static} \neq 0$



$t_{PHL} < t_{PHL} \text{ CMOS}$
Pseudo CMOS

- ❖ Electronics I
- ❖ Electronics II
- ❖ Electronics III

Example:

In pseudo NMOS inverter $L = 0,25 \mu\text{m}$ technology

$$V_{DD} = 2,5, \quad V_t = 0,4 \text{ V}, \quad \mu_n C_{ox} = 4 \mu_p C_{ox} = 100 \mu\text{A/V}^2$$

$$\left(\frac{W}{L}\right)_n = \frac{0,375}{0,25} \quad \text{and} \quad V_{OL} = 0,1 \text{ V}$$

(a) Find L_p, W_p .

$$V_{OL} = (V_{DD} - V_t) \left[1 - \sqrt{1 - \frac{1}{K_R}} \right]$$

$$0,1 = (2,5 - 0,4) \left[1 - \sqrt{1 - \frac{1}{K_R}} \right]$$

$$\therefore K_R = 10,756 = \frac{\mu_n C_{ox} \left(\frac{W}{L}\right)_n}{\mu_p C_{ox} \left(\frac{W}{L}\right)_p}$$

$$\therefore 10,756 = \frac{4 \left(\frac{0,375}{0,25}\right)}{\left(\frac{W}{L}\right)_p}$$

$$\therefore \left(\frac{W}{L}\right)_p = 0,557 < 1$$

$$\therefore W_p < L_p$$

$$\therefore L_p \neq L_{pmin}$$

$$\therefore WP = LP_{\min} = 0,25 \mu\text{m}$$

$$\therefore LP = \frac{0,25}{0,557} = 0,448 \mu\text{m}$$

$$\therefore \left(\frac{W}{L}\right)_p = \frac{0,25 \mu\text{m}}{0,448 \mu\text{m}}$$

$$\square \text{ If } \left(\frac{W}{L}\right) > 1$$

$$\therefore \left(\frac{W}{L}\right)_p = 2,5$$

$$WP = 2,5 LP$$

$$\therefore LP = L_{\min} = 0,25$$

$$\therefore WP = 0,625$$

$$\therefore \left(\frac{W}{L}\right)_p = \frac{0,625}{0,25}$$

(b) Find Power in Low and high state.

in High state:

$$V_{in} = 0$$

$$Q_n \longrightarrow \text{off} \quad I_{DN} = 0$$

$$\therefore P_{\text{static}} = 0$$

In Low State:

$$I_{DN} = I_{DP \text{ sat.}}$$

I_{node}

$$I_{DP \text{ sat.}} = \frac{1}{2} K_P (V_{DD} - V_T)^2$$

$$= \frac{1}{2} * \frac{100}{4} \left(\frac{0,25}{0,448} \right) (2,5 - 0,4)^2$$

$$= 30,7617 \mu A$$

$$P_{stat.} = V_{DD} * I_{stat.}$$

$$= 77 \mu W$$

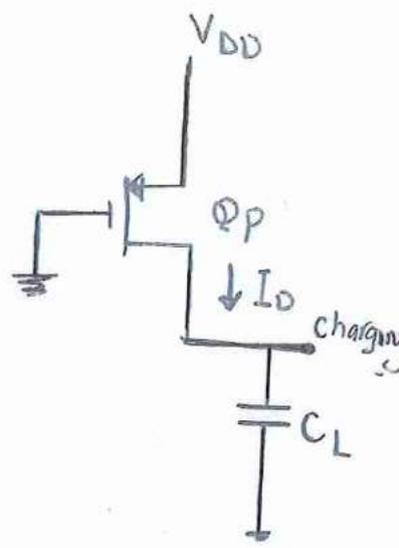
Dynamic operation (Propagation Delay):

(charging)

a) Low to High t_{PLH} :

$V_{in} = \text{Low}$ Q_N off

and C_L charging through Q_P



* $I_p(0)$ In saturation

$$V_{SG} = V_{DD} \quad \& \quad V_{SD} = V_{DD}$$

* $I_p(t_{PLH})$ in Linear

$$V_{SG} = V_{DD} \quad \& \quad V_{SD} = \frac{V_{DD}}{2}$$

∴ Average current charging

$$* I_{ave} = \frac{I_p(0) + I_p(t_{PLH})}{2}$$

$$* t_{PLH} = \frac{C_L * (V_{DD} - \frac{V_{DD}}{2})}{I_{ave}}$$

$$t_{PLH} = \frac{C_L * (\frac{V_{DD}}{2})}{I_{ave}}$$

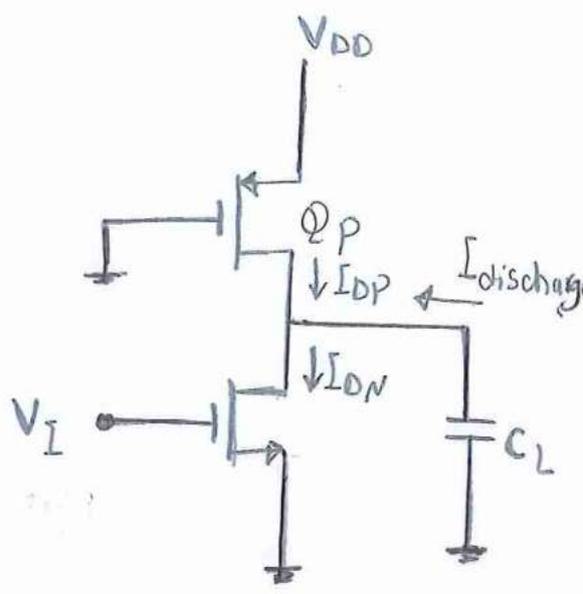
b High to Low (t_{PHL}):

Q_N & Q_P are ON

I_{Discharge} = I_{DN} - I_{DP}

I_{Discharge}(0) = I_{DN}(0) - I_{DP}(0)

I_{Discharge}(t_{PHL}) = I_{DN}(t_{PHL}) - I_{DP}(t_{PHL})



- at t=0 : (V_o = V_{DD})
 - Q_N → Sat.
 - Q_P → Linear

- at t = t_{PHL} : (V_o = V_{DD}/2)
 - Q_N → Linear
 - Q_P → Linear

* t_{PLH} > t_{PHL} → K_n > K_p