UNIT 8

FIELD-EFFECT TRANSISTORS (FETs)

8–1 ■ THE JUNCTION FIELD-EFFECT TRANSISTOR (JFET)

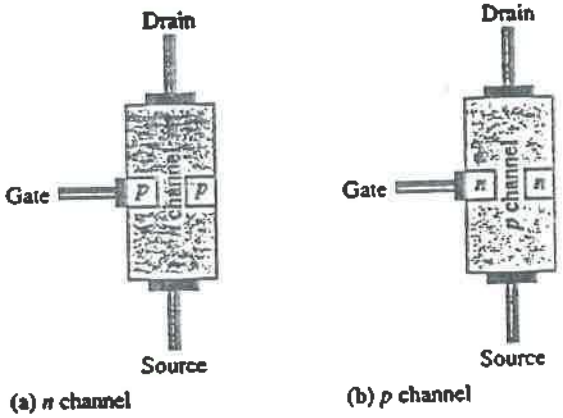
The junction field-effect transistor (JFET) is a type of FET that operates with a reverse-biased junction to control current in a channel. Depending on their structure, JFETs fall into either of two categories, n channel or p channel.

After completing this section, you should be able to

- **Explain the operation of JFETs**
  - ☐ Identify the three terminals of a JFET
  - ☐ Explain what a channel is
  - ☐ Describe the structural difference between an *n*-channel JFET and a *p*-channel JFET
  - ☐ Discuss how voltage controls the current in a JFET
  - ☐ Identify the symbols for *n*-channel and *p*-channel JFETs

Figure 8–1(a) shows the basic structure of an *n*-channel junction field-effect transistor (JFET). Wire leads are connected to each end of the *n*-channel; the drain is at the upper end, and the source is at the lower end. Two *p*-type regions are diffused in the *n*-type material to form a channel, and both *p*-type regions are connected to the gate lead. For simplicity, the gate lead is shown connected to only one of the *p* regions. A *p*-channel JFET is shown in Figure 8–1(b).

FIGURE 8–1
A representation of the basic structure of the two types of JFET.



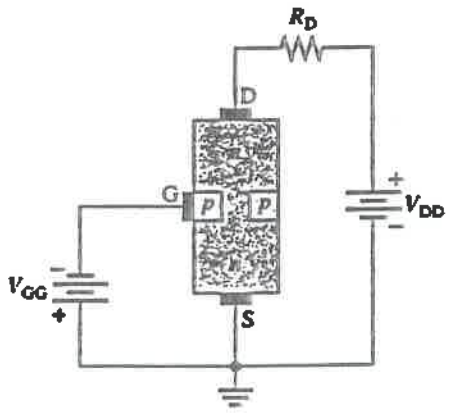
Basic Operation

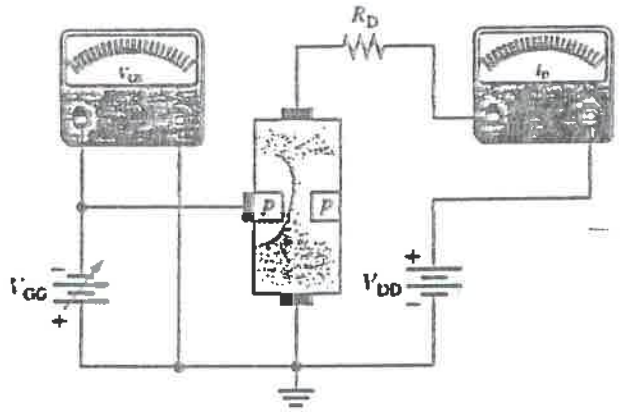
To illustrate the operation of a JFET, Figure 8–2 shows bias voltages applied to an *n*-channel device. V_{DD} provides a drain-to-source voltage and supplies current from drain to source. V_{GG} sets the reverse-bias voltage between the gate and the source, as shown.

The JFET is *always* operated with the gate-source *pn* junction reverse-biased. Reverse-biasing of the gate-source junction with a negative gate voltage produces a depletion region along the *pn* junction, which extends into the *n* channel and thus increases its resistance by restricting the channel width.

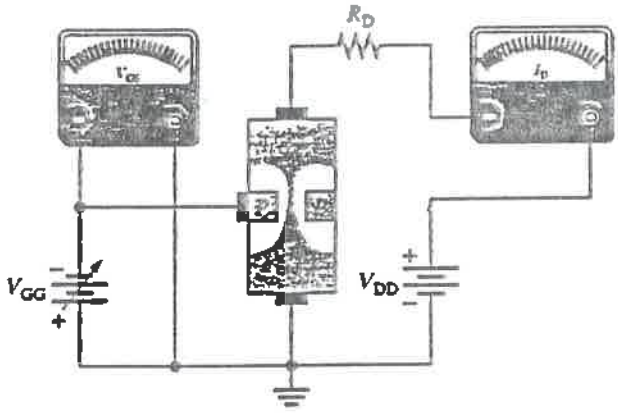
The channel width can be controlled by varying the gate voltage, whereby the amount of drain current, I_D, can also be controlled. Figure 8–3 illustrates this concept. The white areas represent the depletion region created by the reverse bias. It is wider

FIGURE 8–2
A biased n-channel JFET.

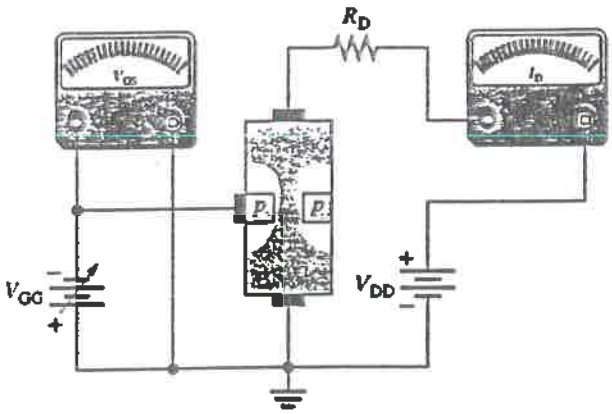




(a) JFET biased for conduction



(b) Greater V_{GG} narrows the channel and decreases I_D.



(c) Less V_{GG} widens the channel and increases I_D.

FIGURE 8–3
Effects of V_{GS} on channel width and on drain current ($V_{GG} = V_{GS}$).

toward the drain end of the channel because the reverse-bias voltage between the gate and the drain is greater than that between the gate and the source. We will discuss JFET characteristic curves and some important parameters in Section 8–2.

JFET Symbols

The schematic symbols for both *n*-channel and *p*-channel JFETs are shown in Figure 8–4. Notice that the arrow on the gate points "in" for *n* channel and "out" for *p* channel.

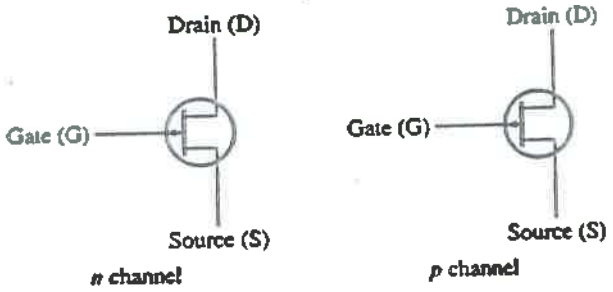


FIGURE 8–4
JFET schematic symbols.

SECTION 8–1 REVIEW

1. Name the three terminals of a JFET.
2. Does an *n*-channel JFET require a positive or negative value for V_{GS}?
3. How is the drain current controlled in a JFET?

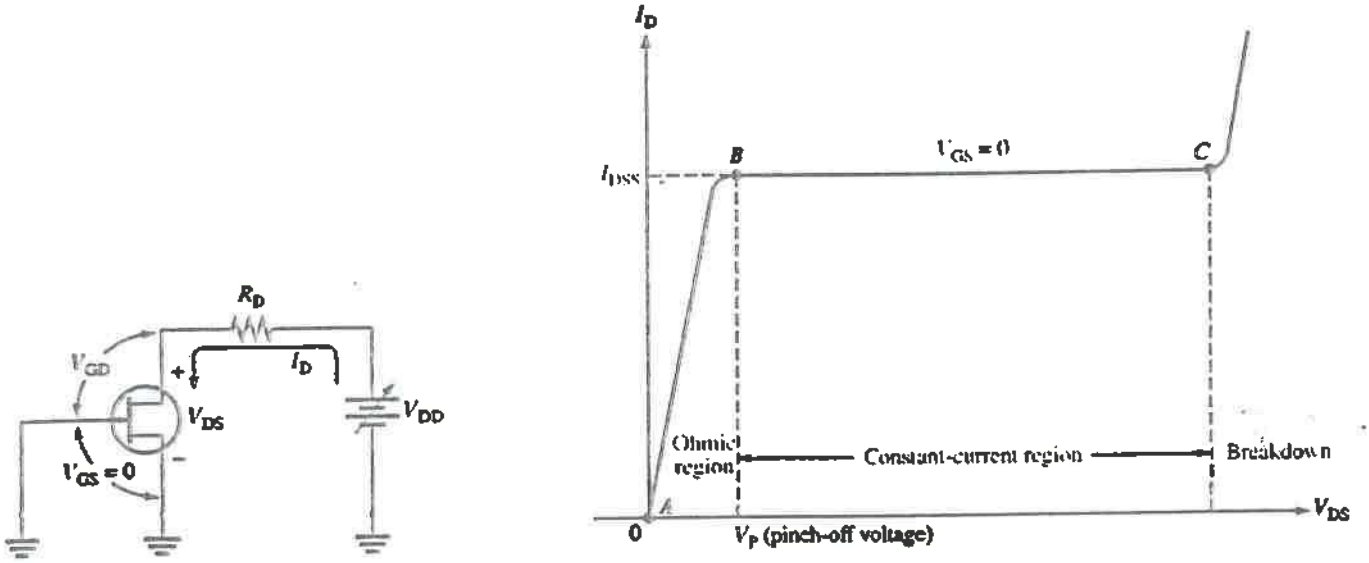
8–2 ■ JFET CHARACTERISTICS AND PARAMETERS

In this section, you will see how the JFET operates as a voltage-controlled, constant-current device. You will also learn about cutoff and pinch-off as well as JFET transfer characteristics.

After completing this section, you should be able to

■ Define, discuss, and apply important JFET parameters
- ☐ Explain ohmic region, constant-current region, and breakdown
- ☐ Define *pinch-off voltage*
- ☐ Describe how gate-to-source voltage controls the drain current
- ☐ Define *cutoff voltage*
- ☐ Compare pinch-off and cutoff
- ☐ Analyze a JFET transfer characteristic curve
- ☐ Use the equation for the transfer characteristic to calculate I_D
- ☐ Use a JFET data sheet
- ☐ Define *transconductance*
- ☐ Explain and determine input resistance and capacitance
- ☐ Determine drain-to-source resistance

First, let's consider the case where the gate-to-source voltage is zero ($V_{GS} = 0$ V). This is produced by shorting the gate to the source, as in Figure 8–5(a) where both are grounded. As V_{DD} (and thus V_{DS}) is increased from zero, I_D will increase proportionally through the *n*-type material, as shown in the graph of Figure 8–5(b) between points *A* and *B*. In this region, the channel resistance is essentially constant because the depletion region is not large enough to have significant effect. This is called the *ohmic region* because V_{DS} and I_D are related by Ohm's law.



(a) JFET with $V_{GS} = 0$ V and a variable V_{DS} (V_{DD})

(b) Drain characteristic

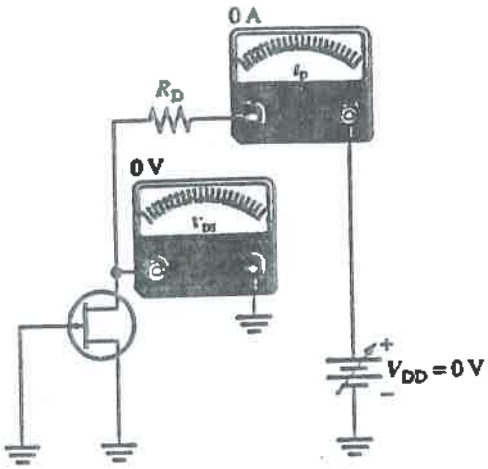
FIGURE 8–5
The drain characteristic curve of a JFET for $V_{GS} = 0$ showing pinch-off.

At point *B* in Figure 8–5(b), the curve levels off and I_D becomes essentially constant. As V_{DS} increases from point *B* to point *C*, the reverse-bias voltage from gate to drain (V_{GD}) produces a depletion region large enough to offset the increase in V_{DS}, thus keeping I_D relatively constant.

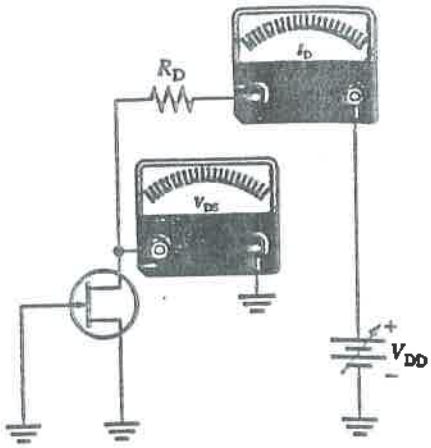
Pinch-Off Voltage

For $V_{GS} = 0$ V, the value of V_{DS} at which I_D becomes essentially constant (point *B* on the curve in Figure 8–5(b)) is the **pinch-off voltage, V_P**. For a given JFET, V_P has a fixed value. As you can see, a continued increase in V_{DS} above the pinch-off voltage produces an almost constant drain current. This value of drain current is I_{DSS} (*D*rain to *S*ource current with gate *S*horted) and is always specified on JFET data sheets. I_{DSS} is the *maximum* drain current that a specific JFET can produce regardless of the external circuit, and it is always specified for the condition, $V_{GS} = 0$ V.

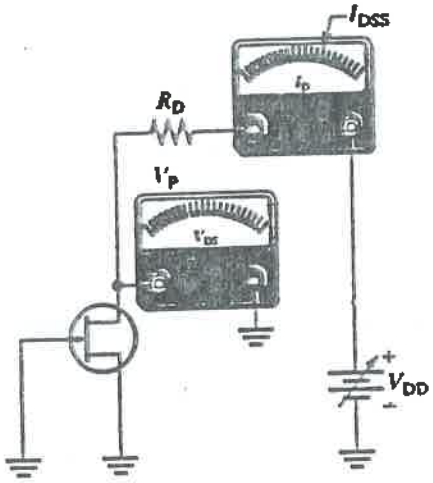
As shown in the graph in Figure 8–5(b), *breakdown* occurs at point *C* when I_D begins to increase very rapidly with any further increase in V_{DS}. Breakdown can result in irreversible damage to the device, so JFETs are always operated below breakdown and



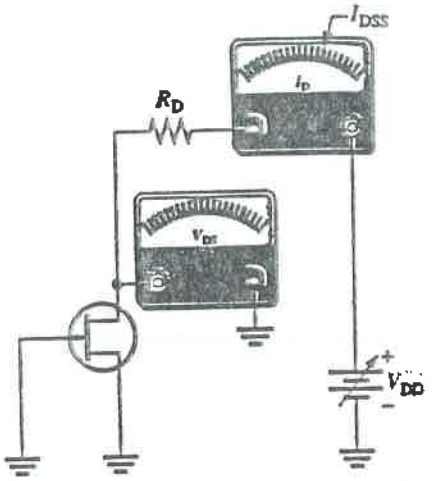
(a) When $V_{DS} = 0$, $I_D = 0$.



(b) I_D increases proportionally with V_{DS} in the ohmic region.



(c) When $V_{DS} = V_P$, $I_D = I_{DSS}$.



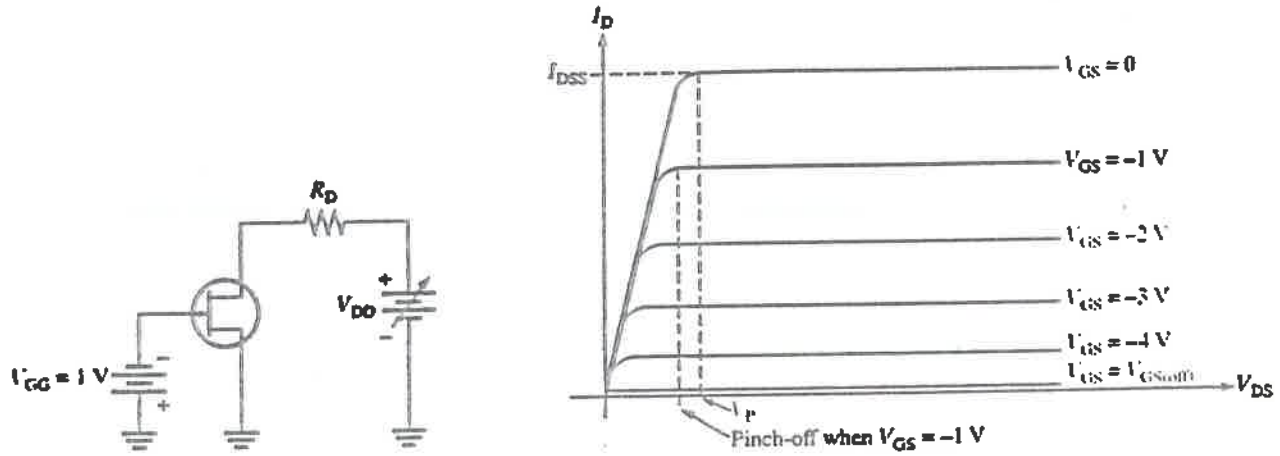
(d) As V_{DS} increases further, I_D remains at I_{DSS} unless breakdown occurs.

FIGURE 8–6
JFET action that produces the characteristic curve for $V_{GS} = 0$ V.

within the *constant-current region* (between points *B* and *C* on the graph). The JFET action that produces the drain characteristic curve to the point of breakdown for $V_{GS} = 0$ V is illustrated in Figure 8–6.

V_{GS} Controls I_D

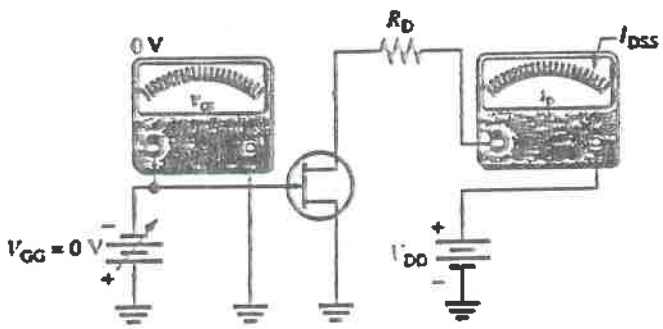
Now, let's connect a bias voltage, V_{GG}, from gate to source as shown in Figure 8–7(a). As V_{GS} is set to increasingly more negative values by adjusting V_{GG}, a family of drain characteristic curves is produced, as shown in Figure 8–7(b). Notice that I_D decreases as the magnitude of V_{GS} is increased to larger negative values because of the narrowing of the channel. Also notice that, for each increase in V_{GS}, the JFET reaches pinch-off (where constant current begins) at values of V_{DS} less than V_P. So, the amount of drain current is controlled by V_{GS}, as illustrated in Figure 8–8.



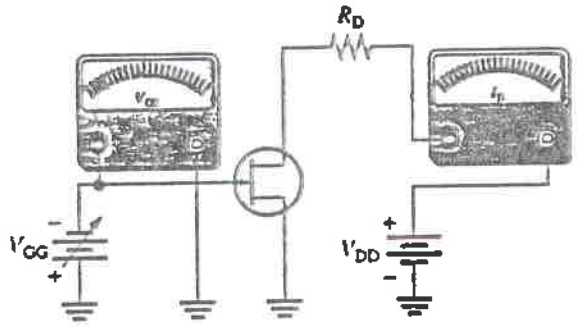
(a) JFET biased at $V_{GS} = -1$ V

(b) Family of drain characteristic curves

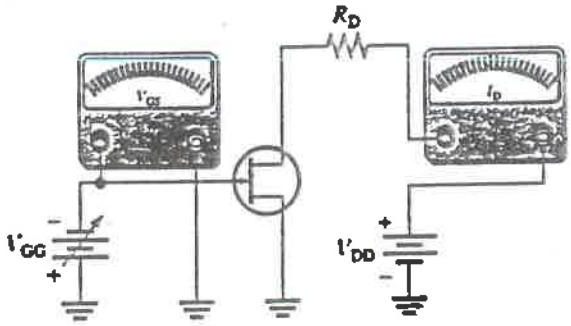
FIGURE 8–7
Pinch-off occurs at a lower V_{DS} as V_{GS} is increased to more negative values.



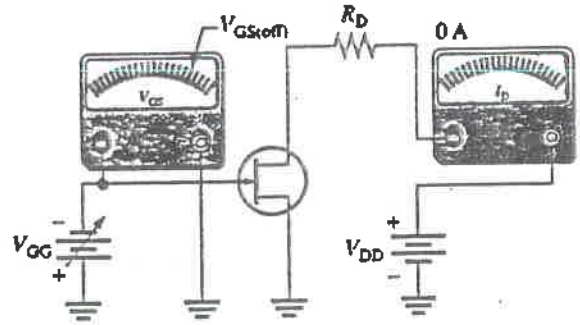
(a) $V_{GS} = 0$ V, $I_D = I_{DSS}$



(b) V_{GS} negative, I_D decreases



(c) I_D continues to decrease as V_{GS} is made more negative.



(d) I_D continues to decrease until $V_{GS} = -V_{GS(off)}$, where it becomes zero.

FIGURE 8–8
V_{GS} controls I_D.

Cutoff Voltage

The value of V_{GS} that makes I_D approximately zero is the cutoff voltage, $V_{GS(off)}$. The JFET must be operated between $V_{GS} = 0$ V and $V_{GS(off)}$. For this range of gate-to-source voltages, I_D will vary from a maximum of I_{DSS} to a minimum of almost zero.

As you have seen, for an *n*-channel JFET, the more negative V_{GS} is, the smaller I_D becomes in the constant-current region. When V_{GS} has a sufficiently large negative value, I_D is reduced to zero. This cutoff effect is caused by the widening of the depletion region to a point where it completely closes the channel as shown in Figure 8–9.

The basic operation of a *p*-channel JFET is the same as for an *n*-channel device except that a *p*-channel JFET requires a negative V_{DD} and a positive V_{GS}, as illustrated in Figure 8–10.

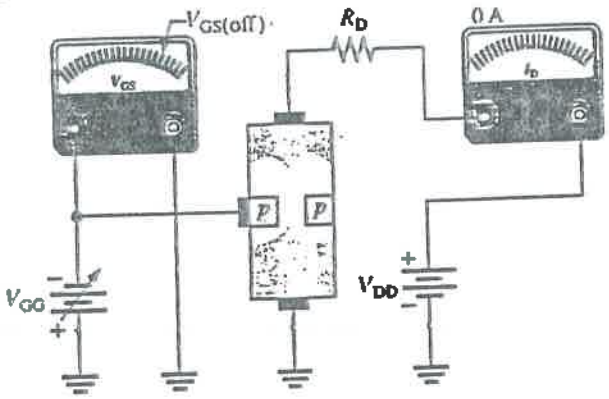


FIGURE 8–9
JFET at cutoff.

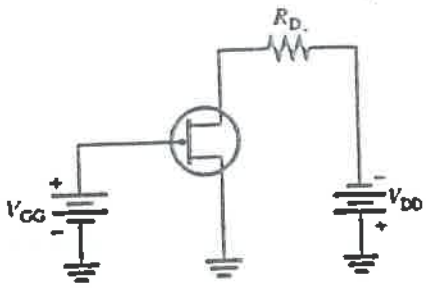


FIGURE 8–10
A biased p-channel JFET.

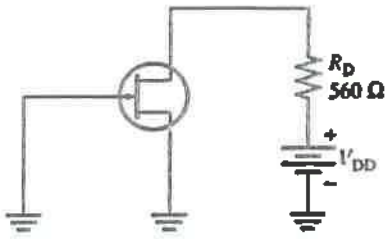
Comparison of Pinch-Off and Cutoff

As you have seen, there is definitely a difference between pinch-off and cutoff. There is also a connection. V_P is the value of V_{DS} at which the drain current becomes constant and is always measured at $V_{GS} = 0$ V. However, pinch-off occurs for V_{DS} values less than V_P when V_{GS} is nonzero. So, although V_P is a constant, the minimum value of V_{DS} at which I_D becomes constant varies with V_{GS}.

$V_{GS(off)}$ and V_P are always equal in magnitude but opposite in sign. A data sheet usually will give either $V_{GS(off)}$ or V_P, but not both. However, when you know one, you have the other. For example, if $V_{GS(off)} = -5$ V, then $V_P = +5$ V.

EXAMPLE 8–1 For the JFET in Figure 8–11, $V_{GS(off)} = -4$ V and $I_{DSS} = 12$ mA. Determine the *minimum* value of V_{DD} required to put the device in the constant-current region of operation.

FIGURE 8–11



Solution Since $V_{GS(off)} = -4$ V, $V_P = 4$ V. The minimum value of V_{DS} for the JFET to be in its constant-current region is

$$V_{DS} = V_P = 4 \text{ V}$$

In the constant-current region with $V_{GS} = 0$ V.

$$I_D = I_{DSS} = 12 \text{ mA}$$

The drop across the drain resistor is

$$V_{R_D} = I_D R_D = (12 \text{ mA})(560 \ \Omega) = 6.72 \text{ V}$$

Apply Kirchhoff's law around the drain circuit.

$$V_{DD} = V_{DS} + V_{R_D} = 4 \text{ V} + 6.72 \text{ V} = 10.7 \text{ V}$$

This is the value of V_{DD} to make $V_{DS} = V_P$ and put the device in the constant-current region.

Related Exercise If V_{DD} is increased to 15 V, what is the drain current?

EXAMPLE 8–2 A particular *p*-channel JFET has a $V_{GS(off)} = +4$ V. What is I_D when $V_{GS} = +6$ V?

Solution The *p*-channel JFET requires a positive gate-to-source voltage. The more positive the voltage, the less the drain current. When $V_{GS} = 4$ V, I_D is 0. Any further increase in V_{GS} keeps the JFET cut off, so I_D remains 0.

Related Exercise What is V_P for the JFET described in this example?

JFET Transfer Characteristic

You have learned that a range of V_{GS} values from zero to $V_{GS(off)}$ controls the amount of drain current. For an *n*-channel JFET, $V_{GS(off)}$ is negative, and for a *p*-channel JFET, $V_{GS(off)}$ is positive. Because V_{GS} does control I_D, the relationship between these two quantities is very important. Figure 8–12 is a typical transfer characteristic curve that illustrates graphically the relationship between V_{GS} and I_D.

Notice that the bottom end of the curve is at a point on the V_{GS} axis equal to $V_{GS(off)}$, and the top end of the curve is at a point on the I_D axis equal to I_{DSS}. This curve, of course, shows that the operating limits of a JFET are

$$I_D = 0 \quad \text{when } V_{GS} = V_{GS(off)}$$

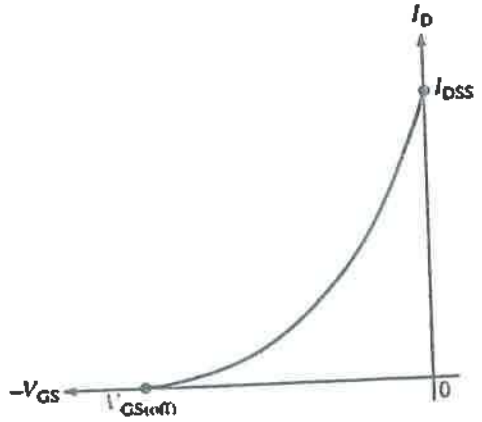


FIGURE 8–12
JFET transfer characteristic curve (n-channel).

and

$$I_D = I_{DSS} \quad \text{when } V_{GS} = 0$$

The transfer characteristic curve can be developed from the drain characteristic curves by plotting values of I_D for the values of V_{GS} taken from the family of drain curves in the pinch-off region, as illustrated in Figure 8–13 for a specific set of curves. Each point on the transfer characteristic curve corresponds to specific values of V_{GS} and I_D on the drain curves. For example, when $V_{GS} = -2$ V, $I_D = 4.32$ mA. Also, for this specific JFET, $V_{GS(off)} = -5$ V and $I_{DSS} = 12$ mA.

A JFET transfer characteristic curve is nearly parabolic in shape and can therefore be expressed approximately as

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 \tag{8–1}$$

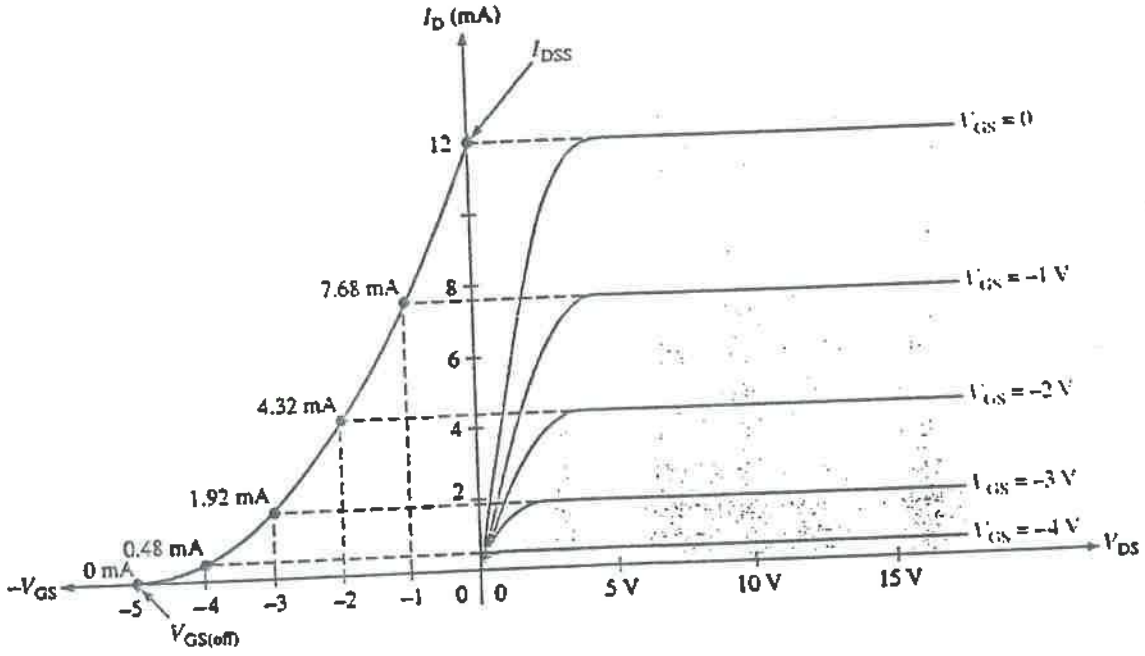


FIGURE 8–13
Example of the development of an n-channel JFET transfer characteristic curve (left) from the JFET drain characteristic curves (right).

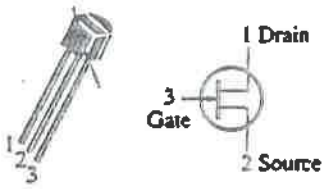
With Equation (8–1), I_D can be determined for any V_{GS} if $V_{GS(off)}$ and I_{DSS} are known. These quantities are usually available from the data sheet for a given JFET. Notice the squared term in the equation. Because of its form, a parabolic relationship is known as a *square law*, and therefore, JFETs and MOSFETs are often referred to as *square-law devices*.

The data sheet for a typical JFET series is shown in Figure 8–14.

FIGURE 8–14
JFET data sheet.

2N5457
thru
2N5459

Case 29-04, Style 5
TO-92 (TO-226AA)



JFETs
General Purpose

***N* channel — Depletion**

Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source voltage	V_{DS}	25	V dc
Drain-Gate voltage	V_{DG}	25	V dc
Reverse gate-source voltage	V_{GSR}	−25	V dc
Gate current	I_G	10	mA dc
Total device dissipation @ T_A = 25°C Derate above 25°C	P_D	310 2.82	mW mW/°C
Junction temperature	T_J	125	°C
Storage channel temperature range	T_{stg}	−65 to +150	°C

Electrical Characteristics (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF Characteristics						
Gate-Source breakdown voltage (I_G = −10 μA dc, V_{DS} = 0)		$V_{(BR)GSS}$	−25	–	–	V dc
Gate reverse current (V_{GS} = −15 V dc, V_{DS} = 0) (V_{GS} = −15 V dc, V_{DS} = 0, T_A = 100°C)		I_{GSS}	– –	– –	−1.0 −200	nA dc
Gate-Source cutoff voltage (V_{DS} = 15 V dc, I_D = 10 nA dc)	2N5457 2N5458 2N5459	$V_{GS(off)}$	−0.5 −1.0 −2.0	– – –	−6.0 −7.0 −8.0	V dc
Gate-Source voltage (V_{DS} = 15 V dc, I_D = 100 μA dc) (V_{DS} = 15 V dc, I_D = 200 μA dc) (V_{DS} = 15 V dc, I_D = 400 μA dc)	2N5457 2N5458 2N5459	V_{GS}	– – –	−2.5 −3.5 −4.5	– – –	V dc
ON Characteristics						
Zero-Gate-Voltage drain current (V_{DS} = 15 V dc, V_{GS} = 0)	2N5457 2N5458 2N5459	I_{DSS}	1.0 2.0 4.0	3.0 6.0 9.0	5.0 9.0 16	mA dc
Small-signal Characteristics						
Forward transfer admittance common source (V_{DS} = 15 V dc, V_{GS} = 0, f = 1.0 kHz)	2N5457 2N5458 2N5459	$\lvert y_{fs}\rvert$	1000 1500 2000	– – –	5000 5500 6000	μmhos or μS
Output admittance common source (V_{DS} = 15 V dc, V_{GS} = 0, f = 1.0 kHz)		$\lvert y_{os}\rvert$	–	10	50	μmhos or μS
Input capacitance (V_{DS} = 15 V dc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	–	4.5	7.0	pF
Reverse transfer capacitance (V_{DS} = 15 V dc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	–	1.5	3.0	pF

EXAMPLE 8–3

The data sheet in Figure 8–14 for a 2N5459 JFET indicates that typically $I_{DSS} = 9$ mA and $V_{GS(off)} = -8$ V (maximum). Determine the drain current for $V_{GS} = 0$ V, −1 V, and −4 V.

Solution For $V_{GS} = 0$ V, $I_D = I_{DSS} = 9$ mA. For $V_{GS} = -1$ V, use Equation (8–1).

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (9\text{ mA})\left(1 - \frac{-1\text{ V}}{-8\text{ V}}\right)^2$$
$$= (9\text{ mA})(1 - 0.125)^2 = (9\text{ mA})(0.766) = 6.89\text{ mA}$$

For $V_{GS} = -4$ V:

$$I_D = (9\text{ mA})\left(1 - \frac{-4\text{ V}}{-8\text{ V}}\right)^2 = (9\text{ mA})(1 - 0.5)^2 = (9\text{ mA})(0.25) = 2.25\text{ mA}$$

Related Exercise Determine I_D for $V_{GS} = -3$ V for the 2N5459 JFET.

JFET Forward Transconductance

The forward transfer conductance (transconductance), g_m, is the change in drain current (ΔI_D) for a given change in gate-to-source voltage (ΔV_{GS}) with the drain-to-source voltage constant. It is expressed as a ratio and has the unit of siemens (S).

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

Other common designations for this parameter are g_{fs} and y_{fs} (forward transfer admittance). As you will see in Chapter 9, g_m is important in FET amplifiers as a major factor in determining the voltage gain.

Because the transfer characteristic curve for a JFET is nonlinear, g_m varies in value depending on the location on the curve as set by V_{GS}. The value for g_m is greater near the top of the curve (near $V_{GS} = 0$) than it is near the bottom (near $V_{GS(off)}$), as illustrated in Figure 8–15. A data sheet normally gives the value of g_m measured at $V_{GS} = 0$ V (g_{m0}). For example, the data sheet for the 2N5457 JFET specifies a minimum g_{m0} (y_{fs}) of 1000 μS with $V_{DS} = 15$ V.

Given g_{m0}, you can calculate an approximate value for g_m at any point on the transfer characteristic curve using the following formula:

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) \tag{8–2}$$

When a value of g_{m0} is not available, you can calculate it using values of I_{DSS} and $V_{GS(off)}$. The vertical lines indicate an absolute value (no sign).

$$g_{m0} = \frac{2I_{DSS}}{|V_{GS(off)}|} \tag{8–3}$$

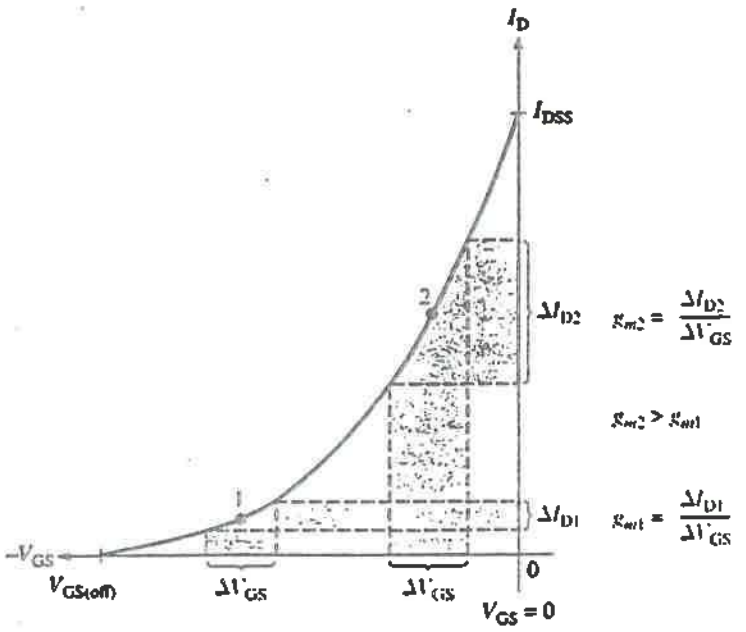


FIGURE 8–15
g_m varies depending on the bias point (V_{GS}).

EXAMPLE 8–4

The following information is included on the data sheet in Figure 8–14 for a 2N5457 JFET: typically, I_{DSS} = 3.0 mA, $V_{GS(off)}$ = –6 V maximum, and $y_{fs(max)}$ = 5000 μS. Determine the forward transconductance for V_{GS} = –4 V, and find I_D at this point.

Solution $g_{m0} = y_{fs} = 5000\ \mu S$. Use Equation (8–2) to calculate g_m.

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) = (5000\ \mu S)\left(1 - \frac{-4\ V}{-6\ V}\right) = 1667\ \mu S$$

Next, use Equation (8–1) to calculate I_D at V_{GS} = –4 V.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (3.0\ mA)\left(1 - \frac{-4\ V}{-6\ V}\right)^2 = 333\ \mu A$$

Related Exercise A given JFET has the following characteristics: I_{DSS} = 12 mA, $V_{GS(off)}$ = –5 V, and g_{m0} = 3000 μS. Find g_m and I_D when V_{GS} = –2 V.

Input Resistance and Capacitance

A JFET operates with its gate-source junction reverse-biased. Therefore, the input resistance at the gate is very high. This high input resistance is one advantage of the JFET over the bipolar transistor. (Recall that a bipolar transistor operates with a forward-biased base-emitter junction.) JFET data sheets often specify the input resistance by giving a

value for the gate reverse current I_{GSS} at a certain gate-to-source voltage. The input resistance can then be determined using the following equation:

$$R_{IN} = \left| \frac{V_{GS}}{I_{GSS}} \right| \tag{8–4}$$

For example, the 2N5457 data sheet in Figure 8–14 lists a maximum I_{GSS} of 1 nA for $V_{GS} = -15$ V at 25°C. I_{GSS} increases with temperature, so the input resistance decreases.

The input capacitance, C_{iss}, is a result of the JFET operating with a reverse-biased *pn* junction. Recall that a reverse-biased *pn* junction acts as a capacitor whose capacitance depends on the amount of reverse voltage. For example, the 2N5457 has a maximum C_{iss} of 7 pF for $V_{GS} = 0$.

EXAMPLE 8–5

A certain JFET has an I_{GSS} of 2 nA for $V_{GS} = -20$ V. Determine the input resistance.

Solution

$$R_{IN} = \left| \frac{V_{GS}}{I_{GSS}} \right| = \frac{20\text{ V}}{2\text{ nA}} = 10{,}000\text{ M}\Omega$$

Related Exercise Determine the minimum input resistance for the 2N5458 from the data sheet in Figure 8–14.

Drain-to-Source Resistance

You learned from the drain characteristic curve that, above pinch-off, the drain current is relatively constant over a range of drain-to-source voltages. Therefore, a large change in V_{DS} produces only a very small change in I_D. The ratio of these changes is the drain-to-source resistance of the device, r'_{ds}.

$$r'_{ds} = \frac{\Delta V_{DS}}{\Delta I_D}$$

Data sheets often specify this parameter as output conductance, g_{os}, or output admittance, y_{os}.

SECTION 8–2 REVIEW

1. The drain-to-source voltage at the pinch-off point of a particular JFET is 7 V. If the gate-to-source voltage is zero, what is V_P?
2. The V_{GS} of a certain *n*-channel JFET is increased negatively. Does the drain current increase or decrease?
3. What value must V_{GS} have to produce cutoff in a *p*-channel JFET with a $V_P = -3$ V?

8–3 ■ JFET BIASING

Using some of the FET parameters discussed in the previous sections, we will now see how to dc-bias JFETs. The purpose of biasing is to select the proper dc gate-to-source voltage to establish a desired value of drain current and, thus, a proper Q-point. You will learn about two major types of bias circuits, self-bias and voltage-divider bias.

After completing this section, you should be able to

- **Discuss and analyze JFET bias circuits**
  - ☐ Describe self-bias
  - ☐ Analyze a self-biased JFET circuit
  - ☐ Set the self-biased Q-point
  - ☐ Analyze a voltage-divider-biased JFET circuit
  - ☐ Use transfer characteristic curves to analyze JFET bias circuits
  - ☐ Discuss Q-point stability

Self-Bias

Recall that a JFET must be operated such that the gate-source junction is always reverse-biased. This condition requires a negative V_{GS} for an *n*-channel JFET and a positive V_{GS} for a *p*-channel JFET. This can be achieved using the self-bias arrangements shown in Figure 8–16. The gate resistor, R_G, does not affect the bias because it has essentially no voltage drop across it; and therefore the gate remains at 0 V. R_G is necessary only to isolate an ac signal from ground in amplifier applications, as you will see later.

For the *n*-channel JFET in Figure 8–16(a), I_S produces a voltage drop across R_S and makes the source positive with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then $V_S = I_D R_S$. The gate-to-source voltage is

$$V_{GS} = V_G - V_S = 0 - I_D R_S$$

so

$$V_{GS} = -I_D R_S \tag{8–5}$$

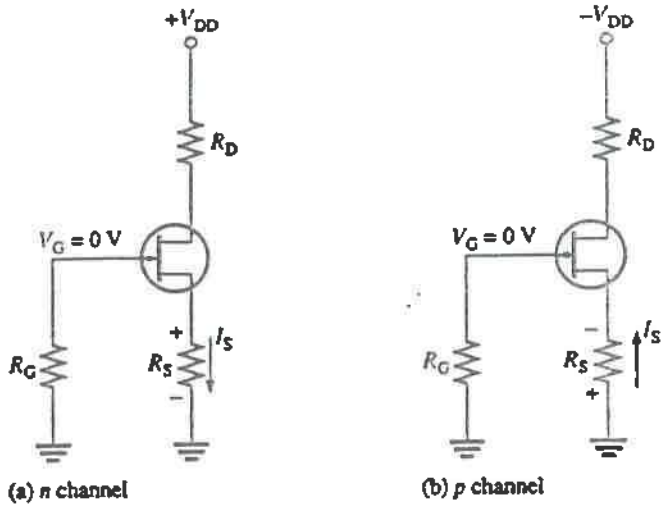


FIGURE 8–16
Self-biased JFETs ($I_S = I_D$ in all FETs).

For the *p*-channel JFET shown in Figure 8–16(b), the current through R_S produces a negative voltage at the source and therefore

$$V_{GS} = +I_D R_S \tag{8–6}$$

In the following analysis, the *n*-channel JFET in Figure 8–16(a) is used for illustration. Keep in mind that analysis of the *p*-channel JFET is the same except for opposite-polarity voltages. The drain voltage with respect to ground is determined as follows:

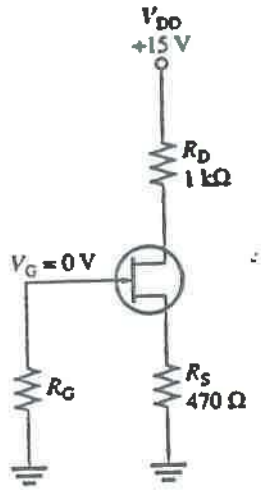
$$V_D = V_{DD} - I_D R_D$$

Since $V_S = I_D R_S$, the drain-to-source voltage is

$$V_{DS} = V_D - V_S = V_{DD} - I_D(R_D + R_S)$$

EXAMPLE 8–6 Find V_{DS} and V_{GS} in Figure 8–17, given that $I_D = 5$ mA.

FIGURE 8–17



Solution

$$V_S = I_D R_S = (5 \text{ mA})(470\ \Omega) = 2.35 \text{ V}$$
$$V_D = V_{DD} - I_D R_D = 15 \text{ V} - (5 \text{ mA})(1 \text{ k}\Omega) = 15 \text{ V} - 5 \text{ V} = 10 \text{ V}$$

Therefore,

$$V_{DS} = V_D - V_S = 10 \text{ V} - 2.35 \text{ V} = 7.65 \text{ V}$$

Since $V_G = 0$ V,

$$V_{GS} = V_G - V_S = 0 \text{ V} - 2.35 \text{ V} = -2.35 \text{ V}$$

Related Exercise Determine V_{DS} and V_{GS} in Figure 8–17 when $I_D = 8$ mA. Assume that $R_D = 860\ \Omega$, $R_S = 390\ \Omega$, and $V_{DD} = 12$ V.

Setting the Q-Point of a Self-Biased JFET

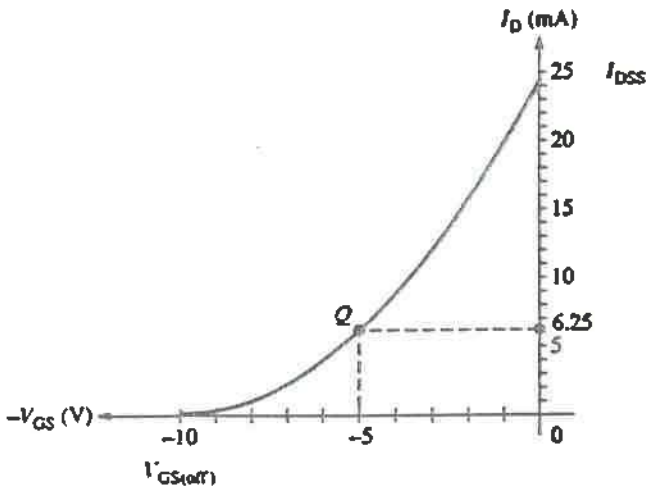
The basic approach to establishing a JFET bias point is to determine I_D for a desired value of V_{GS} or vice versa. Then calculate the required value of R_S using the relationship derived from Equation (8–5) and stated in Equation (8–7). The vertical lines indicate an absolute value.

$$R_S = \left| \frac{V_{GS}}{I_D} \right| \tag{8–7}$$

For a desired value of V_{GS}, I_D can be determined in either of two ways: from the transfer characteristic curve for the particular JFET, or more practically, from Equation (8–1) using I_{DSS} and $V_{GS(off)}$ from the JFET data sheet. The next two examples illustrate these procedures.

EXAMPLE 8–7 Determine the value of R_S required to self-bias an *n*-channel JFET having the transfer characteristic curve shown in Figure 8–18 at $V_{GS} = -5$ V.

FIGURE 8–18



Solution From the graph, $I_D = 6.25$ mA when $V_{GS} = -5$ V. Calculate R_S:

$$R_S = \left| \frac{V_{GS}}{I_D} \right| = \frac{5\text{ V}}{6.25\text{ mA}} = 800\ \Omega$$

Related Exercise Find R_S for $V_{GS} = -3$ V.

EXAMPLE 8–8

Determine the value of R_S required to self-bias a *p*-channel JFET with $I_{DSS} = 25$ mA and $V_{GS(off)} = 15$ V. V_{GS} is to be 5 V.

Solution Use Equation (8–1) to calculate I_D.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (25\text{ mA})\left(1 - \frac{5\text{ V}}{15\text{ V}}\right)^2 = (25\text{ mA})(1 - 0.333)^2 = 11.1\text{ mA}$$

Now, determine R_S.

$$R_S = \left|\frac{V_{GS}}{I_D}\right| = \frac{5\text{ V}}{11.1\text{ mA}} = 450\ \Omega$$

Since 450 Ω is not a standard value, use a 470 Ω resistor.

Related Exercise Find the value of R_S required to self-bias a *p*-channel JFET with $I_{DSS} = 18$ mA and $V_{GS(off)} = 8$ V. $V_{GS} = 4$ V.

Midpoint Bias It is often desirable to bias a JFET near the midpoint of its transfer characteristic curve where $I_D = I_{DSS}/2$. Under signal conditions, midpoint bias allows a maximum amount of drain current swing between I_{DSS} and 0. Using Equation (8–1), it is shown in Appendix B that I_D is approximately one-half of I_{DSS} when $V_{GS} = V_{GS(off)}/3.4$.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = I_{DSS}\left(1 - \frac{V_{GS(off)}/3.4}{V_{GS(off)}}\right)^2 = 0.5I_{DSS}$$

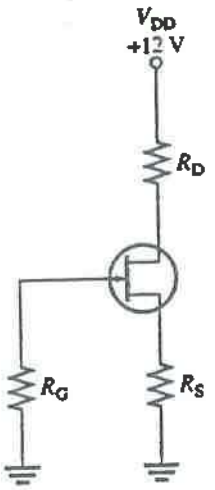
So, by selecting $V_{GS} = V_{GS(off)}/3.4$, you get a midpoint bias in terms of I_D.

To set the drain voltage at midpoint ($V_D = V_{DD}/2$), select a value of R_D to produce the desired voltage drop. Choose R_G arbitrarily large to prevent loading on the driving stage in a cascaded amplifier arrangement. Example 8–9 illustrates these concepts.

EXAMPLE 8–9

Select resistor values in Figure 8–19 to set up an approximate midpoint bias. The JFET parameters are $I_{DSS} = 15$ mA and $V_{GS(off)} = -8$ V. V_D should be 6 V (one-half of V_{DD}).

FIGURE 8–19



Solution For midpoint bias,

$$I_D \cong \frac{I_{DSS}}{2} = 7.5 \text{ mA}$$

and

$$V_{GS} \cong \frac{V_{GS(off)}}{3.4} = \frac{-8 \text{ V}}{3.4} = -2.35 \text{ V}$$

Then

$$R_S = \left| \frac{V_{GS}}{I_D} \right| = \frac{2.35 \text{ V}}{7.5 \text{ mA}} = 313 \ \Omega$$

$$V_D = V_{DD} - I_D R_D$$

$$I_D R_D = V_{DD} - V_D$$

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{12 \text{ V} - 6 \text{ V}}{7.5 \text{ mA}} = 800 \ \Omega$$

Use the nearest standard values of 330 Ω and 820 Ω.

Related Exercise Select resistor values in Figure 8–19 to set up an approximate midpoint bias. The JFET parameters are $I_{DSS} = 10$ mA and $V_{GS(off)} = -10$ V. $V_{DD} = 15$ V.

Graphical Analysis of a Self-Biased JFET

You can use the transfer characteristic curve of a JFET and certain parameters to determine the Q-point (I_D and V_{GS}) of a self-biased circuit. A circuit is shown in Figure 8–20(a), and a transfer characteristic curve is shown in Figure 8–20(b). If a curve is not available from the data sheet, you can plot it from Equation (8–1) using data sheet values for I_{DSS} and $V_{GS(off)}$.

To determine the Q-point of the circuit in Figure 8–20(a), a self-bias dc load line is established as follows. First, calculate V_{GS} when I_D is zero.

$$V_{GS} = -I_D R_S = (0)(470 \ \Omega) = 0 \text{ V}$$

This establishes a point at the origin on the graph ($I_D = 0$, $V_{GS} = 0$). Next, get I_{DSS} from the data sheet and calculate V_{GS} when $I_D = I_{DSS}$. From the curve, $I_{DSS} = 10$ mA for the JFET in Figure 8–20.

$$V_{GS} = -I_D R_S = -(10 \text{ mA})(470 \ \Omega) = -4.7 \text{ V}$$

This establishes a second point on the graph ($I_D = 10$ mA, $V_{GS} = -4.7$ V). Now, with two points, the load line can be drawn on the graph of the transfer characteristic curve as shown in Figure 8–21. The point where the line intersects the transfer characteristic curve is the Q-point of the circuit.

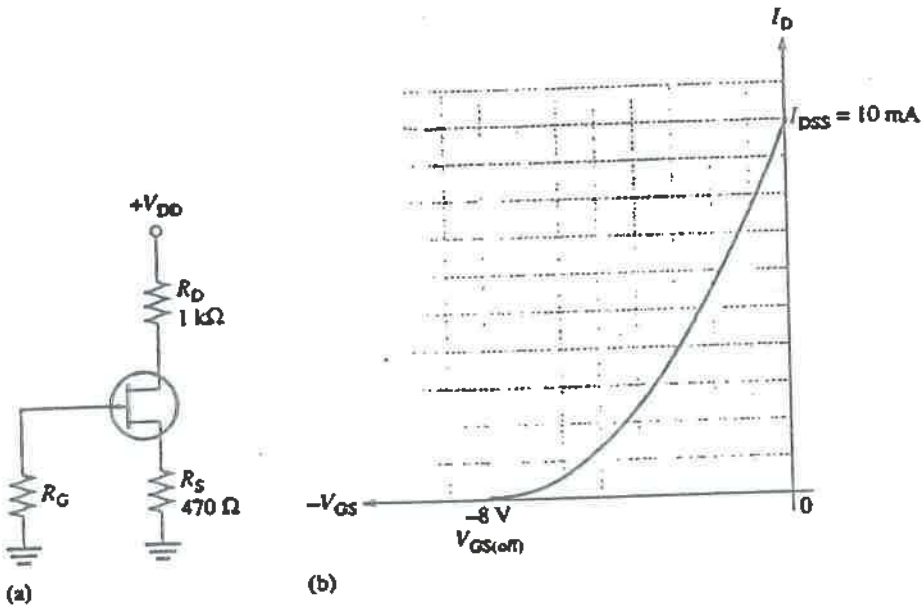
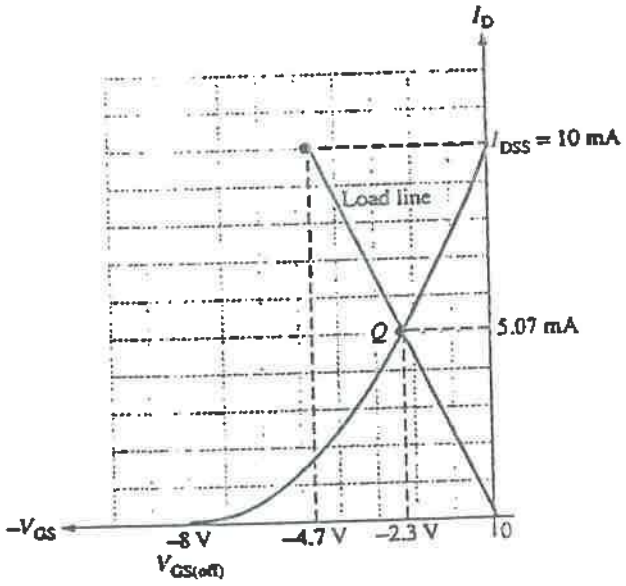


FIGURE 8–20
A self-biased JFET and its transfer characteristic curve.

FIGURE 8–21
The intersection of the self-bias dc load line and the transfer characteristic curve is the Q-point.



EXAMPLE 8–10 Determine the Q-point for the JFET circuit in Figure 8–22(a). The transfer characteristic curve is given in Figure 8–22(b).

Solution For $I_D = 0$,

$$V_{GS} = -I_D R_S = (0)(680\ \Omega) = 0\ \text{V}$$

This gives a point at the origin. From the curve, $I_{DSS} = 4$ mA. So for $I_D = I_{DSS} = 4$ mA.

$$V_{GS} = -I_D R_S = -(4 \text{ mA})(680\ \Omega) = -2.72 \text{ V}$$

This gives a second point at 4 mA and –2.72 V. A line is now drawn between the two points, and the values of I_D and V_{GS} at the intersection of the line and the curve are taken from the graph, as illustrated in Figure 8–22(b). The Q-point values from the graph are $I_D = 2.25$ mA and $V_{GS} = -1.5$ V.

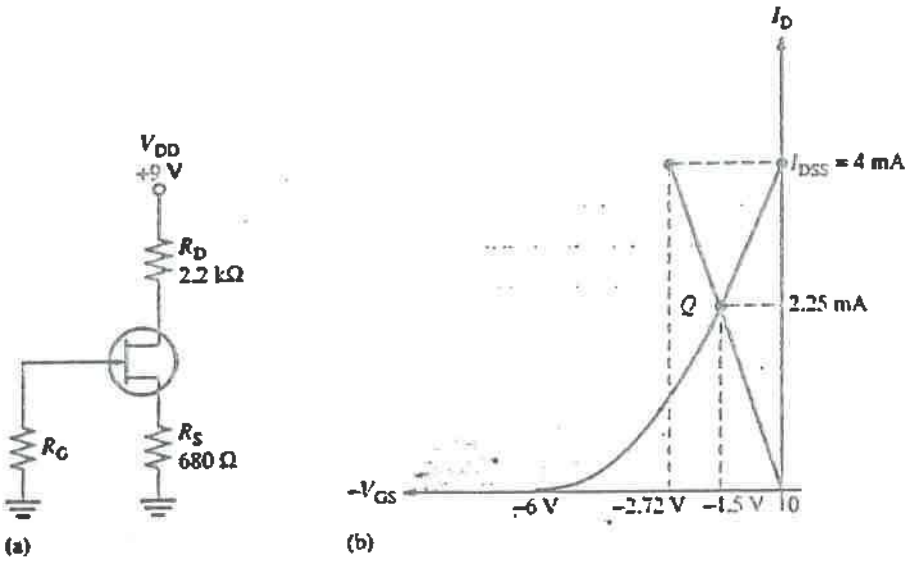


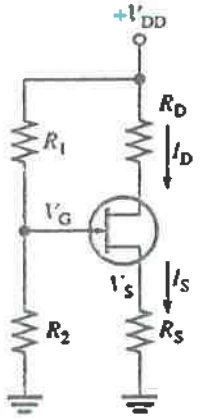
FIGURE 8–22

Related Exercise If R_S is increased to 1 kΩ in Figure 8–22(a), what is the new Q-point?

Voltage-Divider Bias

An *n*-channel JFET with voltage-divider bias is shown in Figure 8–23. The voltage at the source of the JFET must be more positive than the voltage at the gate in order to keep the gate-source junction reverse-biased.

FIGURE 8–23
An n-channel JFET with voltage-divider bias ($I_S = I_D$).



The source voltage is

$$V_S = I_D R_S$$

The gate voltage is set by resistors R_1 and R_2 as expressed by the following equation using the voltage-divider formula:

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD} \tag{8–8}$$

The gate-to-source voltage is

$$V_{GS} = V_G - V_S$$

and the source voltage is

$$V_S = V_G - V_{GS}$$

The drain current can be expressed as

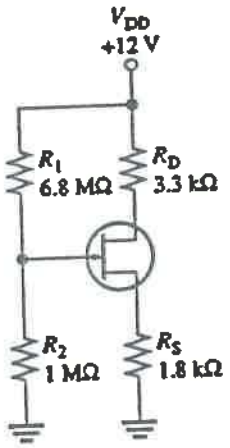
$$I_D = \frac{V_S}{R_S}$$

Substituting for V_S,

$$I_D = \frac{V_G - V_{GS}}{R_S} \tag{8–9}$$

EXAMPLE 8–11 Determine I_D and V_{GS} for the JFET with voltage-divider bias in Figure 8–24, given that $V_D = 7$ V.

FIGURE 8–24



Solution

$$I_D = \frac{V_{DD} - V_D}{R_D} = \frac{12\text{ V} - 7\text{ V}}{3.3\text{ k}\Omega} = \frac{5\text{ V}}{3.3\text{ k}\Omega} = 1.52\text{ mA}$$

Calculate the gate-to-source voltage as follows:

$$V_S = I_D R_S = (1.52\text{ mA})(1.8\text{ k}\Omega) = 2.74\text{ V}$$

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} = \left(\frac{1\text{ M}\Omega}{7.8\text{ M}\Omega}\right)12\text{ V} = 1.54\text{ V}$$

$$V_{GS} = V_G - V_S = 1.54\text{ V} - 2.74\text{ V} = -1.2\text{ V}$$

If V_D had not been given in this example, the Q-point values could not have been found without the transfer characteristic curve.

Related Exercise Given that $V_D = 6$ V in Figure 8–24, determine the Q-point.

Graphical Analysis of a JFET with Voltage-Divider Bias

An approach similar to the one used for self-bias can be used with voltage-divider bias to graphically determine the Q-point of a circuit on the transfer characteristic curve.

In a JFET with voltage-divider bias when $I_D = 0$, V_{GS} is not zero, as in the self-biased case, because the voltage divider produces a voltage at the gate independent of the drain current. The voltage-divider dc load line is determined as follows.

For $I_D = 0$,

$$V_S = I_D R_S = (0)R_S = 0\text{ V}$$

$$V_{GS} = V_G - V_S = V_G - 0\text{ V} = V_G$$

Therefore, one point on the line is at $I_D = 0$ and $V_{GS} = V_G$.

For $V_{GS} = 0$,

$$I_D = \frac{V_G - V_{GS}}{R_S} = \frac{V_G}{R_S}$$

A second point on the line is at $I_D = V_G/R_S$ and $V_{GS} = 0$. The dc load line is shown in Figure 8–25.

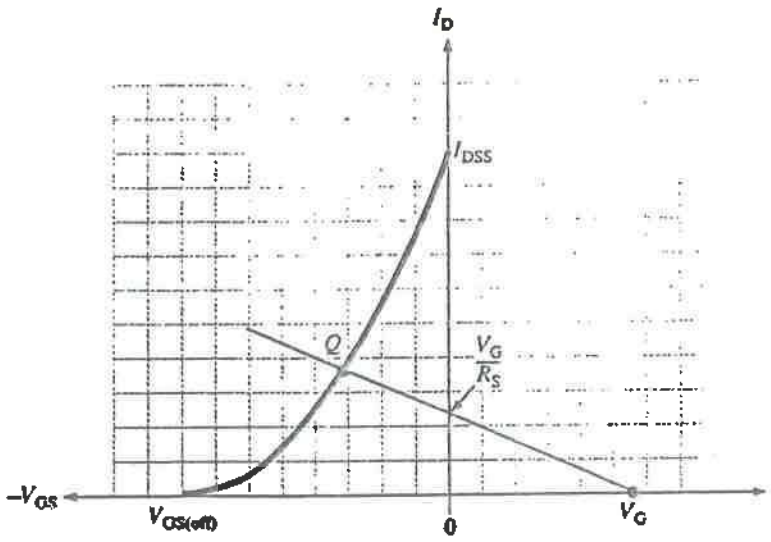


FIGURE 8–25
DC load line for a JFET with voltage-divider bias.

EXAMPLE 8–12 Determine the Q-point for the JFET with voltage-divider bias in Figure 8–26(a), given the transfer characteristic curve in Figure 8–26(b).

Solution First, establish the two points for the bias line.

For $I_D = 0$,

$$V_{GS} = V_G = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} = \left(\frac{2.2\ \text{M}\Omega}{4.4\ \text{M}\Omega}\right)8\ \text{V} = 4\ \text{V}$$

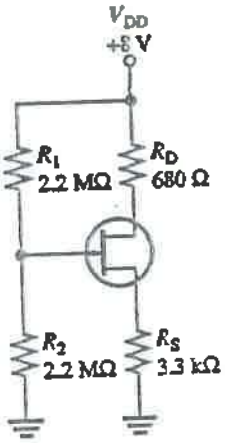
The first point is at $I_D = 0$ and $V_{GS} = 4$ V.

For $V_{GS} = 0$,

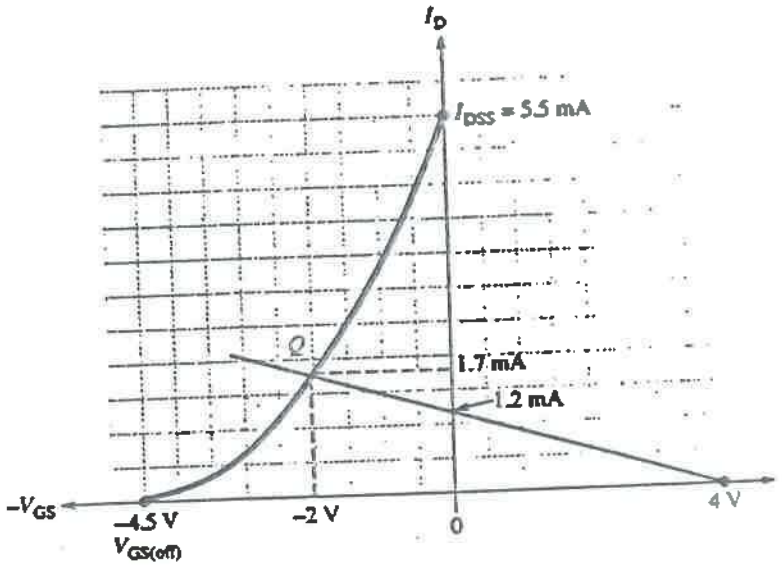
$$I_D = \frac{V_G - V_{GS}}{R_S} = \frac{V_G}{R_S} = \frac{4\ \text{V}}{3.3\ \text{k}\Omega} = 1.2\ \text{mA}$$

The second point is at $I_D = 1.2$ mA and $V_{GS} = 0$.

The load line is drawn in Figure 8–26(b), and the Q-point values of $I_D = 1.7$ mA and $V_{GS} = -2$ V are picked off the graph, as indicated.



(a)



(b)

FIGURE 8–26

Related Exercise Change R_S to 4.7 kΩ and determine the Q-point for the circuit in Figure 8–26(a).

Q-Point Stability

Unfortunately, the transfer characteristic of a JFET can differ considerably from one device to another of the same type. If, for example, a 2N5459 JFET is replaced in a given bias circuit with another 2N5459, the transfer characteristic curve can vary greatly as illustrated in Figure 8–27(a). In this case, the maximum I_{DSS} is 16 mA and the minimum

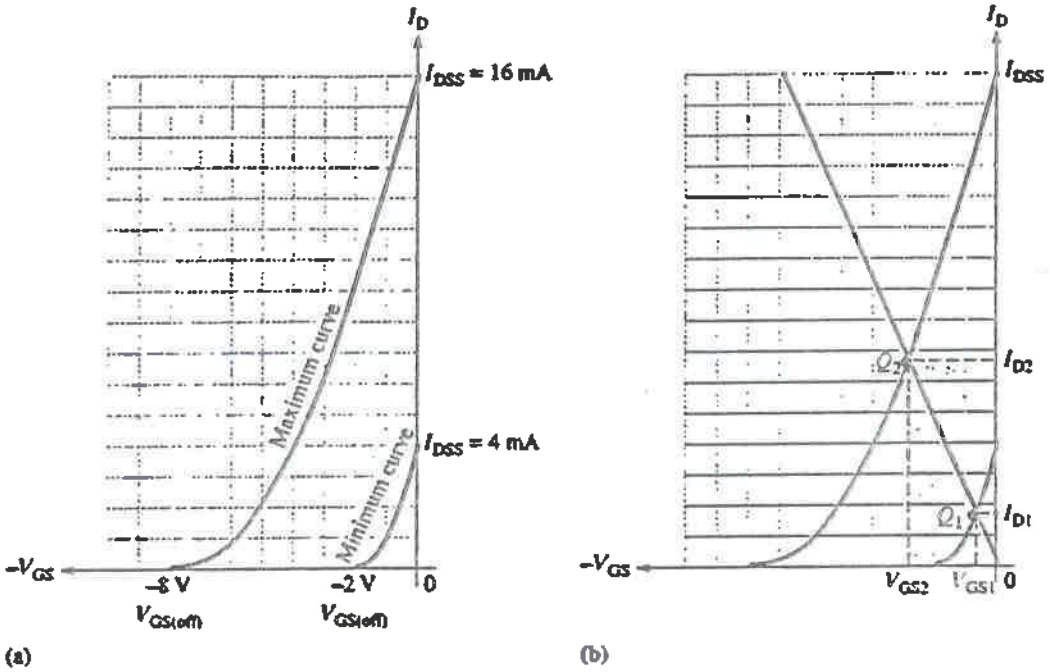


FIGURE 8–27
Variation in the transfer characteristic of 2N5459 JFETs and the effect on the Q-point.

I_{DSS} is 4 mA. Likewise, the maximum $V_{GS(off)}$ is −8 V and the minimum $V_{GS(off)}$ is −2 V. This means that if you have a selection of 2N5459s and you randomly pick one out, it can have values anywhere within these ranges.

If a self-bias dc load line is drawn as illustrated in Figure 8–27(b), the same circuit using a 2N5459 can have a Q-point anywhere along the line from Q_1, the minimum bias point, to Q_2, the maximum bias point. Accordingly, the drain current can be any value between I_{D1} and I_{D2}, as shown. This means that the dc voltage at the drain can have a range of values depending on I_D. Also, the gate-to-source voltage can be any value between V_{GS1} and V_{GS2}, as indicated.

With voltage-divider bias, the dependency of I_D on the range of Q-points is reduced because the slope of the bias line is less than for self-bias. Although V_{GS} varies quite a bit for both self-bias and voltage-divider bias, I_D is much more stable with voltage-divider bias, as illustrated in Figure 8–28.

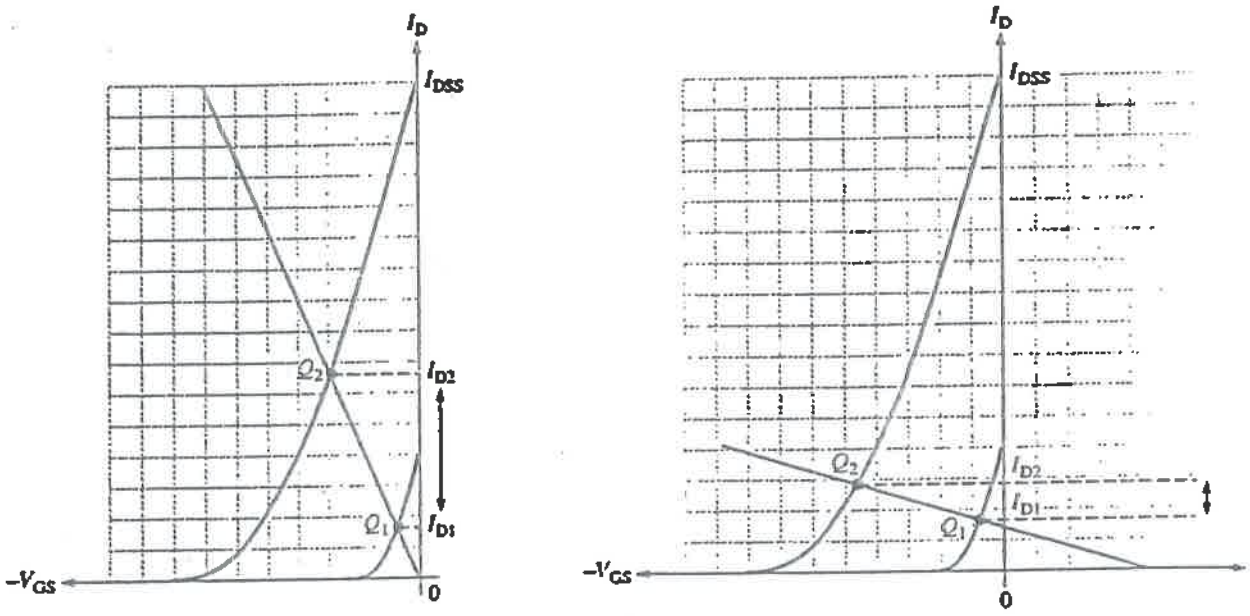


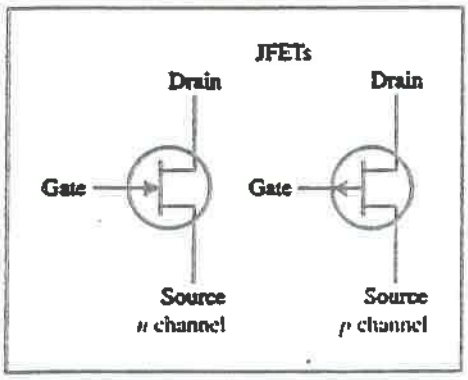
FIGURE 8–28
The change in I_D between the minimum and the maximum Q-points is much less for a JFET with voltage-divider bias than for a self-biased JFET.

SECTION 8–3 REVIEW

1. Should a *p*-channel JFET have a positive or a negative V_{GS}?
2. In a certain self-biased *n*-channel JFET circuit, $I_D = 8$ mA and $R_S = 1$ kΩ. Determine V_{GS}.
3. An *n*-channel JFET with voltage-divider bias has a gate voltage of 3 V and a source voltage of 5 V. Calculate V_{GS}.

SUMMARY OF FIELD-EFFECT TRANSISTORS

JFETs



- Gate-source junction must be reverse-biased.
- V_{GS} controls I_D.
- Value of V_{DS} at which I_D becomes constant is the pinch-off voltage.
- Value of V_{GS} at which I_D becomes zero is the cutoff voltage, $V_{GS(off)}$.
- I_{DSS} is drain current when $V_{GS} = 0$.
- Transfer characteristic:

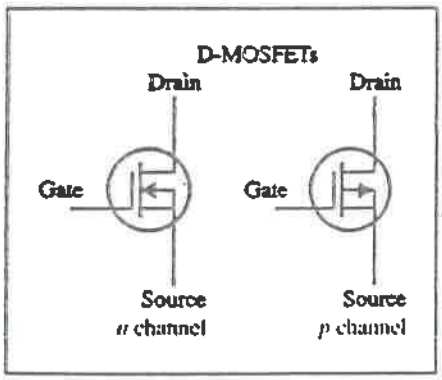
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

- Forward transconductance:

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$$

$$g_{m0} = \frac{2I_{DSS}}{|V_{GS(off)}|}$$

D-MOSFETs



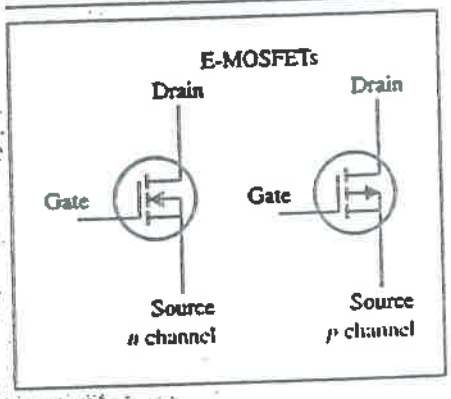
Except that it can be operated in enhancement mode, the D-MOSFET characteristics are the same as JFET.

- *Depletion mode:*
  - *n* channel: V_{GS} negative
  - *p* channel: V_{GS} positive
- *Enhancement mode:*
  - *n* channel: V_{GS} positive
  - *p* channel: V_{GS} negative
- V_{GS} controls I_D.
- Value of V_{GS} at which I_D becomes zero is the cutoff voltage, $V_{GS(off)}$.
- I_{DSS} is drain current when $V_{GS} = 0$.
- Transfer characteristic:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

SUMMARY OF FIELD-EFFECT TRANSISTORS, *continued*

E-MOSFETs



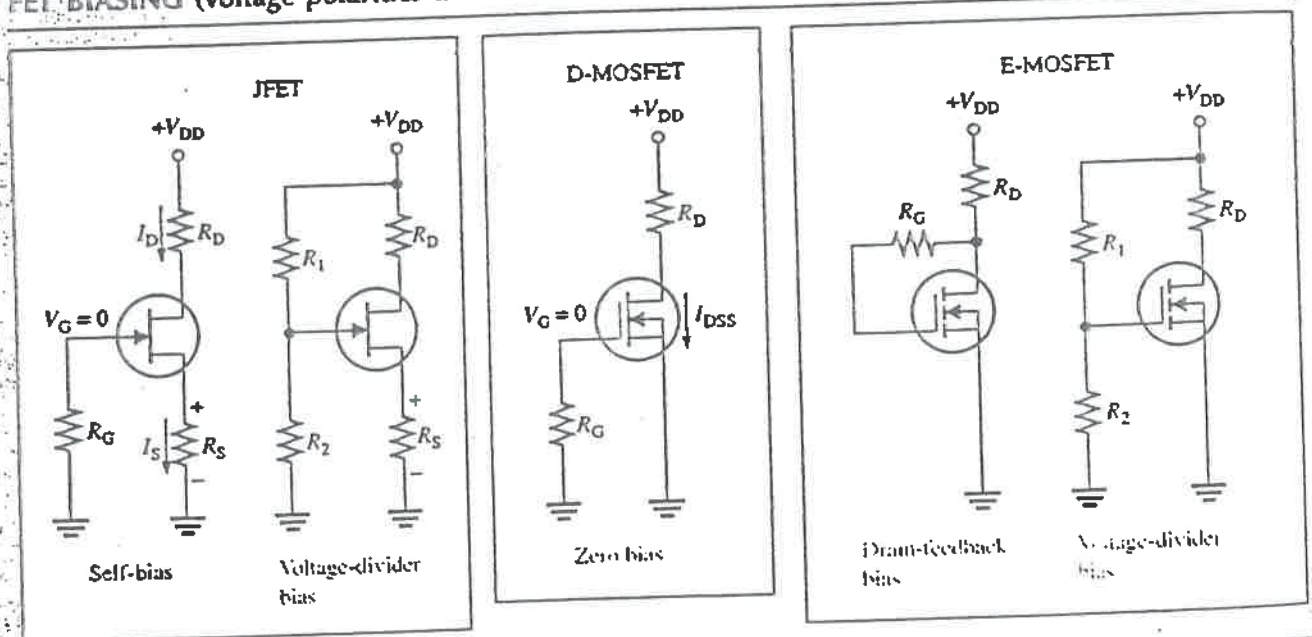
There is no depletion mode and characteristics differ from D-MOSFET.

- *Enhancement mode:*
  - *n* channel: V_{GS} positive
  - *p* channel: V_{GS} negative
- V_{GS} controls I_D.
- Value of V_{GS} at which I_D starts to flow is the threshold voltage, $V_{GS(th)}$.
- Transfer characteristic:

$$I_D = K(V_{GS} - V_{GS(th)})^2$$

- K in formula can be calculated by substituting data sheet values $I_{D(on)}$ for I_D and V_{GS} at which $I_{D(on)}$ is specified for V_{GS}.

FET BIASING (voltage polarities and current directions reverse for *p* channel)



8-4 SMALL-SIGNAL FET AMPLIFIERS

8-4-1 JFET Common-Source Amplifier

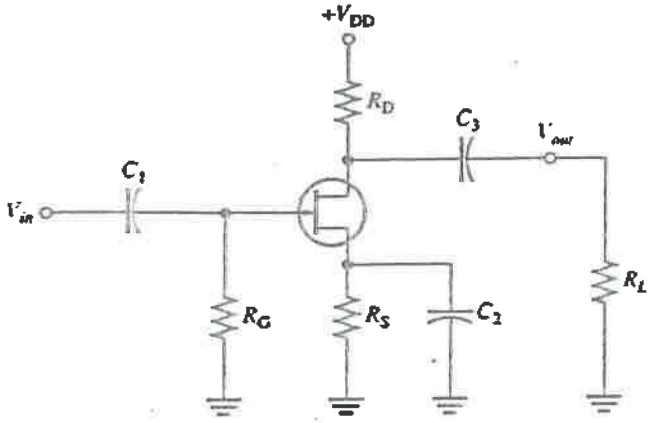


FIGURE 9–12
JFET common-source amplifier.

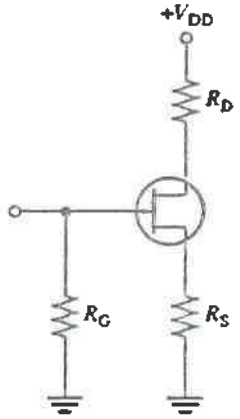
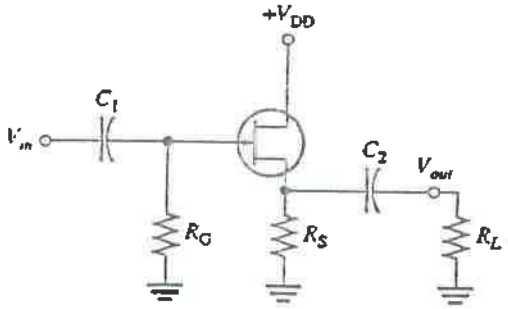


FIGURE 9–13
DC equivalent circuit for the amplifier in Figure 9–12.

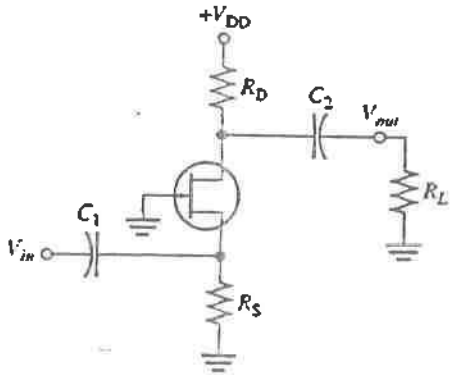
8-4-2 JFET Common-Drain Amplifier

FIGURE 9–22
JFET common-drain amplifier (source-follower).



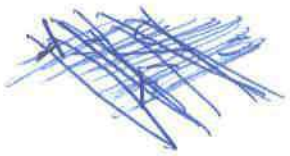
8-4-3 JFET Common-Gate Amplifier

FIGURE 9–26
JFET common-gate amplifier.



44115594 كاظم البكري

1- What is the wavelength of FM radio channel with 90 MHz frequency ?



$$\lambda = \frac{c}{F} = \frac{3 \times 10^8 \ m/s}{90 \times 10^6 \ Hz} = 3.33 \ m$$

2- The wavelength of a Greenn laser light is abut 500nm, determnine the frequency? (Use suitable metric Prefix)

$$f = \frac{c}{\lambda} = \frac{3 \times 10^8 \ m/s}{500 \times 10^{-9} \ m} = 6 \times 10^{14} \ Hz$$