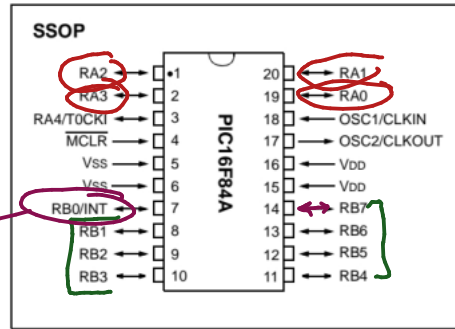
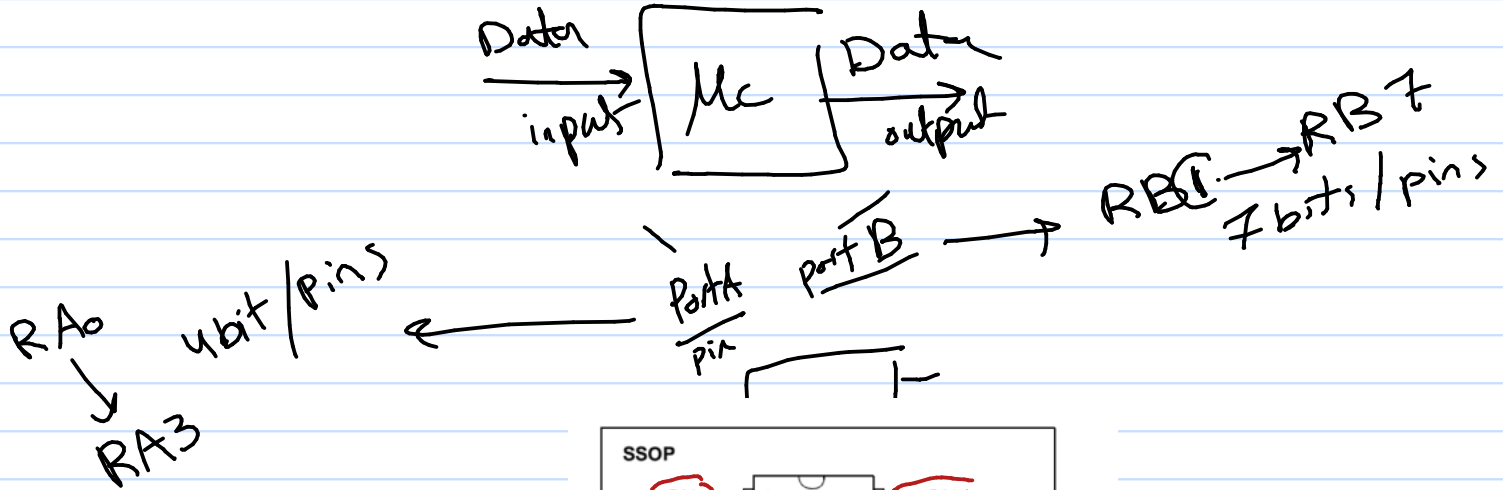


<< lab 4 >>

Input & output



interrupts

bidirectional
↓
input or output

PORTA → TRISA
PORTB → TRISB

FIGURE 2-2: REGISTER FILE MAP - PIC16F84A

File Address	Register Name	File Address	Register Name
00h	Indirect addr. ⁽¹⁾	80h	Indirect addr. ⁽¹⁾
01h	TMR0	81h	OPTION_REG
02h	PCL	82h	PCL
03h	STATUS	83h	STATUS
04h	FSR	84h	FSR
05h	PORTA	85h	TRISA
06h	PORTB	86h	TRISB
07h	—	87h	—
08h	EEDATA	88h	EECON1
09h	EEADR	89h	EECON2 ⁽¹⁾
0Ah	PCLATH	8Ah	PCLATH
0Bh	INTCON	8Bh	INTCON
0Ch	—	8Ch	—
68 General Purpose Registers (SRAM)		Mapped (accesses) in Bank 0	
4Fh	—	CFh	—
50h	—	D0h	—
Bank 0		Bank 1	
7Fh	—	FFh	—

0x2

CLRF TRISA
PAA
0000

MovLW 0xFF
MovWF TRISA

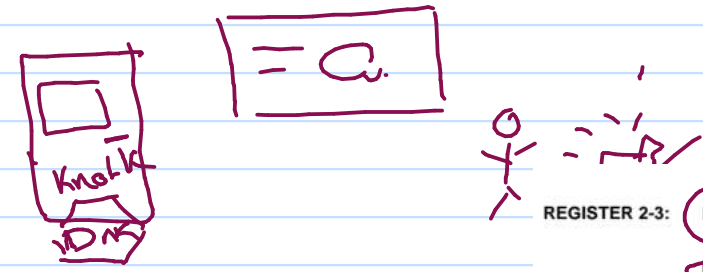
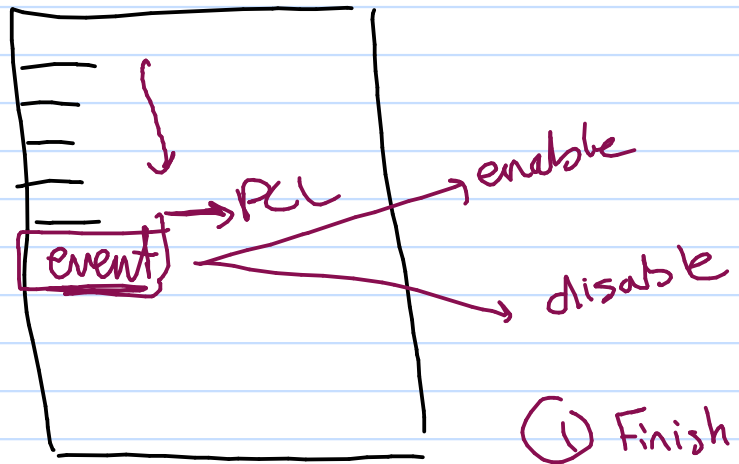
TRISA
0000 1111

PORTA
- 1111
output inputs

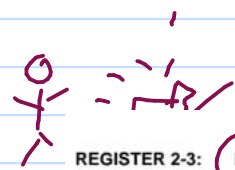
bit RPO
status
Bank 0 Bank 1

set=1
clear=0
BSF status, RPO; Bank 1
BCF status, RPO; Bank 0

<< Interrupts >>



- ① Finish the current Event
- ② save PCL value
- ③ loading the new PCL (004)
- ④ clear the flag
- ⑤ perform the instruct
- ⑥ Return from terrup and PCL
- ⑦ Return Back at:



REGISTER 2-3:

INTCON REGISTER (ADDRESS 0Bh, 8Bh)

	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
bit 7	GIE	EEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF
bit 7	<p>GIE: Global Interrupt Enable bit 1 = Enables all unmasked interrupts 0 = Disables all interrupts</p>							
bit 6	<p>EEIE: EE Write Complete Interrupt Enable bit 1 = Enables the EE Write Complete interrupts 0 = Disables the EE Write Complete interrupt</p>							
bit 5	<p>TOIE: TMR0 Overflow Interrupt Enable bit 1 = Enables the TMR0 interrupt 0 = Disables the TMR0 interrupt</p>							
bit 4	<p>INTE: RB0/INT External Interrupt Enable bit 1 = Enables the RB0/INT external interrupt 0 = Disables the RB0/INT external interrupt</p>							
bit 3	<p>RBIE: RB Port Change Interrupt Enable bit 1 = Enables the RB port change interrupt 0 = Disables the RB port change interrupt</p>							
bit 2	<p>TOIF: TMR0 Overflow Interrupt Flag bit 1 = TMR0 register has overflowed (must be cleared in software) 0 = TMR0 register did not overflow</p>							
bit 1	<p>INTF: RB0/INT External Interrupt Flag bit 1 = The RB0/INT external interrupt occurred (must be cleared in software) 0 = The RB0/INT external interrupt did not occur</p>							
bit 0	<p>RBIF: RB Port Change Interrupt Flag bit 1 = At least one of the RB7:RB4 pins changed state (must be cleared in software) 0 = None of the RB7:RB4 pins have changed state</p>							

Legend:
 R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

$TRISB, 0 \rightarrow BSF$

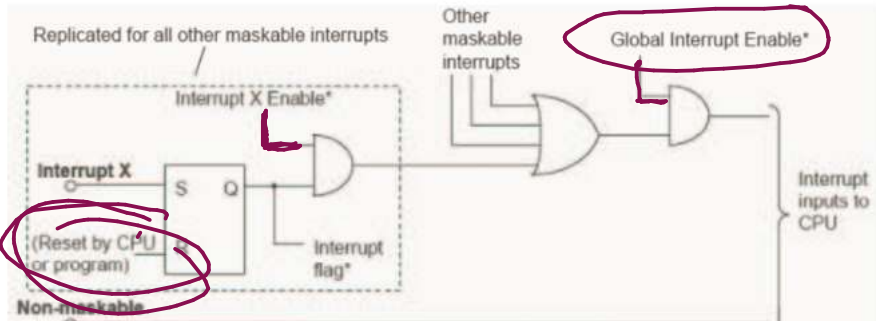
$BSF\ INTCON, GIE$
 $BSF\ INTCON, INTE$

ISR
 Interrupt service Routine

$BCF\ INTCON, INTF$

$RETfie$

sig 100#4
 Retfie
 GOTO ISR



GIE

3. Interrupts

Program 3: Write the following program in the source code file (**Note that this program requires the Delay.inc include file**):

```

BSF STATUS, RP0
CLRF TRISA
BSF TRISB, 0
BSF INTCON, GIE
BSF INTCON, INTE
BCF STATUS, RP0
LOOP CLRF PORTA
GOTO LOOP

ISR BCF INTCON, INTF
COMF PORTA
CALL delay500ms
RETIE
  
```

Handwritten notes:

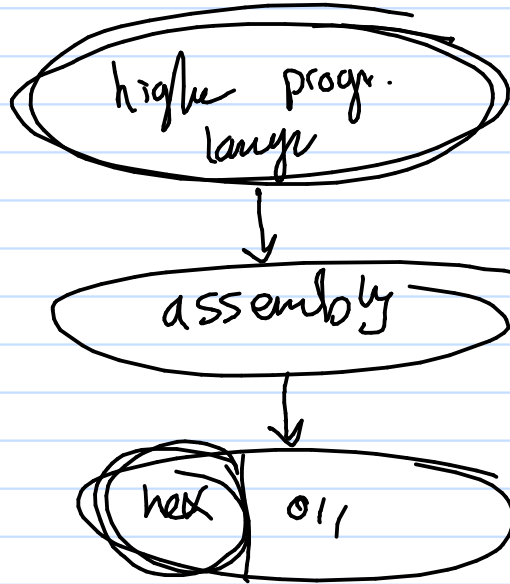
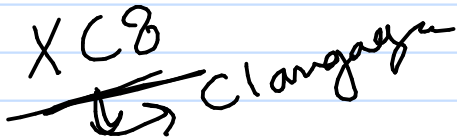
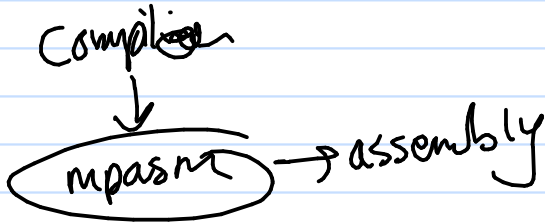
- man # include "Delay.inc"
- Bank 0
- PORTA output
- RBO → input (interrupt)
- External Interrupt
- External Reg
- Delay.inc
- 0000
- 1111

Code 3 – Program 3

MPLAB

Assembly

C code



PICKIT3

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