UNIT 7

POWER AMPLIFIERS

7–1 ■ CLASS A AMPLIFIERS

When a common-emitter, common-collector, or common-base amplifier is biased so that it operates in the linear region for the full 360° of the input cycle, it is a class A amplifier. In this mode of operation, the amplifier does not go into cutoff or saturation; therefore, the output voltage waveform has the same shape as the input waveform. A class A amplifier can be either inverting or noninverting. All of the small-signal amplifiers that you studied in Chapter 6 were class A. In this section, you will learn about large-signal class A amplifiers.

After completing this section, you should be able to

- **Explain and analyze the operation of large-signal class A amplifiers**
  - ☐ Explain class A operation
  - ☐ Discuss how the location of the Q-point on the ac load line affects the operation of the amplifier
  - ☐ Analyze ac load line operation
  - ☐ Explain how to center the Q-point on the load line
  - ☐ Determine large-signal voltage gain
  - ☐ Discuss distortion
  - ☐ Calculate power gain and quiescent power
  - ☐ Calculate ac output power for several Q-point conditions
  - ☐ Determine the efficiency of a class A amplifier
  - ☐ Determine the maximum load power

The operation of a class A large-signal amplifier is illustrated in Figure 7–1, where the output waveform is an amplified replica of the input and may be either in phase or 180° out of phase with the input.

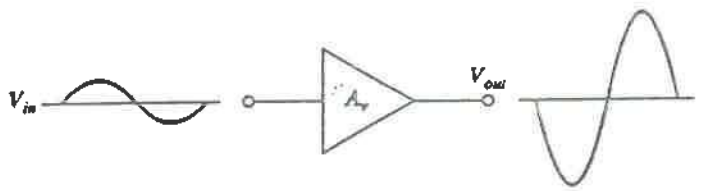


FIGURE 7–1
Basic class A amplifier operation (inverting).

Centered Q-Point for Maximum Output Signal

When the Q-point is at the center of the ac load line (midway between saturation and cutoff), a maximum class A signal can be obtained. This is graphically illustrated in the ac load line in Figure 7–2(a). Ideally, the collector current can vary from its Q-point value, I_{CQ}, up to its saturation value $I_{c(sat)}$, and down to its cutoff value of zero. This operation is indicated in Figure 7–2(b).

As you can see in Figure 7–2(b), the peak value of the collector current equals I_{CQ}, and the peak value of the collector-to-emitter voltage equals V_{CEQ}. This is the largest signal achievable from a class A amplifier. When the input signal is too large, the amplifier is driven into cutoff and saturation, as illustrated in Figure 7–3.

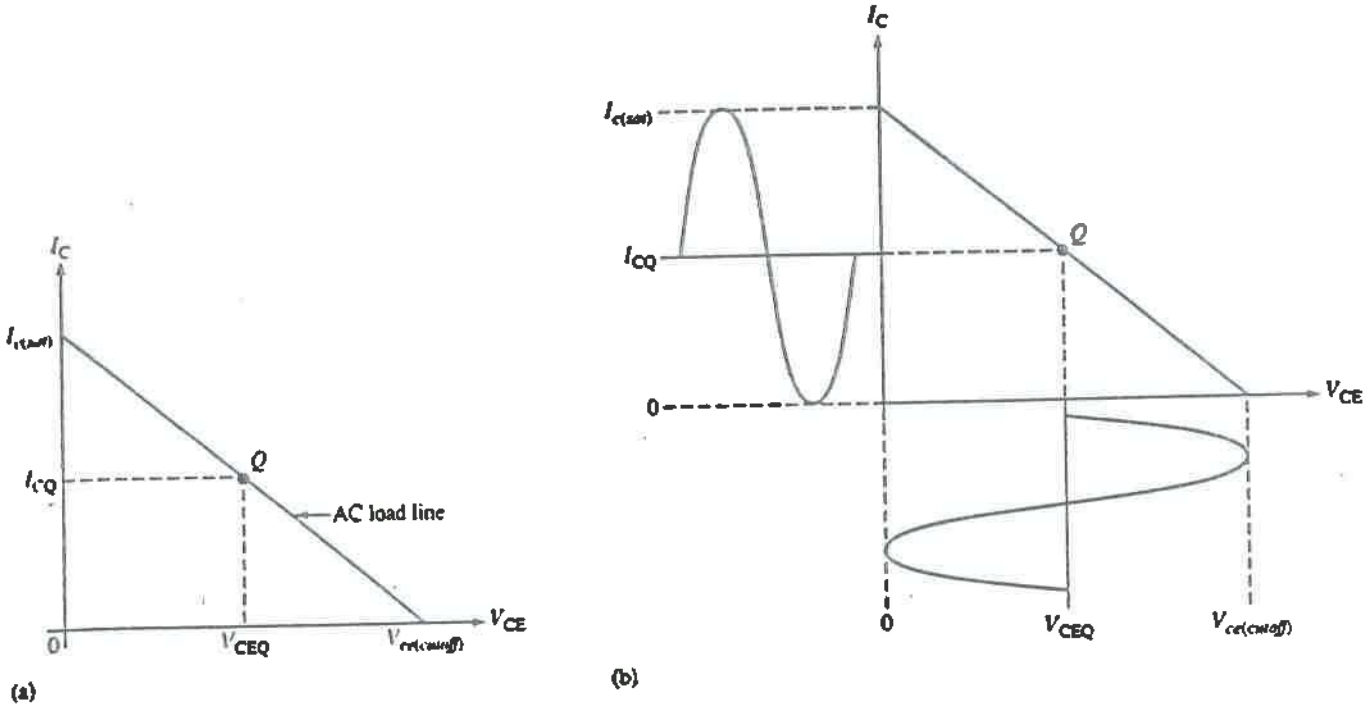


FIGURE 7–2
For maximum class A operation, the Q-point is centered on the ac load line.

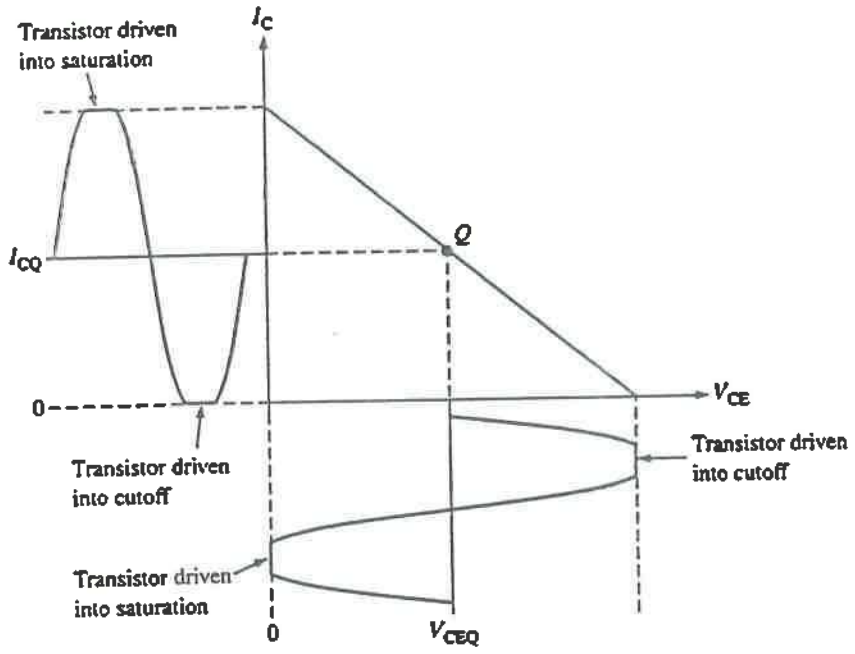
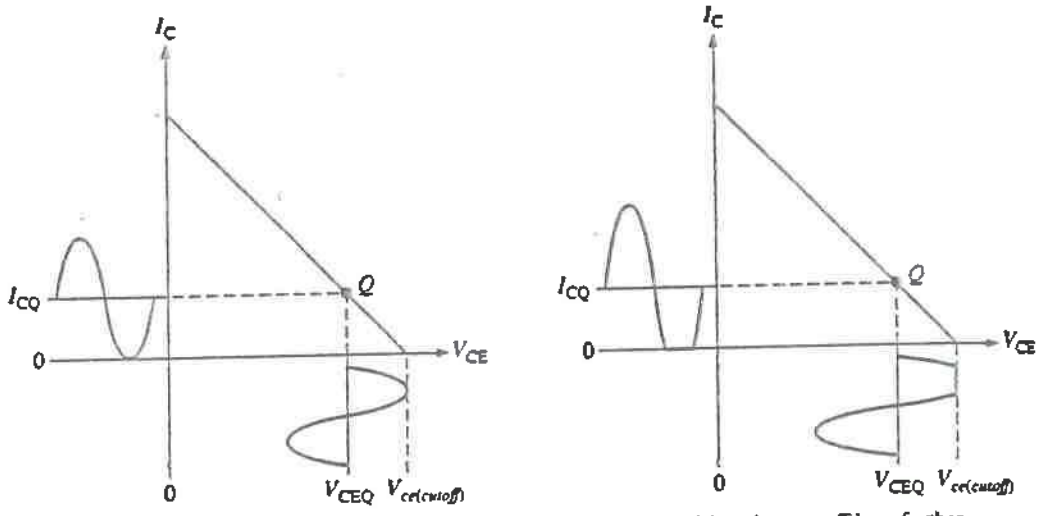


FIGURE 7–3
Waveforms are clipped at cutoff and saturation because the amplifier is overdriven (too large an input signal).

A Noncentered Q-Point Limits the Output

Q-Point Closer to Cutoff If the Q-point is not centered on the ac load line, V_{ce} is limited to less than the possible maximum. Figure 7–4(a) shows an ac load line with the Q-point moved away from center toward cutoff. V_{ce} is limited by cutoff in this case. The collector current can swing only down to near zero and an equal amount above I_{CQ}. The collector-to-emitter voltage can swing only up to its cutoff value and an equal amount below V_{CEQ}. If the amplifier is driven any further than this by an increase in the input signal, it will go into cutoff, as shown in Figure 7–4(b), and the waveforms will be clipped off on one peak.



(a) Amplitude of V_{ce} and I_c limited by cutoff

(b) Transistor driven into cutoff by a further increase in input amplitude

FIGURE 7–4
Q-point closer to cutoff.

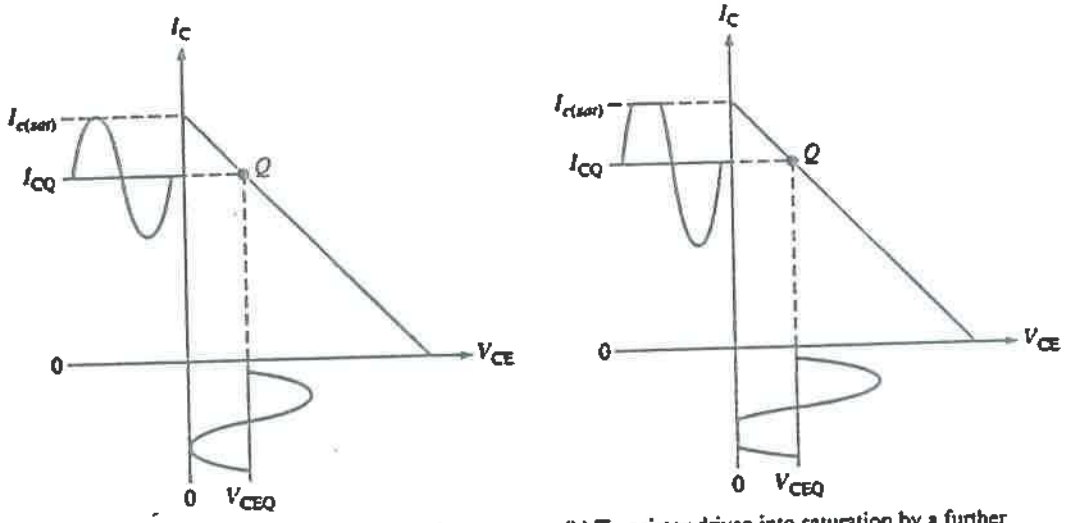
Q-Point Closer to Saturation Figure 7–5(a) shows an ac load line with the Q-point moved away from center toward saturation. In this case, V_{ce} is limited by saturation. The collector current can swing only up to near saturation and an equal amount below I_{CQ}. The collector-to-emitter voltage can swing only down to near its saturation value and an equal amount above V_{CEQ}. If the amplifier is driven any further than this by an increase in the input signal, it will go into saturation, as shown in Figure 7–5(b).

Large-Signal Load Line Operation

Recall that an amplifier such as that shown in Figure 7–6 can be represented in terms of either its dc or its ac equivalent.

DC Load Line Using the dc equivalent circuit in Figure 7–7(a), you can determine the dc load line as follows: $I_{C(sat)}$ occurs when $V_{CE} \cong 0$, so

$$I_{C(sat)} \cong \frac{V_{CC}}{R_C + R_E}$$



(a) Amplitude of V_{ce} and I_c limited by saturation

(b) Transistor driven into saturation by a further increase in input amplitude

FIGURE 7–5
Q-point closer to saturation.

FIGURE 7–6
Common-emitter amplifier with signal source.

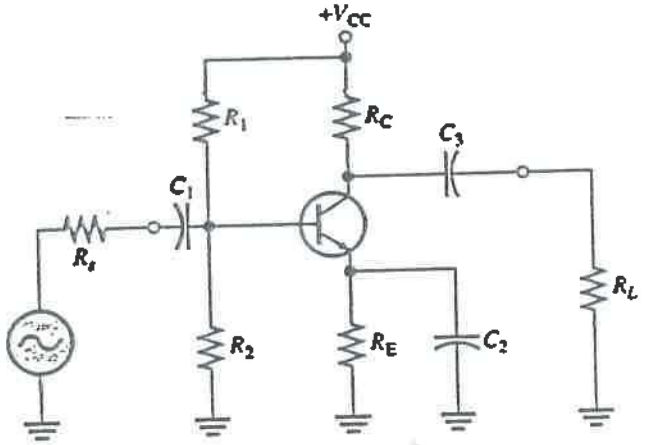
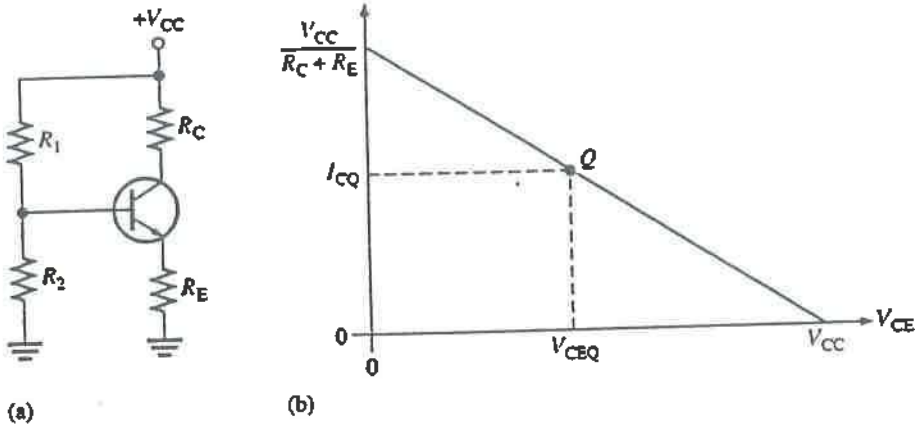


FIGURE 7–7
DC equivalent circuit and dc load line for the amplifier in Figure 7–6.



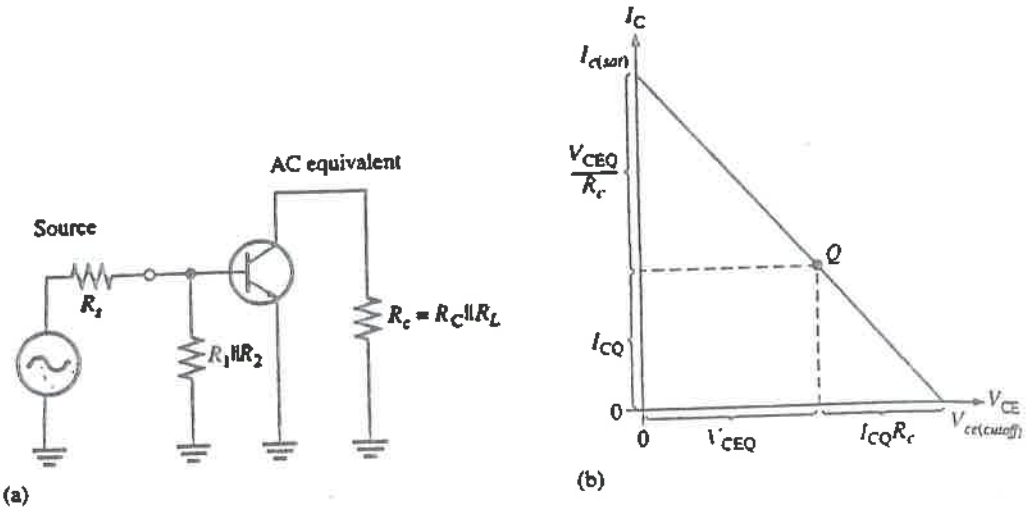


FIGURE 7–8
AC equivalent circuit and ac load line for the amplifier in Figure 7–6.

$V_{CE(cutoff)}$ occurs when $I_C \cong 0$, so

$$V_{CE(cutoff)} \cong V_{CC}$$

The dc load line is shown in Figure 7–7(b).

AC Load Line From the ac viewpoint, the circuit in Figure 7–6 looks different than it does from the dc viewpoint. The collector resistance is different because R_L is in parallel with R_C due to the coupling capacitor C_3, and the emitter resistance is zero due to the bypass capacitor C_2; therefore, the ac load line is different from the dc load line. How much collector current can there be under ac conditions before saturation occurs? To answer this question, refer to the ac equivalent circuit and ac load line in Figure 7–8. Remember that a lowercase italic subscript indicates an ac quantity and an uppercase nonitalic subscript indicates a dc quantity. For example, R_c is the ac collector resistance and R_C is the dc collector resistance. I_{CQ} and V_{CEQ} are the dc Q-point coordinates. Going from the Q-point to the saturation point, the collector-to-emitter voltage swings from V_{CEQ} to near 0; that is, $\Delta V_{CE} = V_{CEQ}$. The change in collector current going from the Q-point to saturation is therefore

$$\Delta I_C = \frac{V_{CEQ}}{R_c}$$

where $R_c = R_C \| R_L$ is the ac collector resistance. The ac collector current at saturation is

$$I_{c(sat)} = I_{CQ} + \Delta I_C$$

Thus,

$$I_{c(sat)} = I_{CQ} + \frac{V_{CEQ}}{R_c} \tag{7–1}$$

Going from the Q-point to the cutoff point, the collector current swings from I_{CQ} to near 0; that is, $\Delta I_C = I_{CQ}$. The change in collector-to-emitter voltage going from the Q-point to cutoff is therefore

$$\Delta V_{CE} = (\Delta I_C)R_c = I_{CQ}R_c$$

The cutoff value of ac collector-to-emitter voltage is

$$V_{ce(cutoff)} = V_{CEQ} + I_{CQ}R_c \tag{7–2}$$

These results are shown on the ac load line of Figure 7–9. The corresponding dc load line is shown for comparison.

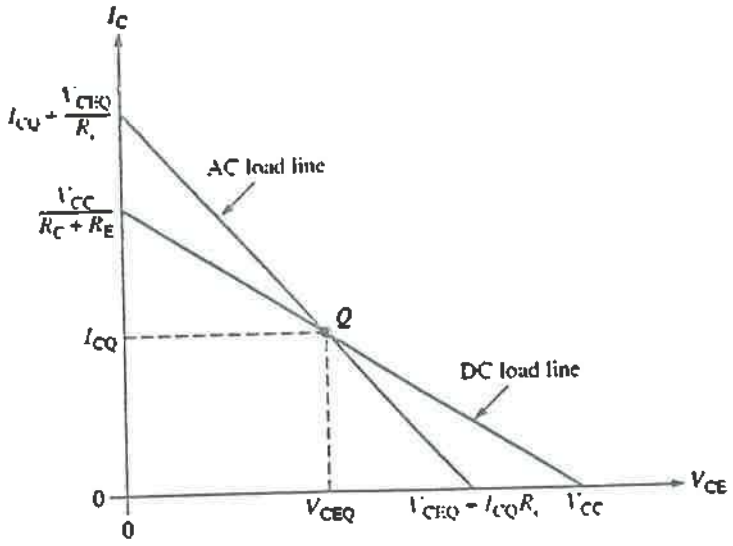
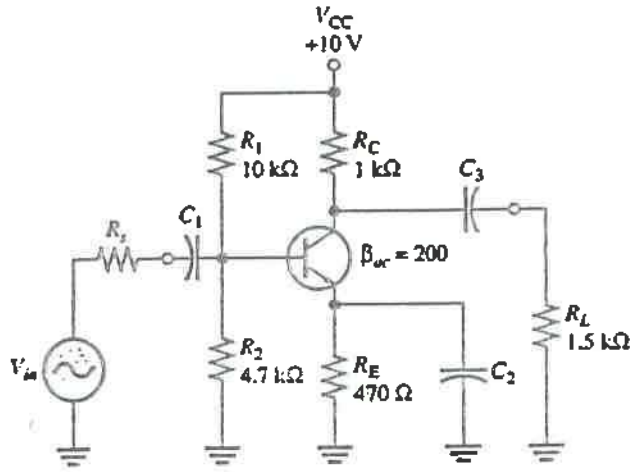


FIGURE 7–9
DC and ac load lines.

EXAMPLE 7–1

Determine the collector current and the collector-to-emitter voltage at the points of saturation and cutoff in Figure 7–10 with an ac signal input. Assume $X_{C1} = X_{C2} = X_{C3} \cong 0\ \Omega$.

FIGURE 7–10



Solution The Q-point values for this amplifier are determined as follows (neglecting $R_{IN(base)}$):

$$V_{BQ} \cong \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{4.7\ \text{k}\Omega}{14.7\ \text{k}\Omega}\right)10\ \text{V} = 3.2\ \text{V}$$

Then,

$$I_{EQ} = \frac{V_{BQ} - 0.7\ \text{V}}{R_E} = \frac{3.2\ \text{V} - 0.7\ \text{V}}{470\ \Omega} = 5.3\ \text{mA}$$

Therefore, since $I_C \cong I_E$,

$$I_{CQ} \cong 5.3\ \text{mA}$$

The collector voltage is

$$V_{CQ} \cong V_{CC} - I_{CQ}R_C = 10\ \text{V} - (5.3\ \text{mA})(1\ \text{k}\Omega) = 4.7\ \text{V}$$

Therefore, the collector-to-emitter voltage is

$$V_{CEQ} = V_{CQ} - I_{EQ}R_E = 4.7\ \text{V} - 2.5\ \text{V} = 2.2\ \text{V}$$

The point of saturation under ac conditions is determined as follows:

$$V_{ce(sat)} \cong 0\ \text{V}$$

$$I_{c(sat)} = I_{CQ} + \frac{V_{CEQ}}{R_c}$$

The ac collector resistance is

$$R_c = R_C \parallel R_L = \frac{R_C R_L}{R_C + R_L} = \frac{(1\ \text{k}\Omega)(1.5\ \text{k}\Omega)}{2.5\ \text{k}\Omega} = 600\ \Omega$$

Thus,

$$I_{c(sat)} = 5.3\text{ mA} + \frac{2.2\text{ V}}{600\ \Omega} = 5.3\text{ mA} + 3.67\text{ mA} = 8.97\text{ mA}$$

The point of cutoff under ac conditions is determined as follows:

$$I_{c(cutoff)} = 0\text{ A}$$
$$V_{ce(cutoff)} = V_{CEQ} + I_{CQ}R_c = 2.2\text{ V} + (5.3\text{ mA})(600\ \Omega) = 5.38\text{ V}$$

These results show that the collector current can swing up to almost 8.97 mA or the collector-to-emitter voltage can swing up to almost 5.38 V without the peaks being clipped due to saturation or cutoff.

Related Exercise Determine I_c and V_{ce} at the points of saturation and cutoff in Figure 7–10 for the following circuit values: $V_{CC} = 15$ V and $\beta_{ac} = 150$.

As described earlier, a centered Q-point allows a maximum unclipped output swing. A closer look at Example 7–1 shows that the Q-point is not centered, and therefore, the unclipped output swing is somewhat less than it could be if the Q-point were centered on the ac load line. This is examined further in Example 7–2.

EXAMPLE 7–2

Figure 7–11 shows the ac load line for the circuit in Example 7–1. Notice that the Q-point is *not* centered. The maximum output swings are

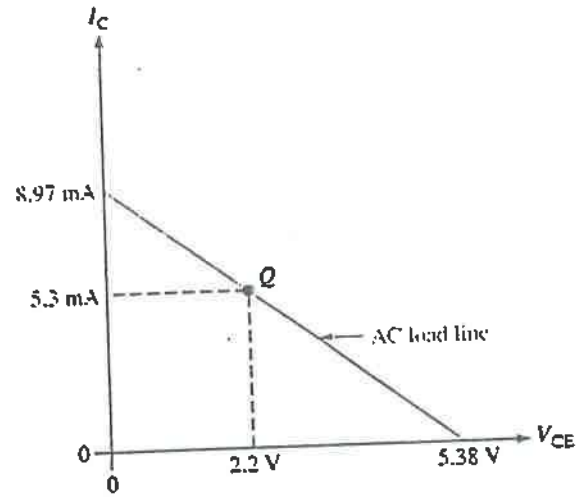
$$\Delta I_C = I_{c(sat)} - I_{CQ} = 8.97\text{ mA} - 5.3\text{ mA} = 3.67\text{ mA}$$

and

$$\Delta V_{CE} = V_{CEQ} = 2.2\text{ V}$$

Determine the maximum output swings for collector current and collector-to-emitter voltage when the Q-point is centered, assuming the same load line is maintained.

FIGURE 7–11



Solution The maximum output swings for a centered Q-point are

$$\Delta I_C = I_{CQ} = \frac{I_{c(sat)}}{2} = \frac{8.97\text{ mA}}{2} = 4.49\text{ mA}$$

$$\Delta V_{CE} = V_{CEQ} = \frac{V_{ce(cutoff)}}{2} = \frac{5.38\text{ V}}{2} = 2.69\text{ V}$$

Related Exercise Explain what happens to the output voltage if the Q-point is shifted to $V_{CE} = 3$ V.

Centering the Q-Point on the AC Load Line

To have a centered Q-point on the ac load line in Figure 7–9, V_{CEQ} must be midway between zero and the lower (cutoff) end of the ac load line, expressed as

$$V_{CEQ} = \frac{V_{CEQ} + I_{CQ}R_c}{2}$$

I_{CQ} must be midway between zero and the upper saturation end of the ac load line, expressed as

$$I_{CQ} = \frac{I_{CQ} + V_{CEQ}/R_c}{2}$$

The condition for a centered Q-point is developed as follows using the preceding equation for V_{CEQ}:

$$2V_{CEQ} = V_{CEQ} + I_{CQ}R_c$$

$$2V_{CEQ} - V_{CEQ} = I_{CQ}R_c$$

$$V_{CEQ} = I_{CQ}R_c \tag{7–3}$$

The Q-point can be moved to an approximate center position on the load line by changing I_{CQ} until both sides of Equation (7–3) are approximately equal.

To move the Q-point toward cutoff on the ac load line without affecting the load line itself, I_{CQ} should be decreased by increasing R_E. To move the Q-point toward saturation on the load line, I_{CQ} should be increased by decreasing R_E.

EXAMPLE 7–3 As you saw in Example 7–2, the circuit in Figure 7–10 does *not* have a centered Q-point. Select a value for R_E that will produce a Q-point that is approximately centered on the ac load line.

Solution You know from Example 7–2 that the collector current for a centered Q-point should be 4.49 mA. $R_c = 600\ \Omega$ from Example 7–1.

$$I_{CQ}R_c = (4.49\text{ mA})(600\ \Omega) = 2.69\text{ V}$$

Determine R_E by the following steps:

$$V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E)$$
$$= V_{CC} - I_{CQ}R_C - I_{CQ}R_E$$

Transpose terms:

$$V_{CEQ} - V_{CC} + I_{CQ}R_C = -I_{CQ}R_E$$

Then,

$$I_{CQ}R_E = V_{CC} - V_{CEQ} - I_{CQ}R_C$$
$$R_E = \frac{V_{CC} - V_{CEQ} - I_{CQ}R_C}{I_{CQ}} = \frac{10\text{ V} - 2.69\text{ V} - (4.49\text{ mA})(1\text{ k}\Omega)}{4.49\text{ mA}} = 628\ \Omega$$

Choose the nearest standard value:

$$R_E = 620\ \Omega$$

This will produce an approximately centered Q-point.

Related Exercise If R_C in Figure 7–10 is increased to 1.2 kΩ, what should you do to R_E to keep a centered Q-point?

Voltage Gain

The voltage gain of a class A large-signal amplifier is determined in the same way as for a small-signal amplifier with the exception that the formula $r'_e \cong 25\text{ mV}/I_E$ is not valid for the large-signal amplifier. This is because the signal swings over a large portion of the transconductance curve. Since $r'_e = \Delta V_{BE}/\Delta I_C$, the value is different for large-signal operation than it is for small-signal conditions because of the nonlinearity of the curve.

The large-signal ac emitter resistance, r'_e, can be determined graphically from the transconductance curve, as shown in Figure 7–12, using the relationship in Equation (7–4):

$$r'_e = \frac{\Delta V_{BE}}{\Delta I_C} \tag{7–4}$$

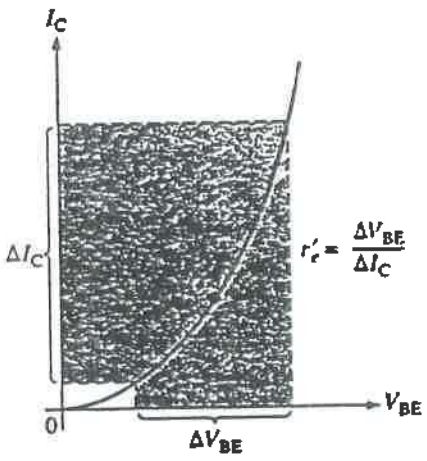


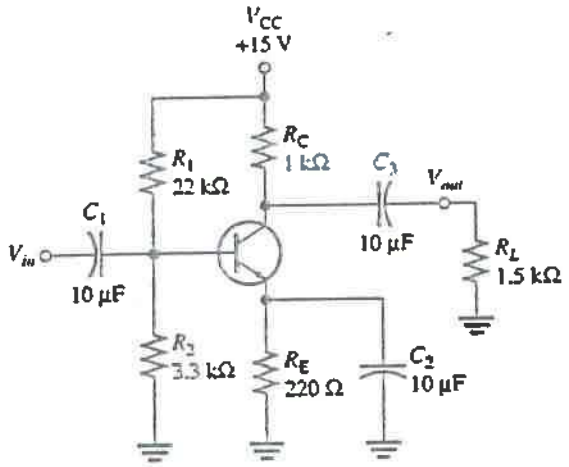
FIGURE 7–12
Determination of r'_e from the transconductance curve.

The voltage-gain formula for a common-emitter, large-signal amplifier with R_E completely bypassed is

$$A_v = \frac{R_c}{r'_e} \tag{7–5}$$

EXAMPLE 7–4 Find the large-signal voltage gain of the amplifier in Figure 7–13. Assume that r'_e has been found to be 8 Ω from graphical data.

FIGURE 7–13



Solution

$$R_c = \frac{(R_C)(R_L)}{R_C + R_L} = \frac{(1\text{ k}\Omega)(1.5\text{ k}\Omega)}{2.5\text{ k}\Omega} = 600\ \Omega$$

$$A_v = \frac{R_c}{r'_e} = \frac{600\ \Omega}{8\ \Omega} = 75$$

Related Exercise Find the large-signal voltage gain of the amplifier in Figure 7–13 if the supply voltage is changed to 9 V. R_L is changed to 1 kΩ, and r'_e is 10 Ω.

Distortion

When the collector current swings over a large portion of the transconductance curve, distortion can occur on the negative half-cycle because of the greater nonlinearity on the lower end of the curve, as shown in Figure 7–14. Distortion can be sufficiently reduced by keeping the collector current on the more linear part of the curve (at higher values of I_{CQ} and V_{BEQ}). Increasing the base bias voltage will result in more collector current and an increase in V_{BE} due to more voltage drop across r'_e.

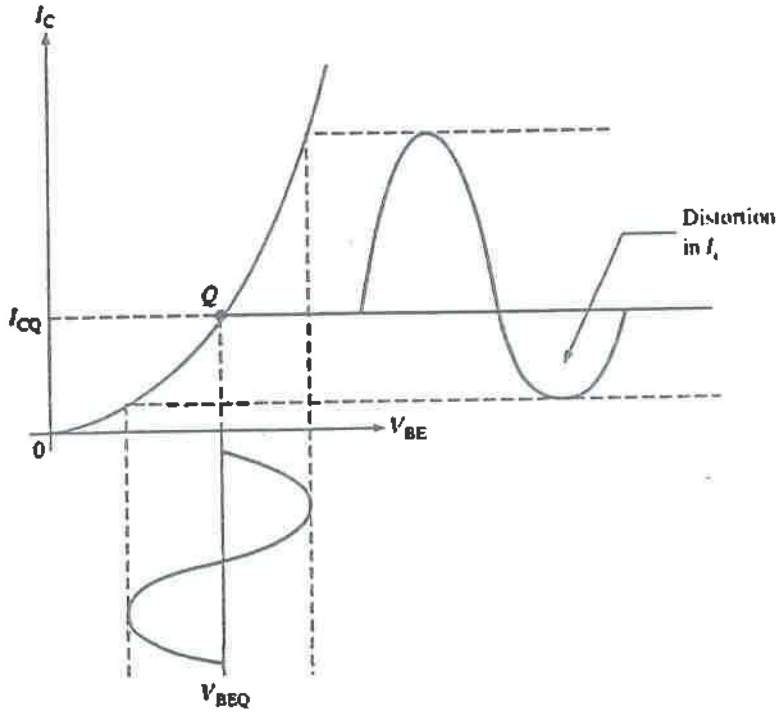


FIGURE 7–14
Example of distortion.

Power Gain

The main purpose of a large-signal amplifier is to achieve power gain. If we assume that the large-signal current gain, A_i, is approximately equal to β_{DC}, then the power gain, A_p, for a common-emitter amplifier is

$$A_p = A_i A_v = \beta_{DC} A_v$$

$$A_p = \beta_{DC}\left(\frac{R_c}{r'_e}\right) \tag{7–6}$$

Quiescent Power

The power dissipation of a transistor with no signal input is the product of its Q-point current and voltage.

$$P_{DQ} = I_{CQ} V_{CEQ} \tag{7–7}$$

The quiescent power is the maximum power that the class A transistor must handle; therefore, its power rating should exceed this value.

Output Power

In general, for any Q-point location on the ac load line, the output power of a common-emitter amplifier is the product of the rms collector current and the rms collector-to-emitter voltage.

$$P_{out} = V_{ce} I_c$$

Let's now consider the output power for three cases of Q-point location.

Q-Point Closer to Saturation When the Q-point is closer to saturation, the maximum collector-to-emitter voltage swing is V_{CEQ}, and the maximum collector current swing is V_{CEQ}/R_c, as shown in Figure 7–15(a). The ac output power is, therefore,

$$P_{out} = \left(\frac{0.707 V_{CEQ}}{R_c}\right) 0.707 V_{CEQ}$$

$$P_{out} = \frac{0.5 V_{CEQ}^2}{R_c} \tag{7–8}$$

where $R_c = R_C \parallel R_L$.

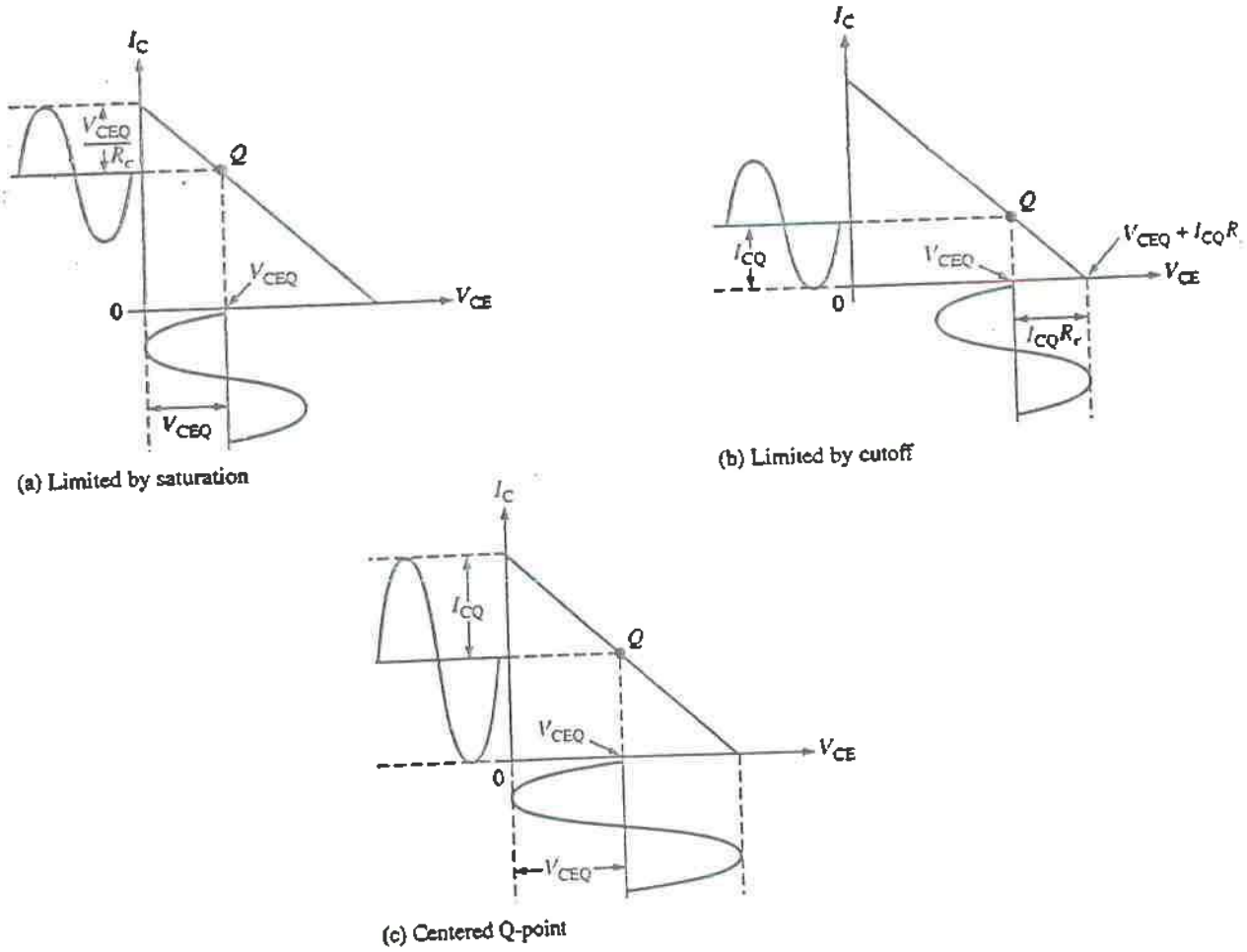


FIGURE 7–15
AC load line operation showing limitations of output voltage swings.

Q-Point Closer to Cutoff When the Q-point is closer to cutoff, the maximum collector current swing is I_{CQ}, and the collector-to-emitter voltage swing is $I_{CQ}R_c$, as shown in Figure 7–15(b). The ac output power is, therefore,

$$P_{out} = (0.707I_{CQ})(0.707I_{CQ}R_c)$$

$$P_{out} = 0.5I_{CQ}^2R_c \tag{7–9}$$

Q-Point Centered When the Q-point is centered, the maximum collector current swing is I_{CQ}, and the maximum collector-to-emitter voltage swing is V_{CEQ}, as shown in Figure 7–15(c). The ac output power is, therefore,

$$P_{out} = (0.707V_{CEQ})(0.707I_{CQ})$$

$$P_{out} = 0.5V_{CEQ}I_{CQ} \tag{7–10}$$

This is the maximum ac output power from a class A amplifier under signal conditions. Notice that it is one-half the quiescent power dissipation.

Efficiency

Efficiency (η) of an amplifier is the ratio of ac output power to dc input power. The dc input power is the dc supply voltage times the current drawn from the supply.

$$P_{DC} = V_{CC}I_{CC}$$

The average supply current I_{CC} equals I_{CQ}, and the supply voltage V_{CC} is twice V_{CEQ} when the Q-point is centered. The maximum efficiency is therefore

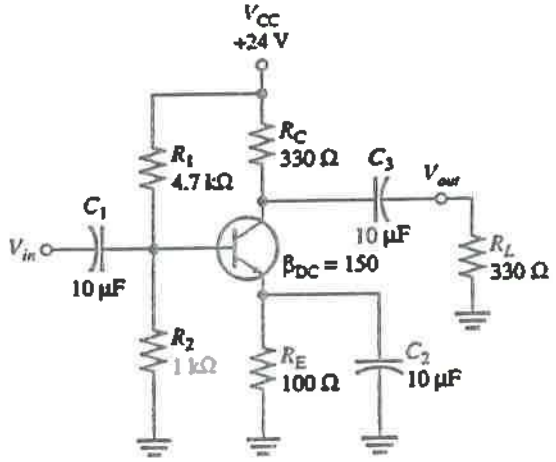
$$\eta_{max} = \frac{P_{out}}{P_{DC}} = \frac{0.5V_{CEQ}I_{CQ}}{V_{CC}I_{CC}} = \frac{0.5V_{CEQ}I_{CQ}}{2V_{CEQ}I_{CQ}} = \frac{0.5}{2}$$

$$\eta_{max} = 0.25 \tag{7–11}$$

Thus, 0.25 or 25 percent is the highest possible efficiency available from a class A amplifier and is approached only when the Q-point is at the center of the ac load line.

EXAMPLE 7–5 Determine the following values for the amplifier in Figure 7–16 when operated with the maximum possible output signal:
(a) Minimum transistor power rating
(b) AC output power
(c) Efficiency

FIGURE 7–16



Solution First determine the dc values. Neglect $R_{IN(base)}$.

$$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{1\text{ k}\Omega}{5.7\text{ k}\Omega}\right)24\text{ V} = 4.2\text{ V}$$

Then

$$V_E = V_B - V_{BE} = 4.2\text{ V} - 0.7\text{ V} = 3.5\text{ V}$$

$$I_E = \frac{V_E}{R_E} = \frac{3.5\text{ V}}{100\ \Omega} = 35\text{ mA}$$

Therefore, the collector current at the Q-point is

$$I_{CQ} \cong 35\text{ mA}$$

and

$$V_C = V_{CC} - I_{CQ}R_C = 24\text{ V} - (35\text{ mA})(330\ \Omega) = 12.5\text{ V}$$

$$V_{CEQ} = V_C - V_E = 12.5\text{ V} - 3.5\text{ V} = 9.0\text{ V}$$

(a) The transistor power rating must be greater than

$$P_D = V_{CEQ}I_{CQ} = (9.0\text{ V})(35\text{ mA}) = 315\text{ mW}$$

(b) To make a calculation of ac output power under a *maximum* signal condition, you must know the location of the Q-point relative to the center. This will tell you whether I_{CQ} or V_{CEQ} is the limiting factor if the Q-point is not centered. The ac load line values are as follows:

$$R_c = R_C \parallel R_L = 330\ \Omega \parallel 330\ \Omega = 165\ \Omega$$

$$I_{c(sat)} = I_{CQ} + \frac{V_{CEQ}}{R_c} = 35\text{ mA} + \frac{9.0\text{ V}}{165\ \Omega} = 89.5\text{ mA}$$

and

$$V_{ce(cutoff)} = V_{CEQ} + I_{CQ}R_c = 9.0\text{ V} + (35\text{ mA})(165\ \Omega) = 14.8\text{ V}$$

A *centered* Q-point is at

$$I_{CQ} = \frac{89.5\text{ mA}}{2} = 44.8\text{ mA}$$

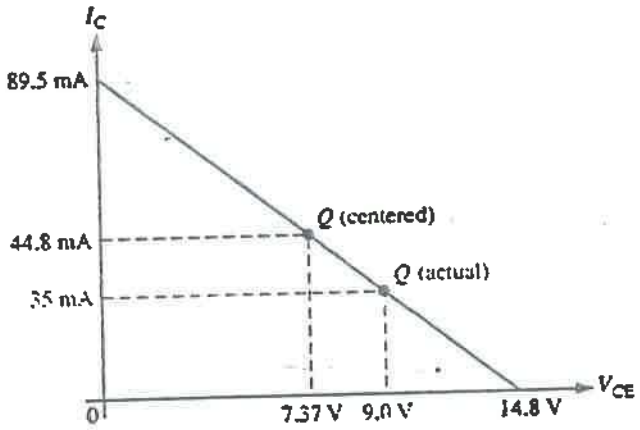
and

$$V_{CEQ} = \frac{14.8\text{ V}}{2} = 7.37\text{ V}$$

These Q-point values are shown on the ac load line in Figure 7–17. The *actual* Q-point for this amplifier is closer to cutoff, as shown in the figure. Therefore, the maximum collector current swing is I_{CQ}, and the ac output power is

$$P_{out} = 0.5I_{CQ}^2 R_c = 0.5(35\text{ mA})^2(165\ \Omega) = 101\text{ mW}$$

FIGURE 7–17



(c) The efficiency is

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{P_{out}}{V_{CC}I_{CC}} = \frac{P_{out}}{V_{CC}I_{CQ}} = \frac{101\text{ mW}}{(24\text{ V})(35\text{ mA})} = 0.12$$

This efficiency of 12 percent is considerably less than the maximum possible efficiency (25 percent) because the actual Q-point is not centered.

Related Exercise Suggest ways to increase the efficiency of the amplifier in Figure 7–16.

Maximum Load Power

The maximum power to the load in a class A amplifier occurs when the Q-point is centered, as you can see in Figure 7–15(c). The maximum peak load voltage equals V_{CEQ}, assuming a negligible voltage drop across the output coupling capacitor.

$$P_L = \frac{V_L^2}{R_L} = \frac{(0.707V_{CEQ})^2}{R_L}$$

$$P_L = \frac{0.5V_{CEQ}^2}{R_L} \qquad (7\text{–}12)$$

Sometimes the load power is defined as the output power.

EXAMPLE 7–6 Determine the maximum load power for the amplifier in Example 7–5.

Solution When the Q-point is centered, $V_{CEQ} = 7.37$ V.

$$P_{L(max)} = \frac{0.5V_{CEQ}^2}{R_L} = \frac{0.5(7.37\text{ V})^2}{330\ \Omega} = 82.3\text{ mW}$$

Related Exercise If the Q-point in the amplifier is shifted to $V_{CEQ} = 5$ V, what is the load power?

SECTION 7–1 REVIEW

1. Why does the ac load line differ from the dc load line?
2. What is the optimum Q-point location for class A amplifiers?
3. What is the maximum efficiency of a class A amplifier?
4. How do you approach maximum efficiency in a class A amplifier?

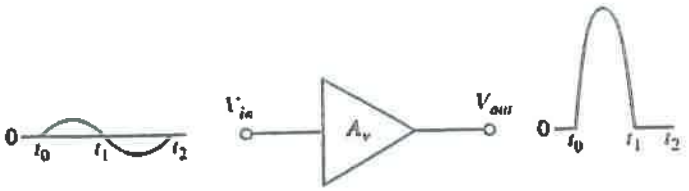
7–2 ■ CLASS B AND CLASS AB PUSH-PULL AMPLIFIERS

When an amplifier is biased at cutoff such that it operates in the linear region for 180° of the input cycle and is in cutoff for 180°, it is a class B amplifier. Class AB amplifiers are biased to conduct for slightly more than 180°. The primary advantage of a class B or class AB amplifier over a class A amplifier is that they are more efficient; you can get more output power for a given amount of input power. A disadvantage of class B or class AB is that it is more difficult to implement the circuit in order to get a linear reproduction of the input waveform. As you will see in this section, the term push-pull refers to a common type of class B or class AB amplifier circuit in which the input wave shape is reproduced at the output.

After completing this section, you should be able to

- Explain and analyze the operation of class B and class AB amplifiers
  - ☐ Explain class B operation
  - ☐ Discuss Q-point location for class B
  - ☐ Describe class B push-pull operation
  - ☐ Explain crossover distortion and its cause
  - ☐ Explain class AB operation
  - ☐ Analyze class AB push-pull amplifiers
  - ☐ Calculate maximum output power
  - ☐ Calculate dc input power
  - ☐ Determine class B maximum efficiency
  - ☐ Find the input resistance
  - ☐ Analyze a darlington push-pull amplifier
  - ☐ Discuss methods of driving a push-pull amplifier

FIGURE 7–18
Basic class B amplifier operation (noninverting).



Class B Operation

The class B operation is illustrated in Figure 7–18, where the output waveform is shown relative to the input.

The Q-Point Is at Cutoff The class B amplifier is biased at the cutoff point so that $I_{CQ} = 0$ and $V_{CEQ} = V_{CE(cutoff)}$. It is brought out of cutoff and operates in its linear region when the input signal drives it into conduction. This is illustrated in Figure 7–19 with an emitter-follower circuit. Obviously, the output is not a replica of the input. Therefore, a two-transistor configuration, known as a **push-pull** amplifier, is necessary to get a sufficiently good reproduction of the input waveform.

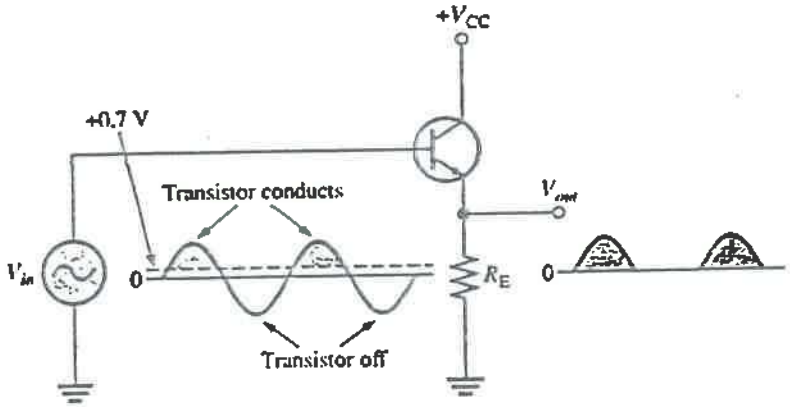


FIGURE 7–19
Common-collector class B amplifier.

Push-Pull Class B Operation Figure 7–20 shows one type of push-pull class B amplifier using two emitter-followers. This is called a complementary amplifier because one emitter-follower uses an *npn* transistor and the other a matched *pnp;* the transistors conduct on *opposite* alternations of the input cycle. A matched **complementary pair** of transistors have identical characteristics, except one is an *npn* and the other a *pnp*. The 2N3904 and 2N3906 are examples. Notice that there is no dc base bias voltage ($V_B = 0$); thus, only the signal voltage drives the transistors into conduction. Q_1 conducts during the positive half of the input cycle, and Q_2 conducts during the negative half.

Crossover Distortion When the dc base voltage is zero, both transistors are off and the input signal voltage must exceed V_{BE} before a transistor conducts. Because of this, there is a time interval between the positive and negative alternations of the input when neither transistor is conducting, as shown in Figure 7–21. The resulting distortion in the output waveform is quite common and is called **crossover distortion.**

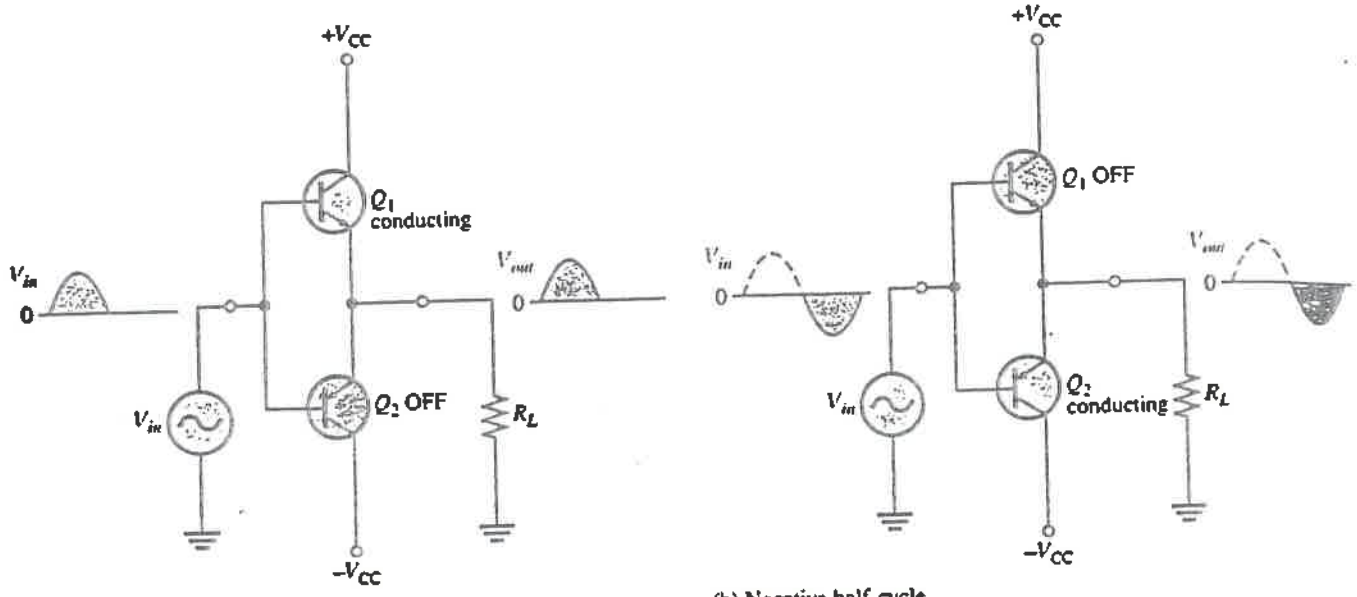


FIGURE 7–20
Class B push-pull ac operation.

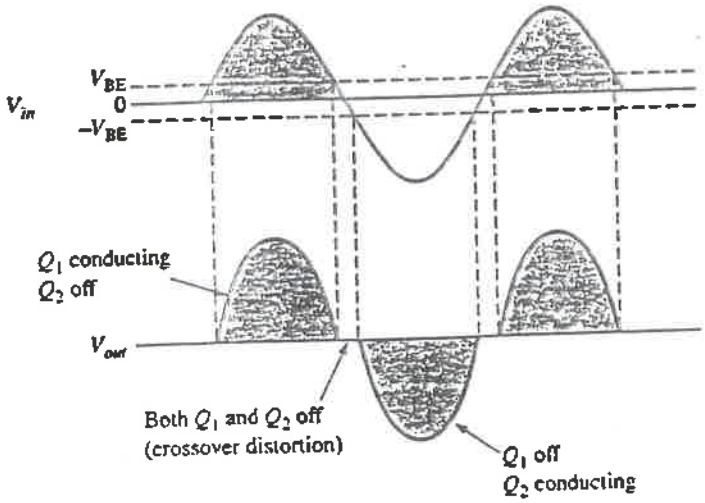
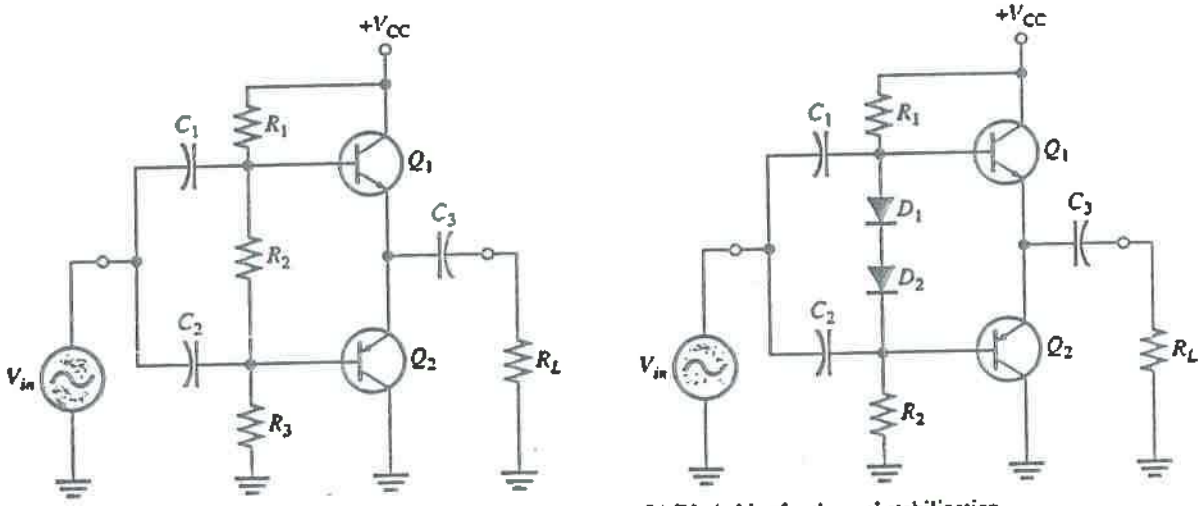


FIGURE 7–21
Illustration of crossover distortion in a class B push-pull amplifier. The transistors conduct only during portions of the input indicated by the shaded areas.

Class AB Operation

To eliminate crossover distortion, both transistors in the push-pull arrangement must be biased slightly above cutoff when there is no signal. This variation of the class B push-pull amplifier is designated as class AB. Class AB biasing can be done with a voltage-divider arrangement, as shown in Figure 7–22(a). It is, however, difficult to maintain a stable bias point with this circuit due to changes in V_{BE} over temperature changes. (The requirement for dual-polarity power supplies is eliminated when R_L is capacitively cou-



(a) Voltage-divider bias

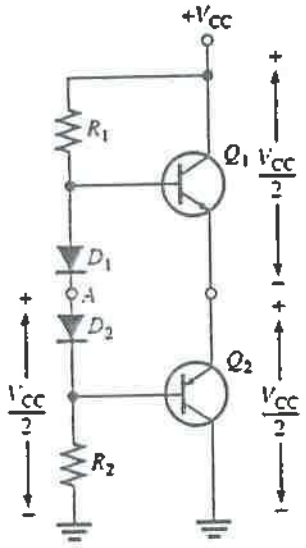
(b) Diode bias for thermal stabilization

FIGURE 7–22
Biasing the push-pull amplifier for class AB operation to eliminate crossover distortion.

pled.) A more suitable arrangement is shown in Figure 7–22(b). When the diode characteristics of D_1 and D_2 are closely matched to the transconductance characteristics of the transistors, a stable bias over temperature can be maintained. This stabilization can also be accomplished by using the base-emitter junctions of two additional matched transistors instead of D_1 and D_2. Although technically incorrect, class AB amplifiers are often referred to as class B in common practice.

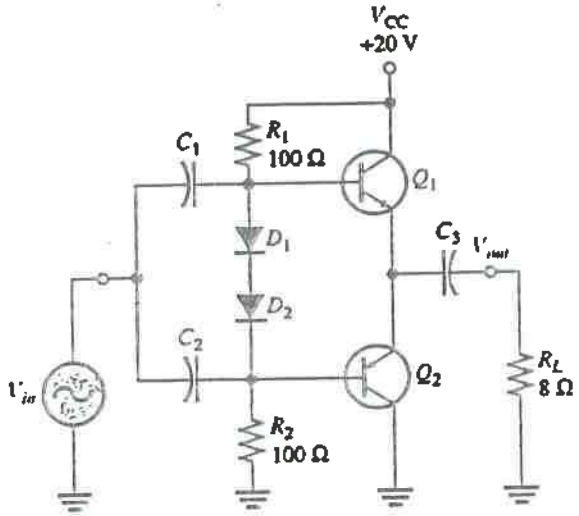
The dc equivalent circuit of the push-pull amplifier is shown in Figure 7–23. Resistors R_1 and R_2 are of equal value; therefore the voltage at point A between the two diodes is $V_{CC}/2$. Assuming that both diodes and both transistors are identical, the drop across D_1 equals the V_{BE} of Q_1, and the drop across D_2 equals the V_{BE} of Q_2. As a result, the voltage at the emitters is also $V_{CC}/2$, and therefore, $V_{CEQ1} = V_{CEQ2} = V_{CC}/2$, as indicated. Because both transistors are biased near cutoff, $I_{CQ} \cong 0$.

FIGURE 7–23
DC equivalent of push-pull amplifier.



EXAMPLE 7–7 Determine the dc voltages at the bases and emitters of the matched complementary transistors Q_1 and Q_2 in Figure 7–24. Also determine V_{CEQ} for each transistor. Assume $V_{D1} = V_{D2} = V_{BE} = 0.7$ V.

FIGURE 7–24



Solution The equivalent for the bias circuit is shown in Figure 7–25(a).

$$I_T = \frac{V_{CC} - V_{D1} - V_{D2}}{R_1 + R_2} = \frac{20\text{ V} - 1.4\text{ V}}{200\ \Omega} = 93\text{ mA}$$

$$V_{B1} = V_{CC} - I_T R_1 = 20\text{ V} - (93\text{ mA})(100\ \Omega) = 10.7\text{ V}$$

and

$$V_{B2} = V_{B1} - V_{D1} - V_{D2} = 10.7\text{ V} - 1.4\text{ V} = 9.3\text{ V}$$

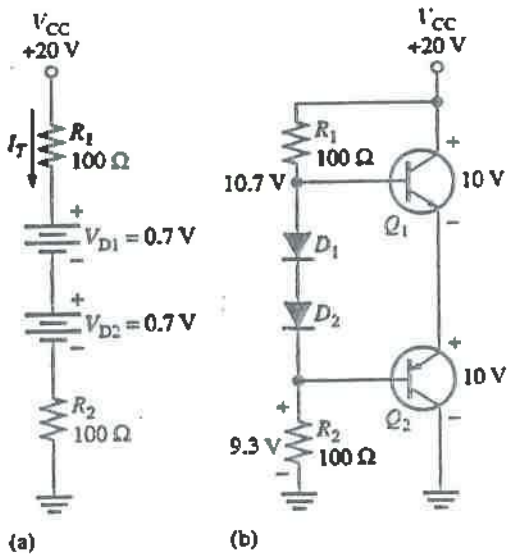
$$V_{E1} = V_{E2} = 10.7\text{ V} - 0.7\text{ V} = 10\text{ V}$$

Therefore,

$$V_{CEQ1} = V_{CEQ2} = \frac{V_{CC}}{2} = \frac{20\text{ V}}{2} = 10\text{ V}$$

These values are shown in Figure 7–25(b).

FIGURE 7–25



Related Exercise If R_1 and R_2 are changed to 220 Ω. what are the base and emitter voltages in Figure 7–24?

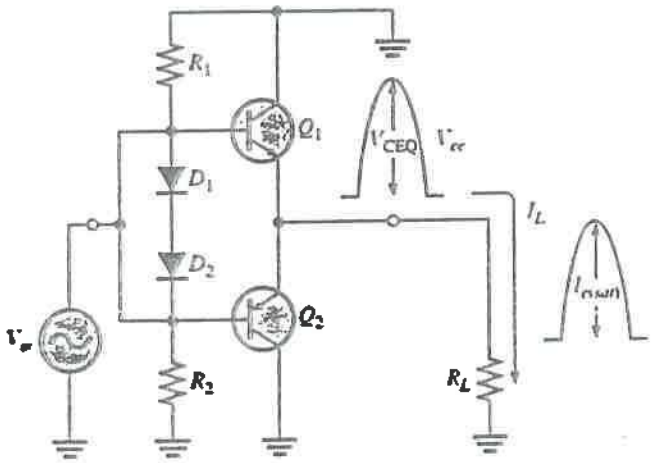
AC Operation Under maximum conditions, transistors Q_1 and Q_2 in a class AB amplifier are alternately driven from near cutoff to near saturation. During the positive alternation of the input signal, the Q_1 emitter is driven from its Q-point value of $V_{CC}/2$ to near V_{CC}, producing a positive peak voltage approximately equal to V_{CEQ}. At the same time, the Q_1 current swings from its Q-point value near zero to near-saturation value, as shown in Figure 7–26(a).

During the negative alternation of the input signal, the Q_2 emitter is driven from its Q-point value of $V_{CC}/2$ to near zero, producing a negative peak voltage approximately equal to V_{CEQ}. Also, the Q_2 current swings from near zero to near-saturation value, as shown in Figure 7–26(b).

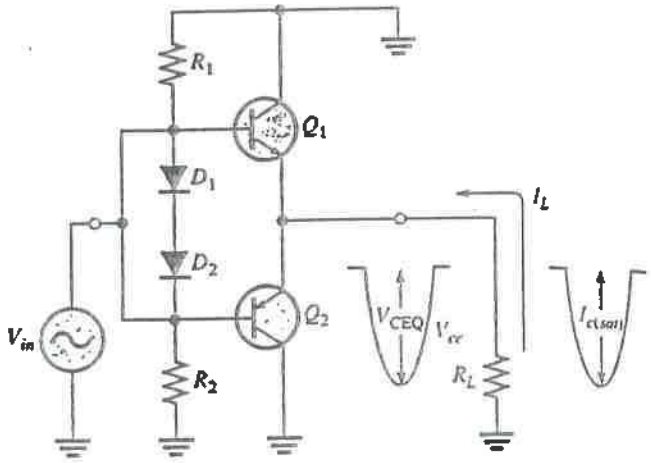
In terms of the ac load line operation, the V_{ce} of both transistors swings from $V_{CC}/2$ to near zero, and the current swings from zero to $I_{c(sat)}$, as shown in Figure 7–26(c). Because the peak voltage across each transistor is V_{CEQ}, the ac collector saturation current is

$$I_{c(sat)} = \frac{V_{CEQ}}{R_L} \tag{7–13}$$

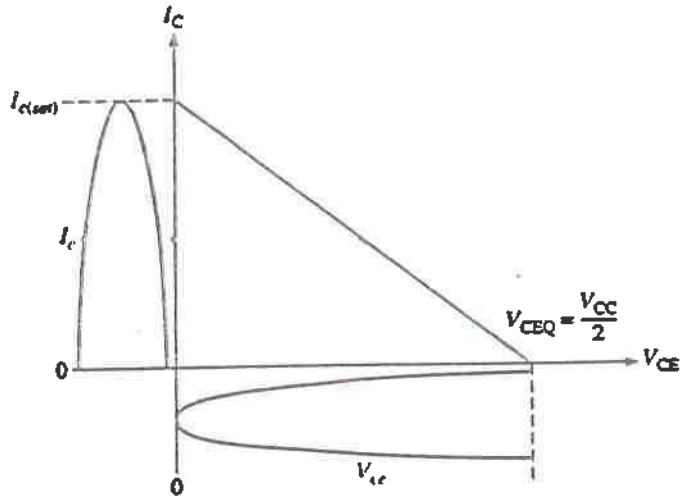
Since $I_e \equiv I_c$ and the output current is the emitter current, the peak output current is also V_{CEQ}/R_L.



(a) Q_1 conducting with maximum signal output



(b) Q_2 conducting with maximum signal output

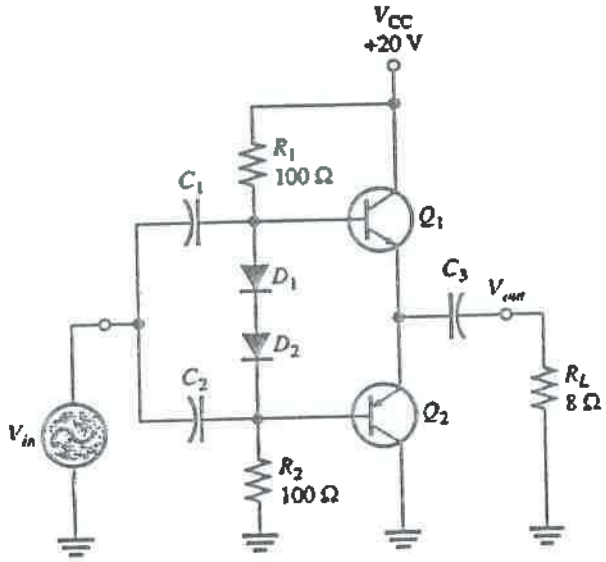


(c) AC load line for each transistor

FIGURE 7–26
Ideal ac push-pull operation for maximum signal operation.

EXAMPLE 7–8 Determine the maximum ideal peak values for the output voltage and current in Figure 7–27.

FIGURE 7–27



Solution The maximum peak output voltage is

$$V_{out(peak)} \cong V_{CEQ} = \frac{V_{CC}}{2} = \frac{20\text{ V}}{2} = 10\text{ V}$$

The maximum peak output current is

$$I_{out(peak)} \cong I_{c(sat)} = \frac{V_{CEQ}}{R_L} = \frac{10\text{ V}}{8\ \Omega} = 1.25\text{ A}$$

Related Exercise Find the maximum peak values for the output voltage and current in Figure 7–27 if V_{CC} is lowered to 15 V and the load resistance is changed to 16 Ω.

Maximum Output Power It has been shown that the maximum peak output current is approximately $I_{c(sat)}$, and the maximum peak output voltage is approximately V_{CEQ}. The maximum average output power is, therefore,

$$P_{out} = V_{out(rms)}I_{out(rms)}$$

Since

$$V_{out(rms)} = 0.707V_{out(peak)} = 0.707V_{CEQ}$$

and

$$I_{out(rms)} = 0.707I_{out(peak)} = 0.707I_{c(sat)}$$

then

$$P_{out} = 0.5V_{CEQ}I_{c(sat)}$$

Substituting $V_{CC}/2$ for V_{CEQ}, you get

$$P_{out} = 0.25V_{CC}I_{c(sat)} \tag{7–14}$$

DC Input Power The dc input power comes from the V_{CC} supply and is

$$P_{DC} = V_{CC}I_{CC}$$

Since each transistor draws current for a half-cycle, the current is a half-wave signal with an average of

$$I_{CC} = \frac{I_{c(sat)}}{\pi} \tag{7–15}$$

So,

$$P_{DC} = \frac{V_{CC}I_{c(sat)}}{\pi} \tag{7–16}$$

Efficiency An advantage of push-pull class B and class AB amplifiers over class A is a much higher efficiency. This advantage usually overrides the difficulty of biasing the class AB push-pull amplifier to eliminate crossover distortion. Recall that efficiency is defined as the ratio of ac output power to dc input power.

$$\text{Efficiency} = \frac{P_{out}}{P_{DC}}$$

The maximum efficiency for a class B amplifier (class AB is slightly less) is designated η_{max} and is developed as follows, starting with Equation (7–14).

$$P_{out} = 0.25V_{CC}I_{c(sat)}$$

$$\eta_{max} = \frac{P_{out}}{P_{DC}} = \frac{0.25V_{CC}I_{c(sat)}}{V_{CC}I_{c(sat)}/\pi} = 0.25\pi$$

$$\eta_{max} = 0.79 \tag{7–17}$$

or, as a percentage

$$\eta_{max} = 79\%$$

Recall that the maximum efficiency for class A is 0.25 (25 percent).

Input Resistance The complementary push-pull configuration used in class B/class AB amplifiers is, in effect, two emitter-followers. The input resistance is, therefore, the same as developed in Chapter 6 for the emitter-follower:

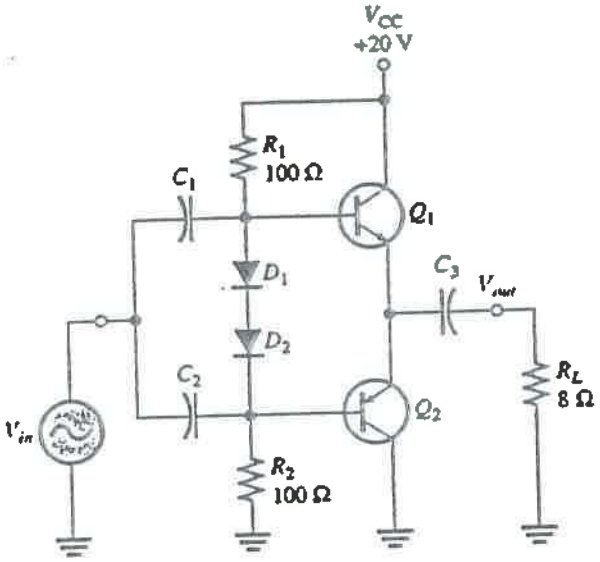
$$R_{in} = \beta_{ac}(r'_e + R_E)$$

Since $R_E = R_L$, the formula is

$$R_{in} = \beta_{ac}(r'_e + R_L) \tag{7–18}$$

EXAMPLE 7–9 Find the maximum ac output power and the dc input power of the amplifier in Figure 7–28. Also, determine the input resistance assuming $\beta_{ac} = 50$ and $r'_e = 6\ \Omega$.

FIGURE 7–28



Solution $I_{c(sat)}$ for this same circuit was found to be 1.25 A in Example 7–8.

$$P_{out} = 0.25 V_{CC} I_{c(sat)} = 0.25(20\text{ V})(1.25\text{ A}) = 6.25\text{ W}$$

$$P_{DC} = \frac{V_{CC} I_{c(sat)}}{\pi} = \frac{(20\text{ V})(1.25\text{ A})}{\pi} = 7.96\text{ W}$$

$$R_{in} = \beta_{ac}(r'_e + R_L) = 50(6\ \Omega + 8\ \Omega) = 700\ \Omega$$

Related Exercise Determine the maximum ac output power and the dc input power in Figure 7–28 for $V_{CC} = 15$ V and $R_L = 16\ \Omega$.

Darlington Class AB Amplifier

In many applications where the push-pull configuration is used, the load resistance is relatively small. For example, an 8 Ω speaker is a common load for a class AB push-pull amplifier.

As a result of low-resistance loading, push-pull amplifiers generally present a quite low input resistance to the preceding amplifier that drives it. Depending on the output resistance of the preceding amplifier, the low push-pull input resistance can load it severely and significantly reduce the voltage gain. As an example, if the complementary transistors in a push-pull amplifier exhibit an ac beta of 50 and the load resistance is 8 Ω, the input resistance (assuming $r'_e = 5\ \Omega$) is

$$R_{in} = \beta_{ac}(r'_e + R_L) = 50(5\ \Omega + 8\ \Omega) = 650\ \Omega$$

If the output resistance of the driving amplifier is, for example, 1 kΩ, the input resistance of the push-pull amplifier reduces the effective collector resistance of the driving

amplifier (assuming a common-emitter) to $R_{out} \| R_{in} = 1\ \text{k}\Omega \| 650\ \Omega = 394\ \Omega$. This drastically reduces the voltage gain of the driving amplifier.

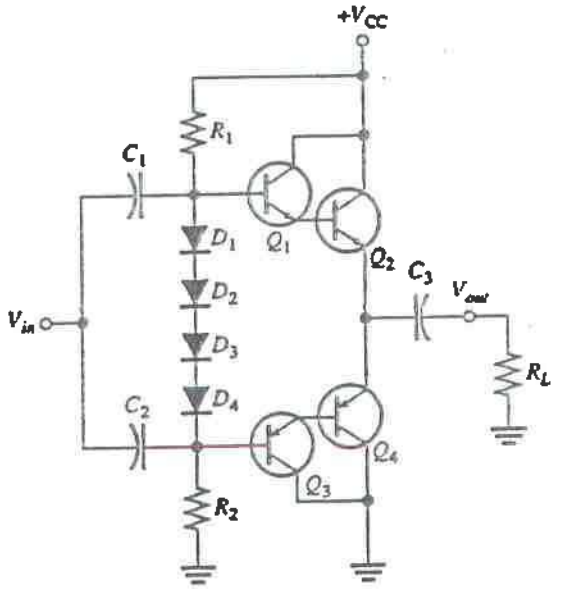
In certain applications with low-resistance loads, a push-pull amplifier using darlington transistors can be used to increase the input resistance presented to the driving amplifier and avoid severely reducing the voltage gain. The ac beta of a darlington pair is generally between a few hundred and several thousand.

In the previous case, for example, if $\beta_{ac} = 50$ for each transistor in a darlington pair, the overall ac beta is $\beta_{ac} = (50)(50) = 2500$. The input resistance is greatly increased, as the following calculation shows.

$$R_{in} = \beta_{ac}(r'_e + R_L) = 2500(5\ \Omega + 8\ \Omega) = 32.5\ \text{k}\Omega$$

A darlington class AB push-pull amplifier is shown in Figure 7–29. Four diodes are required in the bias circuit to match the four base-emitter junctions of the two darlington pairs.

FIGURE 7–29
A darlington class AB push-pull amplifier.

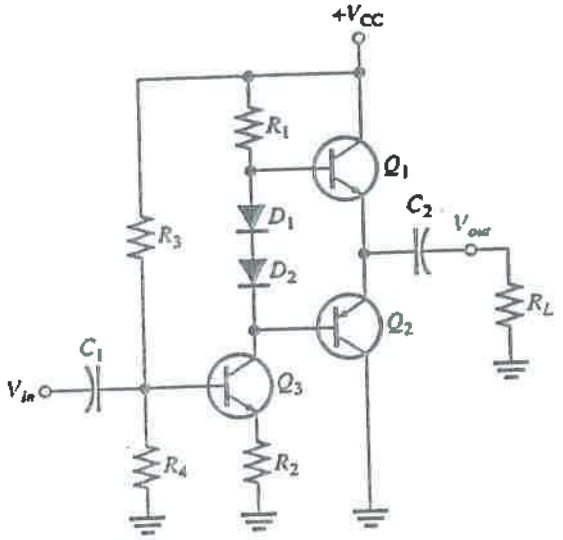


Push-Pull Amplifier with Class A Driver

Up to this point, the input signal to class B and class AB push-pull amplifiers has been capacitively coupled from the input source to each of the two transistors. Another method is to use a class A stage as the driver, as shown in Figure 7–30. As you can see, the driver is a voltage-divider-biased amplifier with a swamped emitter (no emitter-bypass capacitor).

The dc bias voltages for the push-pull amplifier are established by the dc collector current of the driver transistor Q_3. When an input signal is coupled to the base of Q_3, the resulting ac collector current of Q_3 produces signal voltages at the bases of Q_1 and Q_2, as shown in Figure 7–30. The ac voltage dropped across the dynamic resistances of the bias diodes is negligible, so the Q_1 and Q_2 base signals are essentially equal. The reason for this is that the dynamic resistances of the diodes are very small compared to R_1 and, for all practical purposes, the diodes can be considered shorts to the ac signal. This driver circuit has proved to be an effective way to interface the push-pull amplifier with a preamplifier circuit that precedes it.

FIGURE 7–30
A push-pull amplifier with a class A driver.



SECTION 7–2 REVIEW

1. Where is the Q-point for a class B amplifier?
2. What causes crossover distortion?
3. What is the maximum efficiency of a push-pull class B amplifier?
4. Explain the purpose of the push-pull configuration for class B.
5. How does a class AB differ from a class B amplifier?

7–3 ■ CLASS C AMPLIFIERS

Class C amplifiers are biased so that conduction occurs for much less than 180°. Class C amplifiers are more efficient than either class A or push-pull class B and class AB, which means that more output power can be obtained from class C operation. Because the output waveform is severely distorted, class C amplifiers are normally limited to applications as tuned amplifiers at radio frequencies (rf) as you will see in this section.

After completing this section, you should be able to

- Discuss and analyze the operation of class C amplifiers
  - ☐ Explain class C operation
  - ☐ Discuss class C power dissipation
  - ☐ Describe tuned operation
  - ☐ Calculate maximum output power
  - ☐ Determine efficiency
  - ☐ Explain clamper bias in a class C amplifier

Basic Class C Operation

The basic concept of class C operation is illustrated in Figure 7–31. A common-emitter class C amplifier with a resistive load is shown in Figure 7–32(a). It is biased below cut-off with the $-V_{BB}$ supply. The ac source voltage has a peak value that is slightly greater

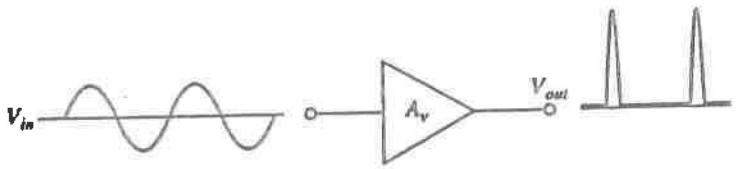


FIGURE 7–31
Basic class C amplifier operation (noninverting).

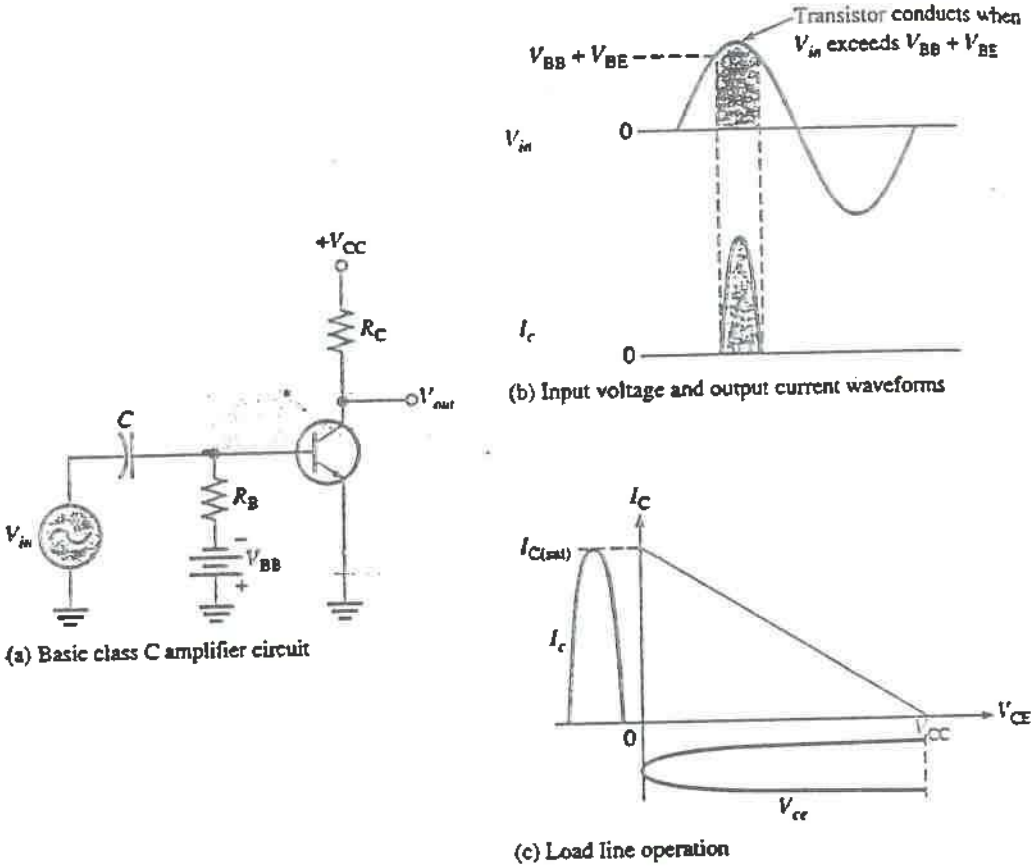


FIGURE 7–32
Basic class C operation.

than $V_{BB} + V_{BE}$ so that the base voltage exceeds the barrier potential of the base-emitter junction for a short time near the positive peak of each cycle, as illustrated in Figure 7–32(b). During this short interval, the transistor is turned on. When the entire ac load line is used, as shown in Figure 7–30(c), the ideal maximum collector current is approximately $I_{C(sat)}$, and the ideal minimum collector voltage is approximately $V_{CE(sat)}$.

Power Dissipation

The power dissipation of the transistor in a class C amplifier is low because it is on for only a small percentage of the input cycle. Figure 7–33(a) shows the collector current pulses. The time between the pulses is the period (T) of the ac input voltage. To avoid

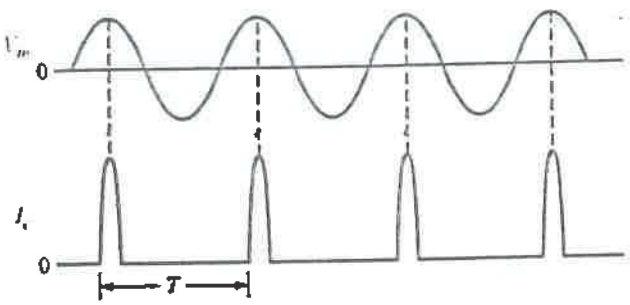
complex mathematics, we will use ideal pulse approximations for the collector current and the collector voltage during the *on* time of the transistor, as shown in Figure 7–33(b). Using this simplification, the maximum current amplitude is $I_{C(sat)}$ and the minimum voltage amplitude is $V_{CE(sat)}$ during the time the transistor is on, if the output swings over the entire load line. The power dissipation during the *on* time is, therefore,

$$P_{D(on)} = V_{CE(sat)} I_{C(sat)}$$

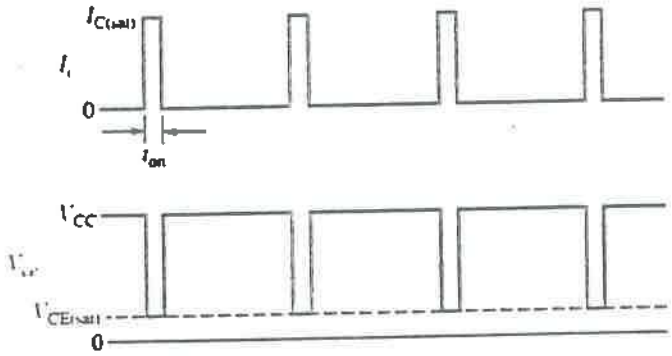
The transistor is on for a short time, t_{ON}, and off for the rest of the input cycle. Therefore, assuming the entire load line is used, the power dissipation averaged over the entire cycle is

$$P_{D(avg)} = \left(\frac{t_{ON}}{T}\right) P_{D(on)}$$

$$P_{D(avg)} = \left(\frac{t_{ON}}{T}\right) V_{CE(sat)} I_{C(sat)} \qquad (7\text{–}19)$$



(a) Collector current pulses



(b) Ideal class C waveforms

FIGURE 7–33
Class C waveforms.

EXAMPLE 7–10 A class C amplifier is driven by a 200 kHz signal. The transistor is on for 1 μs, and the amplifier is operating over 100 percent of its load line. If $I_{C(sat)} = 100$ mA and $V_{CE(sat)} = 0.2$ V, what is the average power dissipation?

Solution The period is

$$T = \frac{1}{200\text{ kHz}} = 5\ \mu\text{s}$$

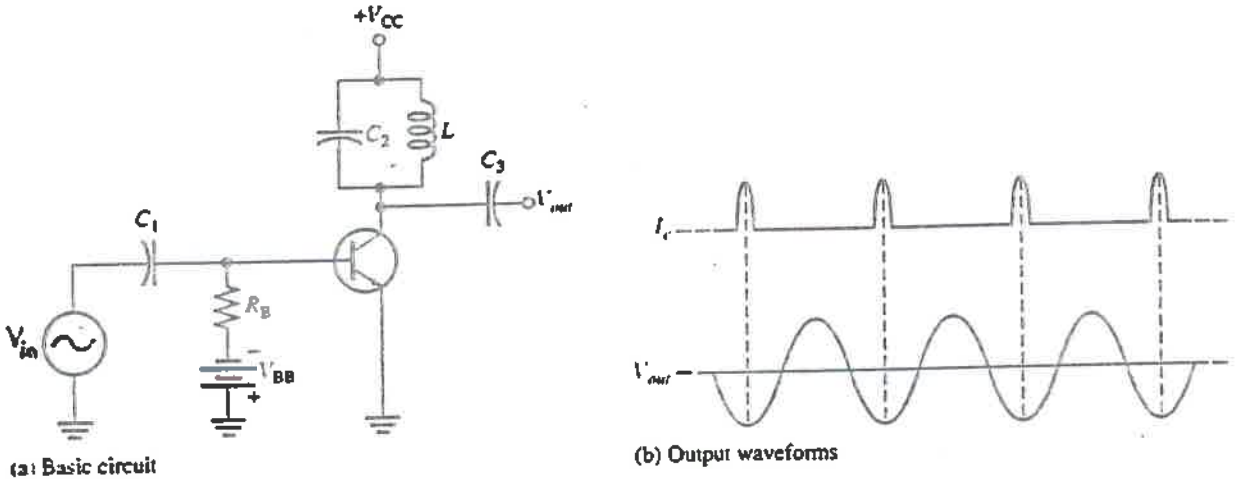
Therefore,

$$P_{D(avg)} = \left(\frac{t_{ON}}{T}\right) V_{CE(sat)} I_{C(sat)} = (0.2)(0.2\text{ V})(100\text{ mA}) = 4\text{ mW}$$

Related Exercise If the frequency is reduced from 200 kHz to 150 kHz, what is the average power dissipation?

Tuned Operation

Because the collector voltage (output) is not a replica of the input, the resistively loaded class C amplifier is of no value in linear applications. It is therefore necessary to use a class C amplifier with a parallel resonant circuit (tank), as shown in Figure 7–34(a). The resonant frequency of the tank circuit is determined by the formula $f_r = 1/(2\pi\sqrt{LC})$. The short pulse of collector current on each cycle of the input initiates and sustains the oscillation of the tank circuit so that an output sinusoidal voltage is produced, as illustrated in Figure 7–34(b).



(a) Basic circuit

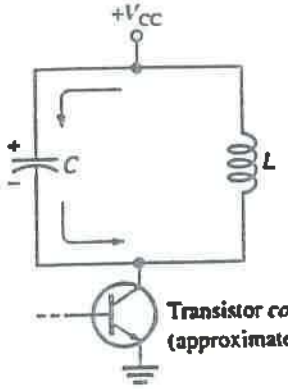
(b) Output waveforms

FIGURE 7–34
Tuned class C amplifier.

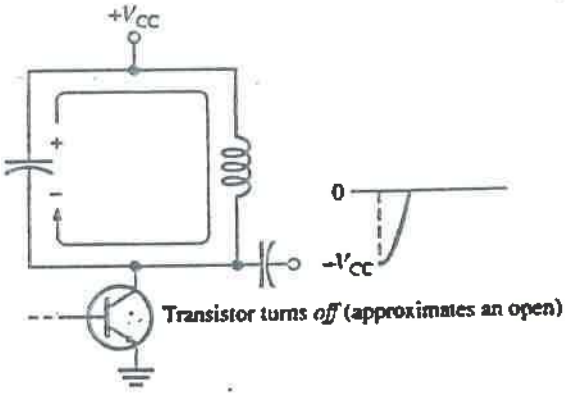
The current pulse charges the capacitor to approximately $+V_{CC}$, as shown in Figure 7–35(a). After the pulse, the capacitor quickly discharges, thus charging the inductor. Then, after the capacitor completely discharges, the inductor's magnetic field collapses and then quickly recharges C to near V_{CC} in a direction opposite to the previous charge. This completes one half-cycle of the oscillation, as shown in parts (b) and (c) of Figure 7–35. Next, the capacitor discharges again, quickly increasing the inductor's magnetic field. The inductor then quickly recharges the capacitor back to a positive peak less than the previous one, due to energy loss in the winding resistance. This completes the second half-cycle, as shown in parts (d) and (e) of Figure 7–35. The peak-to-peak output voltage is therefore approximately equal to $2V_{CC}$.

The amplitude of each successive cycle of the oscillation will be less than that of the previous cycle because of energy loss in the resistance of the tank circuit, as shown in Figure 7–36(a) on page 398, and the oscillation will eventually die out. However, the regular recurrences of the collector current pulse re-energizes the resonant circuit and sustains the oscillations at a constant amplitude.

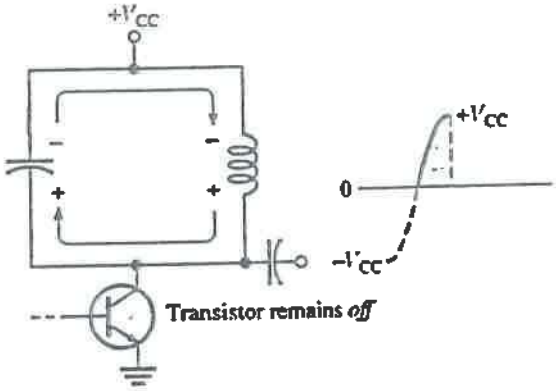
When the tank circuit is tuned to the frequency of the input signal (fundamental), re-energizing occurs on each cycle of the tank voltage V_r, as shown in Figure 7–36(b). When the tank circuit is tuned to the second harmonic of the input signal, re-energizing occurs on alternate cycles as shown in Figure 7–36(c). In this case, a class C amplifier operates as a frequency multiplier (× 2). By tuning the resonant tank circuit to higher harmonics, further frequency multiplication factors are achieved.



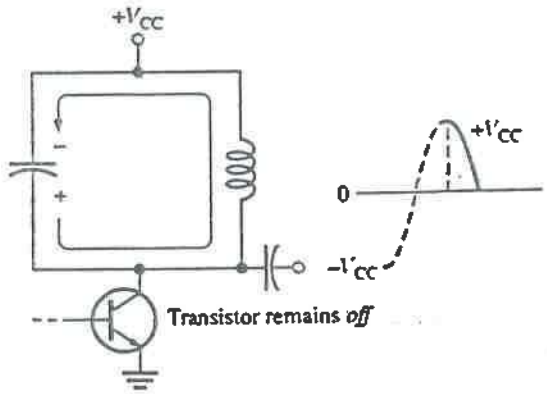
(a) C charges to $+V_{CC}$ at the input peak when transistor is conducting.



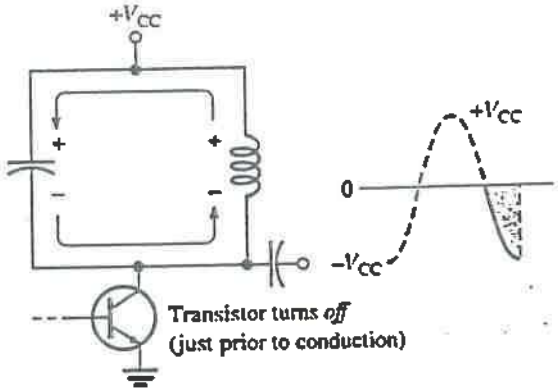
(b) C discharges to 0 volts.



(c) L recharges C in opposite direction.

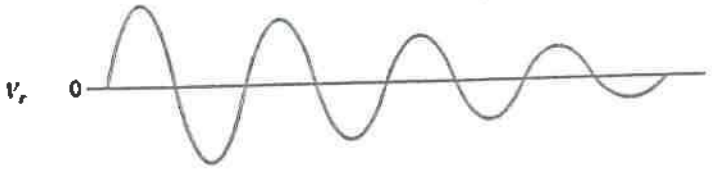


(d) C discharges to 0 volts.

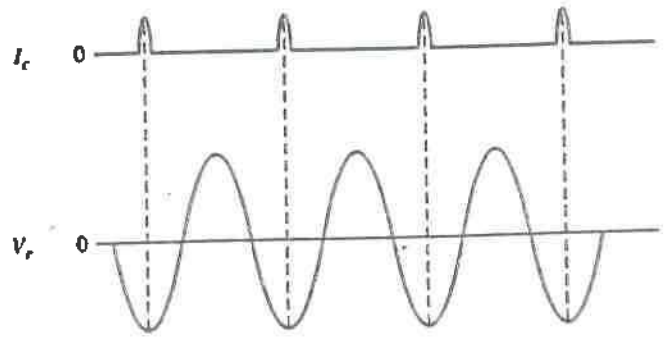


(e) L recharges C.

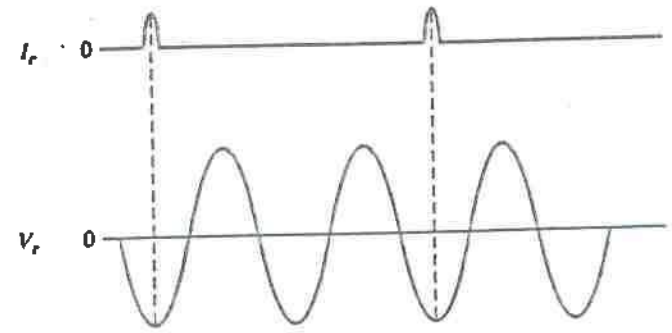
FIGURE 7–35
Resonant circuit action.



(a) Oscillation gradually dies out due to energy loss. The rate of decay depends on the efficiency of the tank circuit.



(b) Oscillation at the fundamental frequency is sustained by short pulses of collector current.



(c) Oscillation at the second harmonic frequency

FIGURE 7–36
Tank circuit oscillations. V_t is the voltage across the tank circuit.

Maximum Output Power

Since the voltage developed across the tank circuit has a peak-to-peak value of approximately $2V_{CC}$, the maximum output power can be expressed as

$$P_{out} = \frac{V_{rms}^2}{R_c} = \frac{(0.707V_{CC})^2}{R_c}$$

$$P_{out} = \frac{0.5V_{CC}^2}{R_c} \tag{7–20}$$

R_c is the equivalent parallel resistance of the collector tank circuit and represents the parallel combination of the coil resistance and the load resistance. It usually has a low value. The total power that must be supplied to the amplifier is

$$P_T = P_{out} + P_{D(avg)}$$

Therefore, the efficiency is

$$\eta = \frac{P_{out}}{P_{out} + P_{D(avg)}} \tag{7–21}$$

When $P_{out} >> P_{D(avg)}$, the class C efficiency closely approaches 1 (100 percent).

EXAMPLE 7–11

Suppose the class C amplifier described in Example 7–10 has a V_{CC} equal to 24 V, and the R_C is 100 Ω. Determine the efficiency.

Solution From Example 7–10, $P_{D(avg)} = 4$ mW.

$$P_{out} = \frac{0.5V_{CC}^2}{R_c} = \frac{0.5(24\text{ V})^2}{100\ \Omega} = 2.88\text{ W}$$

Therefore,

$$\eta = \frac{P_{out}}{P_{out} + P_{D(avg)}} = \frac{2.88\text{ W}}{2.88\text{ W} + 4\text{ mW}} = 0.999$$

or

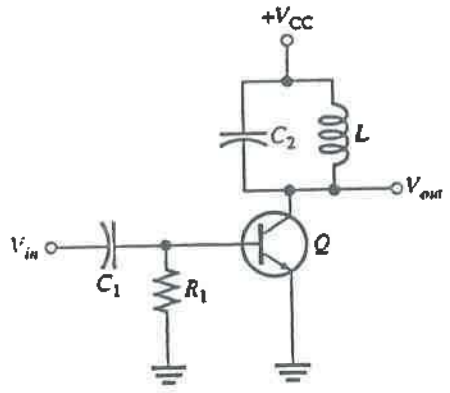
$$\eta \times 100\% = 99.9\%$$

Related Exercise What happens to the efficiency of the amplifier if R_c is increased?

Clamper Bias for a Class C Amplifier

Figure 7–37 shows a class C amplifier with a base bias clamping circuit. The base-emitter junction functions as a diode. When the input signal goes positive, capacitor C_1 is charged to the peak value with the polarity shown in Figure 7–38(a). This action produces

FIGURE 7–37
Tuned class C amplifier with clamper bias.



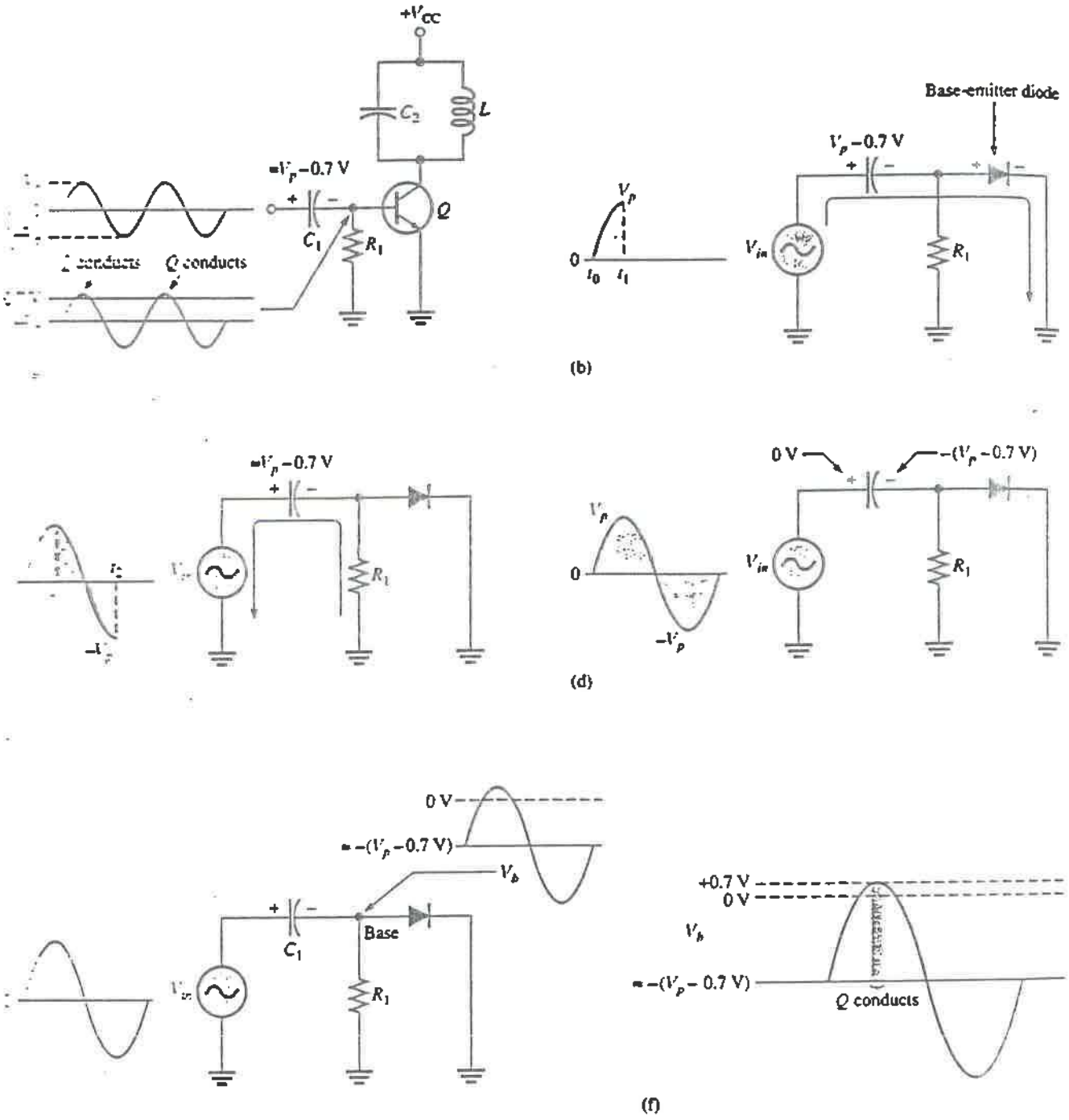


FIGURE 7–38
Clamper bias action.

an average voltage at the base of approximately $-V_p$. This places the transistor in cutoff except at the positive peaks, when the transistor conducts for a short interval. For good clamping action, the R_1C_1 time constant of the clamping circuit must be much greater than the period of the input signal. Parts (b) through (f) of Figure 7–38 illustrate the bias clamping action in more detail. During the time up to the positive peak of the input (t_0 to t_1), the capacitor charges to $V_p - 0.7$ V through the base-emitter diode, as shown in part (b). During the time from t_1 to t_2, as shown in part (c), the capacitor discharges very little

because of the large RC time constant. The capacitor, therefore, maintains an average charge slightly less than $V_p - 0.7$ V.

Since the dc value of the input signal is zero (positive side of C_1), the dc voltage at the base (negative side of C_1) is slightly more positive than $-(V_p - 0.7\text{ V})$, as indicated in Figure 7–38(d). As shown in Figure 7–38(e), the capacitor couples the ac input signal through to the base so that the voltage at the transistor's base is the ac signal riding on a dc level slightly more positive than $-(V_p - 0.7\text{ V})$. Near the positive peaks of the input voltage, the base voltage goes slightly above 0.7 V and causes the transistor to conduct for a short time, as shown in Figure 7–38(f).

SECTION 7–3 REVIEW

1. At what point is a class C amplifier normally biased?
2. What is the purpose of the tuned circuit in a class C amplifier?
3. A certain class C amplifier has a power dissipation of 100 mW and an output power of 1 W. What is its percent efficiency?

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- Collector-Emitter sustaining voltage — @ 100 mA dc
  $V_{CEO(sus)}$ = 60 V dc (Min) — 2N6040, 2N6043
  = 80 V dc (Min) — 2N6041, 2N6044
  = 100 V dc (Min) — 2N6042, 2N6045
- Low collector-emitter saturation voltage
  $V_{CE(sat)}$ = 2.0 V dc (Max) @ I_C = 4.0 A dc — 2N6040,41,2N6043,44
  = 2.0 V dc (Max) @ I_C = 3.0 A dc — 2N6042, 2N6045
- Monolithic construction with built-in base-emitter shunt resistors

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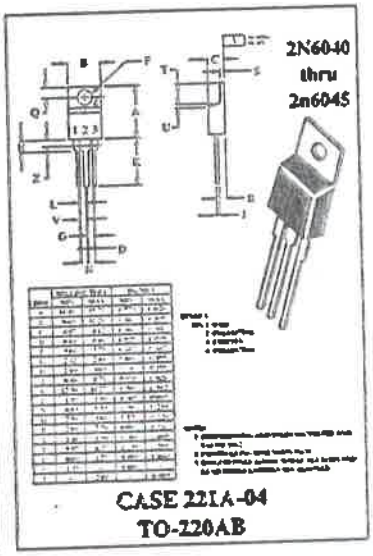


CASE 221A-04
TO-220AB

Maximum Ratings

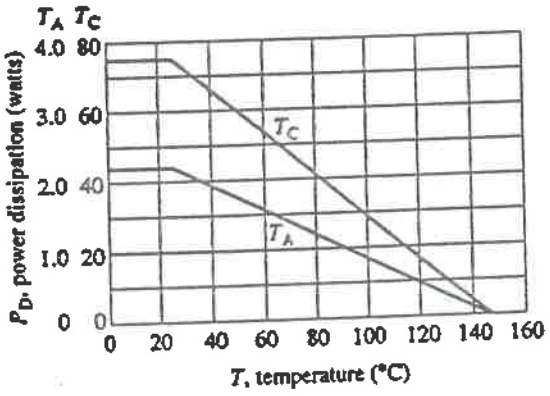
Rating	Symbol	2N6040 2N6043 MJE6040 MJE6043	2N6041 2N6044 MJE6041 MJE6044	2N6042 2N6045 MJE6045	Unit
Collector-Emitter voltage	V_{CEO}	60	80	100	V dc
Collector-Base voltage	V_{CB}	60	80	100	V dc
Emitter-Base voltage	V_{EB}	5.0			V dc
Collector Current—Continuous / Peak	I_C	8.0 / 16			A dc
Base current	I_B	120			mA dc
Total power dissipation @ T_C = 25°C / Derate above 25°C	P_D	75 / 0.60			Watts W/°C
Total power dissipation @ T_A = 25°C / Derate above 25°C	P_D	2.0 / 0.0175			Watts W/°C
Operating and storage junction, Temperature range	T_J, T_{stg}	−65 to +150			°C

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
DC current gain (I_C = 4.0 A dc, V_{CE} = 4.0 V dc) 2N6040,41,2N6043,44,MJE6040,41, MJE6043,44 (I_C = 3.0 A dc, V_{CE} = 4.0 V dc) 2N6042, 2N6045, MJE6045 (I_C = 8.0 A dc, V_{CE} = 4.0 V dc) All Types	h_{FE}	1000 1000 100	20,000 20,000 –	–
Collector-Emitter saturation voltage: (I_C = 4.0 A dc, I_B = 16 mA dc) 2N6040,41,2N6043,44,MJE6040,41,MJE6043,44 (I_C = 3.0 A dc, I_B = 12 mA dc) 2N6042,2N6045,MJE6045 (I_C = 8.0 A dc, I_B = 80 mA dc) All Types	$V_{CE(sat)}$	– – –	2.0 2.0 4.0	V dc
Base-Emitter saturation voltage (I_C = 8.0 A dc, I_B = 80 mA dc)	$V_{BE(sat)}$	–	4.5	V dc
Base-Emitter on voltage (I_C = 4.0 A dc, V_{CE} = 4.0 V dc)	$V_{BE(on)}$	–	2.8	V dc

Dynamic Characteristics

Small-signal current gain (I_C = 3.0 A dc, V_{CE} = 4.0 V dc, f = 1.0 MHz)	$\lvert h_{fe} \rvert$	4.0	–	
Output capacitance (V_{CB} = 10 V dc, I_E = 0, f = 1.0 MHz) 2N6040/2N6042, MJE6040 2N6043/2N6045, MJE6043/MJE6045	C_{ob}	– –	300 200	pF
Small-signal current gain (I_C = 3.0 A dc, V_{CE} = 4.0 V dc, f = 1.0 kHz)	h_{fe}	300	–	–



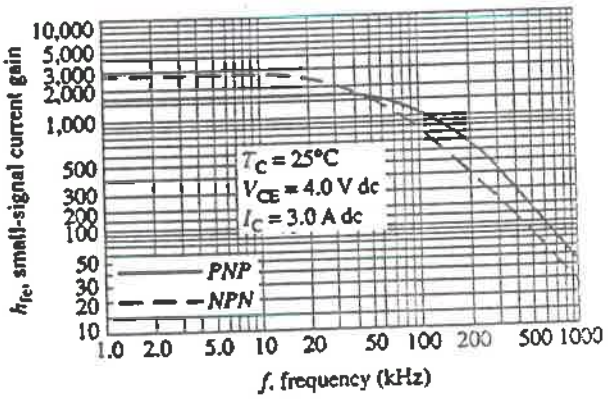


FIGURE 7-43
Partial data sheet for complementary darlington transistors 2N6040 (npn) and 2N6043 (pnp).