UNIT 5

TRANSISTOR BIAS CIRCUITS

5–1 ■ THE DC OPERATING POINT

A transistor must be dc-biased in order to operate as an amplifier. A dc operating point must be set so that signal variations at the input terminal are amplified and accurately reproduced at the output terminal. As you learned in Chapter 4, when you bias a transistor, you establish a certain current and voltage condition. This means, for example, that at the dc operating point, I_C and V_{CE} have specified values. The dc operating point is often referred to as the Q-point (quiescent point).

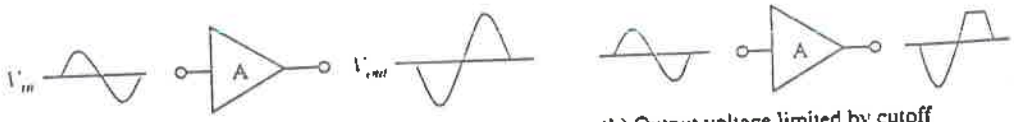
After completing this section, you should be able to

- ■ Discuss the concept of dc bias in a linear amplifier
  - ☐ Describe how to generate collector characteristic curves for a biased transistor
  - ☐ Draw a dc load line for a given biased transistor circuit
  - ☐ Explain Q-point
  - ☐ Explain the conditions for linear operation
  - ☐ Explain the conditions for saturation and cutoff
  - ☐ Discuss the reasons for output waveform distortion

DC Bias

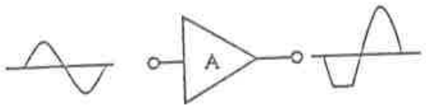
Bias provides for proper operation of an amplifier. If an amplifier is not biased correctly, it can go into saturation or cutoff when an input signal is applied. Figure 5–1 shows the effects of proper and improper biasing of an inverting amplifier. In part (a), the output signal is an amplified replica of the input signal except that it is inverted or 180° out of phase. The output signal swings equally above and below the dc bias level of the output. Improper biasing can cause distortion in the output signal, as illustrated in parts (b) and (c). Part (b) illustrates limiting of the positive portion of the output voltage as a result of a dc operating point (**Q-point**) being too close to cutoff. Part (c) shows limiting of the negative portion of the output voltage as a result of a dc operating point being too close to saturation.

Graphical Analysis The transistor in Figure 5–2(a) is biased with variables V_{CC} and V_{BB} to obtain certain values of I_B, I_C, I_E, and V_{CE}. The collector characteristic curves for this particular transistor are shown in Figure 5–2(b); we will use these to graphically illustrate the effects of dc bias.



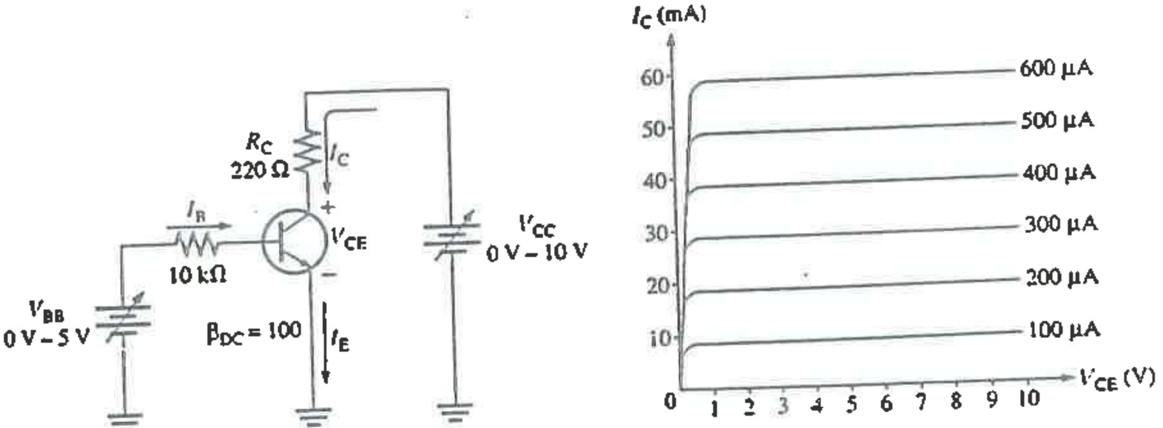
(a) Linear operation

(b) Output voltage limited by cutoff



(c) Output voltage limited by saturation

FIGURE 5–1
Examples of linear and nonlinear operation of an inverting amplifier (the triangle symbol).



(a) Bias circuit

(b) Characteristic curves

FIGURE 5–2

A transistor circuit with variable bias voltages.

In Figure 5–3, we assign three values to I_B and observe what happens to I_C and V_{CE}. First, V_{BB} is adjusted to produce an I_B of 200 µA, as shown in Figure 5–3(a). Since $I_C = \beta_{DC} I_B$, the collector current is 20 mA, as indicated, and

$$V_{CE} = V_{CC} - I_C R_C = 10\text{ V} - (20\text{ mA})(220\ \Omega) = 10\text{ V} - 4.4\text{ V} = 5.6\text{ V}$$

This Q-point is shown on the graph of Figure 5–3(a) as Q_1.

Next, as shown in Figure 5–3(b), V_{BB} is increased to produce an I_B of 300 µA and an I_C of 30 mA.

$$V_{CE} = 10\text{ V} - (30\text{ mA})(220\ \Omega) = 10\text{ V} - 6.6\text{ V} = 3.4\text{ V}$$

The Q-point for this condition is indicated by Q_2 on the graph.

Finally, as in Figure 5–3(c), V_{BB} is increased to give an I_B of 400 µA and an I_C of 40 mA.

$$V_{CE} = 10\text{ V} - (40\text{ mA})(220\ \Omega) = 10\text{ V} - 8.8\text{ V} = 1.2\text{ V}$$

Q_3 is the corresponding Q-point on the graph.

DC Load Line Notice that when I_B increases, I_C increases and V_{CE} decreases. When I_B decreases, I_C decreases and V_{CE} increases. So, as V_{BB} is adjusted up or down, the dc operating point of the transistor moves along a sloping straight line, called the dc load line, connecting each Q-point. At any point along the line, values of I_B, I_C, and V_{CE} can be picked off the graph, as shown in Figure 5–4.

The dc load line intersects the V_{CE} axis at 10 V, the point where $V_{CE} = V_{CC}$. This is the transistor cutoff point because I_B and I_C are zero (ideally). Actually, there is a small leakage current, I_{CBO}, at cutoff as indicated, and therefore V_{CE} is slightly less than 10 V but normally this can be neglected.

The dc load line intersects the I_C axis at 45.5 mA ideally. This is the transistor saturation point because I_C is maximum (ideally 50 mA) at the point where $V_{CE} = 0$ V and $I_C = V_{CC}/R_C$. Actually, there is a small voltage ($V_{CE(sat)}$) across the transistor, and $I_{C(sat)}$ is

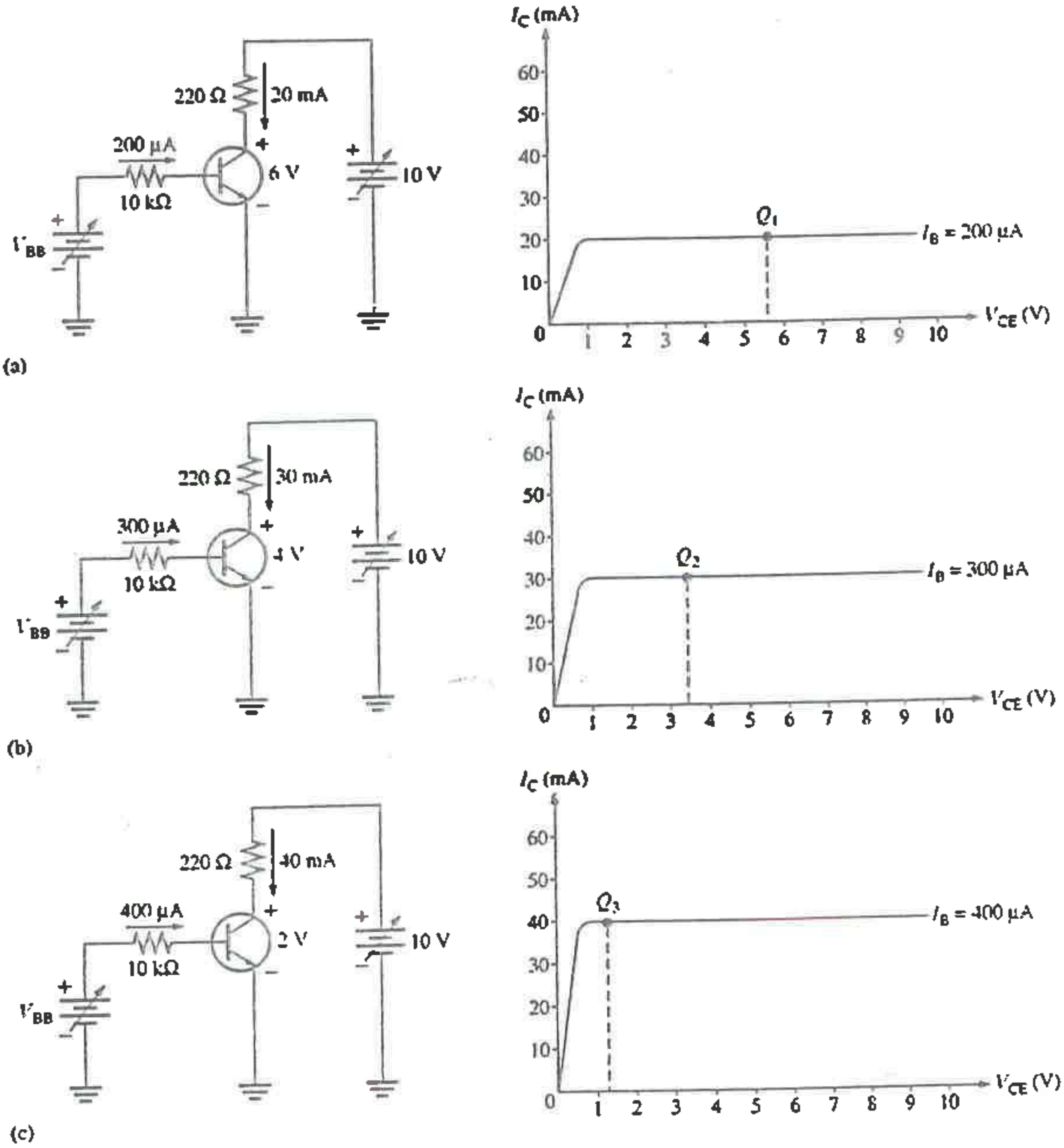


FIGURE 5–3
Illustration of Q-point adjustments.

slightly less than 50 mA, as indicated in Figure 5–4. Note that Kirchhoff's voltage law applied around the collector loop gives

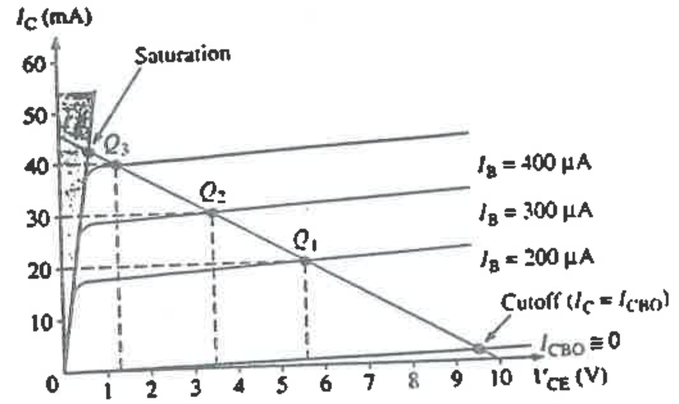
$$V_{CC} - I_C R_C - V_{CE} = 0$$

This results in a straight line equation for the load line of the form $y = mx + b$ as follows:

$$I_C = -\left(\frac{1}{R_E}\right)V_{CE} + \frac{V_{CC}}{R_C}$$

where $-1/R_C$ is the slope and V_{CC}/R_C is the y-axis intercept point.

FIGURE 5–4
The dc load line.



Linear Operation The region along the load line including all points between saturation and cutoff is generally known as the *linear region* of the transistor's operation. As long as the transistor is operated in this region, the output voltage is ideally a linear reproduction of the input.

Figure 5–5 shows an example of the linear operation of a transistor. Assume a sinusoidal voltage, V_{in}, is superimposed on V_{BB}, causing the base current to vary sinusoidally 100 µA above and below its Q-point value of 300 µA. This, in turn, causes the collector current to vary 10 mA above and below its Q-point value of 30 mA. As a result of the variation in collector current, the collector-to-emitter voltage varies 2.2 V above and below its Q-point value of 3.4 V. Point *A* on the load line in Figure 5–5 corresponds to the positive peak of the sinusoidal input voltage. Point *B* corresponds to the negative peak, and point *Q* corresponds to the zero value of the sine wave, as indicated. V_{CEQ} and I_{CQ} are dc Q-point values with no input sinusoidal voltage applied.

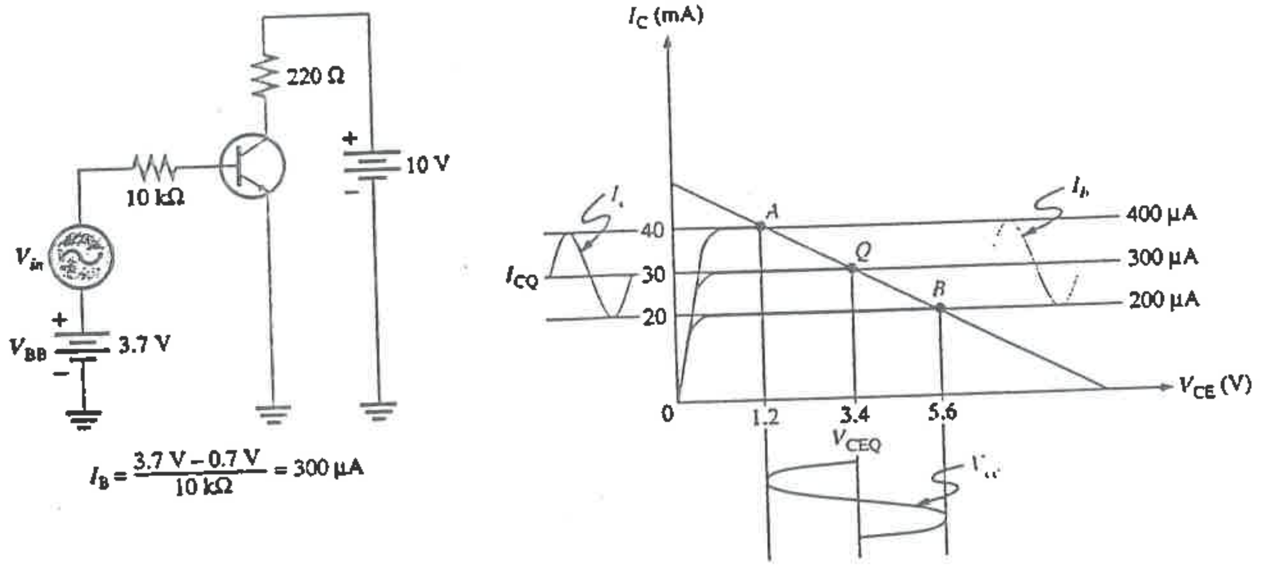
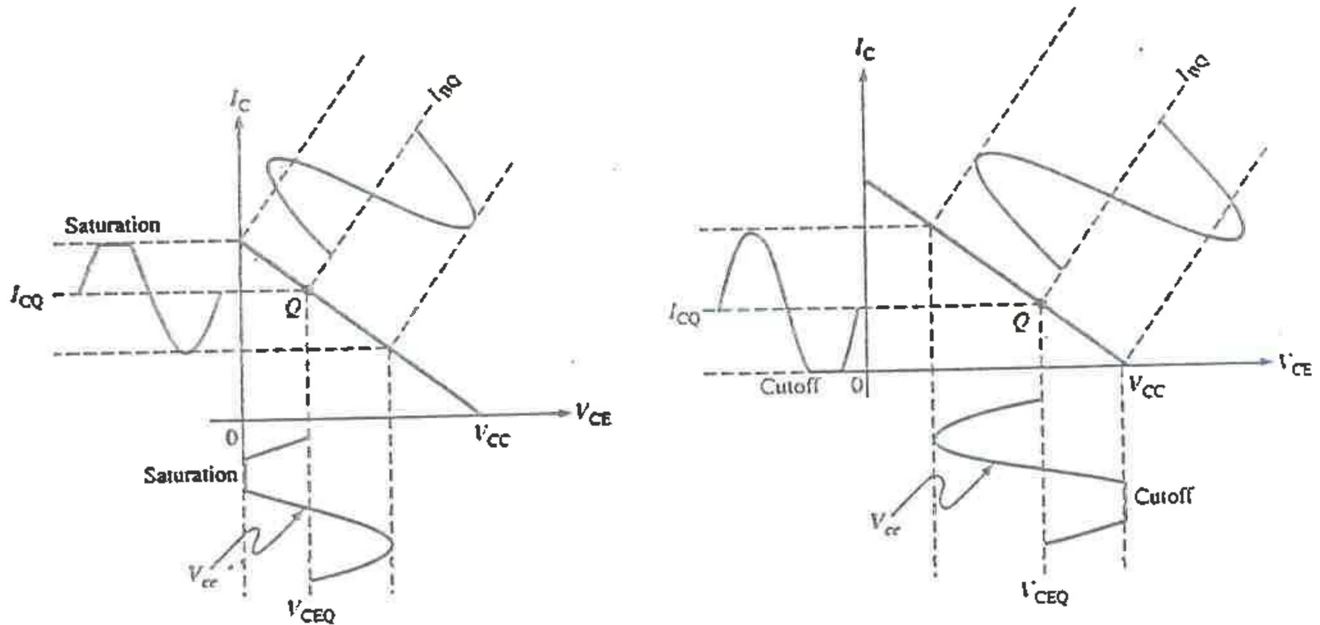


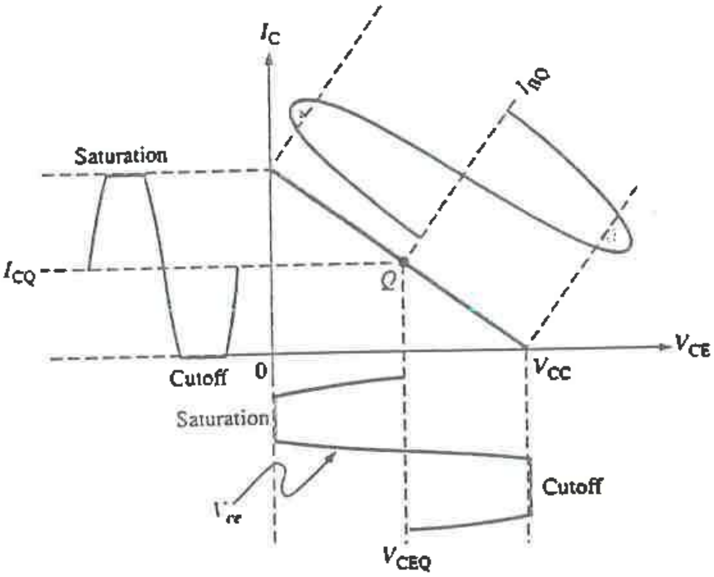
FIGURE 5–5
Variations in collector current and collector-to-emitter voltage as a result of a variation in base current. Notice that ac quantities are indicated by lowercase italic subscripts.

Waveform Distortion As previously mentioned, under certain input signal conditions the location of the Q-point on the load line can cause one peak of V_{ce} to be limited or clipped, as shown in parts (a) and (b) of Figure 5–6. In each case the input signal is too large for the Q-point location and is driving the transistor into cutoff or saturation during a portion of the input cycle. When both peaks are limited as in Figure 5–6(c), the transistor is being driven into both saturation and cutoff by an excessively large input signal.



(a) Transistor driven into saturation

(b) Transistor driven into cutoff



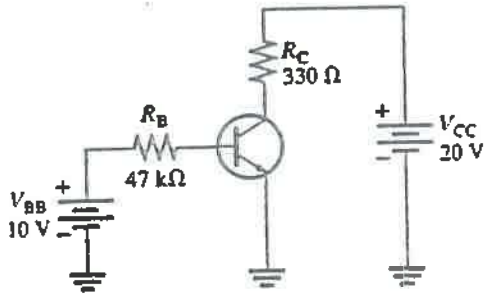
(c) Transistor driven into both saturation and cutoff

FIGURE 5–6
Graphical illustration of saturation and cutoff.

When only the positive peak is limited, the transistor is being driven into cutoff but not saturation. When only the negative peak is limited, the transistor is being driven into saturation but not cutoff. A good rule-of-thumb for a distortion-free output is to limit the maximum peak V_{ce} swing to $0.95V_{CC}$ and the minimum peak to $0.05V_{CC}$ with the Q-point centered on the load line.

EXAMPLE 5–1 Determine the Q-point in Figure 5–7, and find the maximum peak value of base current for linear operation ($\beta_{DC} = 200$).

FIGURE 5–7



Solution The Q-point is defined by I_C and V_{CE}. Find these values by using formulas you learned in Chapter 4.

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{10\text{ V} - 0.7\text{ V}}{47\text{ k}\Omega} = 198\ \mu\text{A}$$

$$I_C = \beta_{DC} I_B = (200)(198\ \mu\text{A}) = 39.6\text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 20\text{ V} - 13.07\text{ V} = 6.93\text{ V}$$

The Q-point is at $I_C = 39.6$ mA and at $V_{CE} = 6.93$ V. Since $I_{C(cutoff)} = 0$, you need to know $I_{C(sat)}$ to determine how much variation in collector current can occur and still maintain linear operation of the transistor.

$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{20\text{ V}}{330\ \Omega} = 60.6\text{ mA}$$

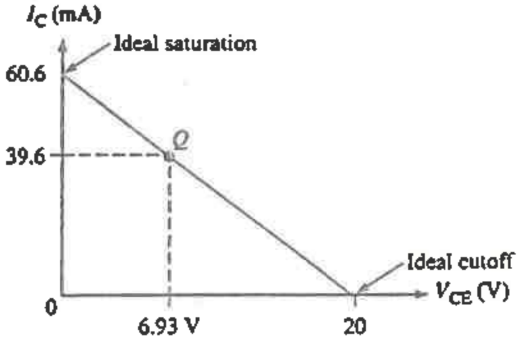
The dc load line is graphically illustrated in Figure 5–8, showing that before saturation is reached, I_C can increase an amount ideally equal to

$$I_{C(sat)} - I_{CQ} = 60.6\text{ mA} - 39.6\text{ mA} = 21\text{ mA}$$

However, I_C can decrease by 39.6 mA before cutoff is reached. Therefore, the limiting excursion is 21 mA because the Q-point is closer to saturation than to cutoff. The 21 mA is the maximum peak variation of the collector current. Actually, it would be slightly less in practice because $V_{CE(sat)}$ is not quite zero. The maximum peak variation of the base current is determined as follows:

$$I_{b(peak)} = \frac{I_{c(peak)}}{\beta_{DC}} = \frac{21\text{ mA}}{200} = 105\ \mu\text{A}$$

FIGURE 5–8



Related Exercise Find the Q-point in Figure 5–7, and determine the maximum peak value of base current for linear operation for the following circuit values: $\beta_{DC} = 100$, $R_C = 1\ k\Omega$, and $V_{CC} = 24$ V.

SECTION 5–1 REVIEW

1. What are the upper and lower limits on a dc load line in terms of V_{CE} and I_C?
2. Define *Q-point.*
3. At what point on the load line does saturation begin? At what point does cutoff occur?
4. For maximum V_{ce}, where should the Q-point be placed?

5–2 ■ BASE BIAS

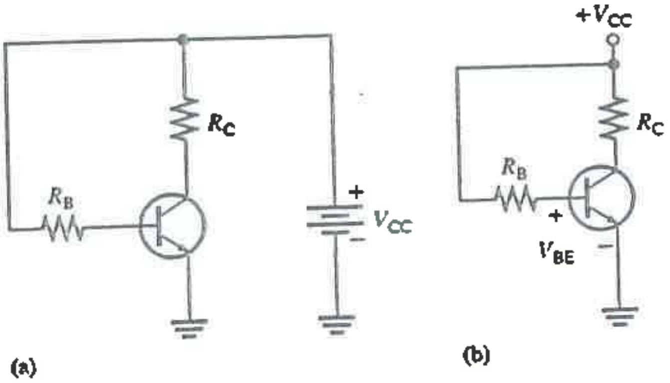
In this section and several following sections, you will learn various methods for dc biasing a transistor circuit without using a separate base bias source. You will see the advantages and disadvantages of each method.

After completing this section, you should be able to

- ■ Analyze a base bias circuit
  - ☐ Recognize a base-biased transistor circuit
  - ☐ Describe how β_{DC} affects the Q-point
  - ☐ Describe how V_{BE} and I_{CBO} affect the Q-point
  - ☐ Discuss the stability of a base bias circuit

Up to this point, we used a separate dc source, V_{BB}, to bias the base-emitter junction strictly for convenience in illustrating transistor operation since it could be varied independently of V_{CC}. A more practical method is to use V_{CC} as the single bias source, as shown in Figure 5–9(a). To simplify the schematics, the battery symbol can be omitted

FIGURE 5–9
Base bias.



and replaced by a line termination circle with a voltage indicator, as shown in Figure 5–9(b).

The analysis of the circuit in Figure 5–9 for the linear region is as follows. The voltage drop across R_B is $V_{CC} - V_{BE}$. Therefore,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \tag{5–1}$$

Kirchhoff's voltage law applied around the collector circuit in Figure 5–9(a) gives the following equation:

$$V_{CC} - I_C R_C - V_{CE} = 0$$

Solving for V_{CE}, we get

$$V_{CE} = V_{CC} - I_C R_C \tag{5–2}$$

We can neglect the leakage current, I_{CBO}. We already know that $I_C = \beta_{DC} I_B$; therefore,

$$I_C = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right) \tag{5–3}$$

Effect of β_{DC} on the Q-Point

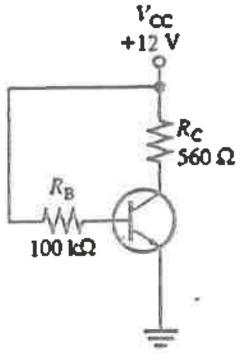
Notice that Equation (5–3) shows that I_C is dependent on β_{DC}. The disadvantage of this is that a variation in β_{DC} causes both I_C and V_{CE} to change, thus changing the Q-point of the transistor and making the base bias circuit extremely beta-dependent.

Recall that β_{DC} varies with temperature and collector current. In addition, there is a large spread of values from one device to another of the same type due to manufacturing variations. Therefore, a circuit using base bias may suddenly produce a distorted output if, due to a fault, the transistor is replaced with one having a different β_{DC} or if a temperature change causes a sufficient shift in the value of β_{DC}.

EXAMPLE 5–2

The base bias circuit in Figure 5–10 is subjected to an increase in temperature from 25°C to 75°C. If $\beta_{DC} = 100$ at 25°C and 150 at 75°C, determine the percent change in Q-point values (I_C and V_{CE}) over the temperature range. Neglect any change in V_{BE} and the effects of any leakage current.

FIGURE 5–10



Solution At 25°C, I_C and V_{CE} are determined as follows:

$$I_C = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right) = 100\left(\frac{12\text{ V} - 0.7\text{ V}}{100\text{ k}\Omega}\right) = 11.3\text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 12\text{ V} - (11.3\text{ mA})(560\ \Omega) = 5.67\text{ V}$$

At 75°C, I_C and V_{CE} are determined as follows:

$$I_C = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right) = 150\left(\frac{12\text{ V} - 0.7\text{ V}}{100\text{ k}\Omega}\right) = 17.0\text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 12\text{ V} - (17.0\text{ mA})(560\ \Omega) = 2.48\text{ V}$$

The percent change in I_C is

$$\%\ \Delta I_C = \frac{I_{C(75°)} - I_{C(25°)}}{I_{C(25°)}} \times 100\%$$

$$= \frac{17.0\text{ mA} - 11.3\text{ mA}}{11.3\text{ mA}} \times 100\% \cong 50\% \quad \text{(an increase)}$$

Notice the I_C changes by the same percentage as β_{DC}. The percent change in V_{CE} is

$$\%\ \Delta V_{CE} = \frac{V_{CE(75°)} - V_{CE(25°)}}{V_{CE(25°)}} \times 100\%$$

$$= \frac{2.48\text{ V} - 5.67\text{ V}}{5.67\text{ V}} \times 100\% = -56.3\ \% \quad \text{(a decrease)}$$

As you can see, the Q-point is extremely dependent on β_{DC} in this circuit and therefore makes the base bias arrangement very unstable. Consequently, base bias is not normally used if linear operation is required. It can be used for switching operation.

Related Exercise If $\beta_{DC} = 50$ at 0°C and 125 at 100°C for the circuit in Figure 5–10, determine the percent change in the Q-point values over the temperature range.

Other Factors Influencing Bias Stability

In addition to being affected by a change in β_{DC}, the bias point can be affected by changes in V_{BE} and I_{CBO}. The base-to-emitter voltage, V_{BE}, decreases with an increase in temperature. As you can see from the equation for I_B, a decrease in V_{BE} increases I_B.

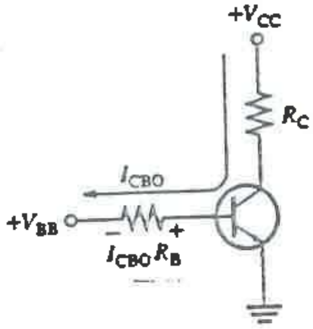
$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

The effect of a change in V_{BE} is negligible if $V_{CC} >> V_{BE}$ (V_{CC} at least 10 times greater than V_{BE}).

The reverse leakage current, I_{CBO}, has the effect of decreasing the net base current and thus increasing the base voltage because it creates a voltage drop across R_B with a polarity that adds to the base bias voltage, as shown in Figure 5–11. In modern transistors, I_{CBO} is usually less than 100 nA, and its effect on the bias is negligible if $V_{BB} >> I_{CBO}R_B$.

FIGURE 5–11

Effect of I_{CBO}.



SECTION 5–2 REVIEW

1. What is an advantage of base bias over using two separate dc supplies?
2. What is the main disadvantage of the base bias method?
3. Explain why the base bias Q-point changes with temperature.

5–3 ■ EMITTER BIAS

Although this method of biasing requires two separate dc voltage sources, one positive and the other negative, it does have an important advantage as you will learn.

After completing this section, you should be able to

- ■ Analyze an emitter bias circuit
  - ☐ Discuss the effect of β_{DC} and V_{CE} on the Q-point
  - ☐ Explain how to minimize or essentially eliminate the effects of β_{DC} and V_{BE} on the stability of the Q-point
  - ☐ Discuss emitter bias for a *pnp* transistor

An emitter bias circuit uses both a positive and a negative supply voltage, as shown in Figure 5–12. In this circuit, the V_{EE} supply voltage forward-biases the base-emitter junction. Kirchhoff's voltage law applied around the base-emitter circuit in Figure 5–12(a), which has been redrawn in Figure 5–12(b) for analysis, gives the following equation:

$$V_{EE} - I_B R_B - V_{BE} - I_E R_E = 0$$

Solving for V_{EE}, we get

$$V_{EE} = I_B R_B + I_E R_E + V_{BE}$$

Since $I_C \cong I_E$ and $I_C = \beta_{DC} I_B$,

$$I_B \cong \frac{I_E}{\beta_{DC}}$$

Substituting for I_B, we get

$$\left(\frac{I_E}{\beta_{DC}}\right) R_B + I_E R_E + V_{BE} = V_{EE}$$

Factoring out I_E yields

$$I_E\left(\frac{R_B}{\beta_{DC}} + R_E\right) + V_{BE} = V_{EE}$$

Transposing V_{BE} and then solving for I_E, we get

$$I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta_{DC}} \qquad (5\text{–}4)$$

Since $I_C \cong I_E$,

$$I_C \cong \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta_{DC}} \qquad (5\text{–}5)$$

The emitter voltage with respect to ground is

$$V_E = -V_{EE} + I_E R_E \qquad (5\text{–}6)$$

The base voltage with respect to ground is

$$V_B = V_E + V_{BE} \qquad (5\text{–}7)$$

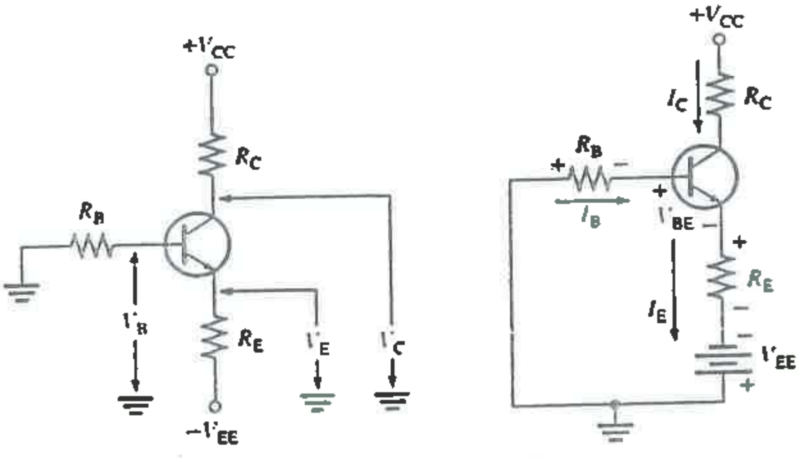
The collector voltage with respect to ground is

$$V_C = V_{CC} - I_C R_C \qquad (5\text{–}8)$$

Subtracting V_E from V_C and using the approximation $I_C \cong I_E$, we get

$$V_{CE} = V_{CC} - I_C R_C - (-V_{EE} + I_E R_E)$$

$$V_{CE} \cong V_{CC} + V_{EE} - I_C(R_C + R_E) \qquad (5\text{–}9)$$



(a) (b)

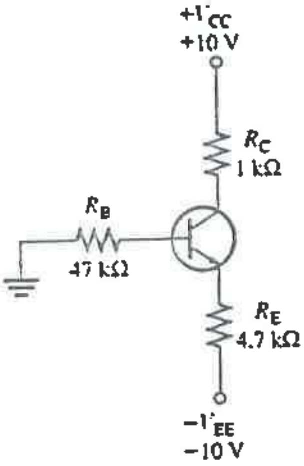
FIGURE 5–12

An npn transistor with emitter bias. Polarities are reversed for a pnp. Single subscripts indicate voltages with respect to ground.

EXAMPLE 5–3

Find I_E, I_C, and V_{CE} in Figure 5–13 for $\beta_{DC} = 100$ and $V_{BE} = 0.7$ V. Draw the dc load line.

FIGURE 5–13



Solution

$$I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta_{DC}} = \frac{10\text{ V} - 0.7\text{ V}}{4.7\text{ k}\Omega + 47\text{ k}\Omega/100} = \frac{9.3\text{ V}}{5.17\text{ k}\Omega} = 1.80\text{ mA}$$

$$I_C \cong I_E = 1.80\text{ mA}$$

$$V_{CE} \cong V_{CC} + V_{EE} - I_C(R_C + R_E) = 10\text{ V} + 10\text{ V} - 1.80\text{ mA}\,(5.7\text{ k}\Omega) = 9.74\text{ V}$$

I_C and V_{CE} are the Q-point values for the circuit in Figure 5–13. The dc load line is graphically illustrated in Figure 5–14. The approximate collector saturation current is determined as follows:

$$I_{C(sat)} = \frac{V_{CC} - (-V_{EE})}{R_C + R_E} = \frac{10\text{ V} - (-10\text{ V})}{5.7\text{ k}\Omega} = \frac{20\text{ V}}{5.7\text{ k}\Omega} = 3.51\text{ mA}$$

The collector-to-emitter voltage at cutoff is

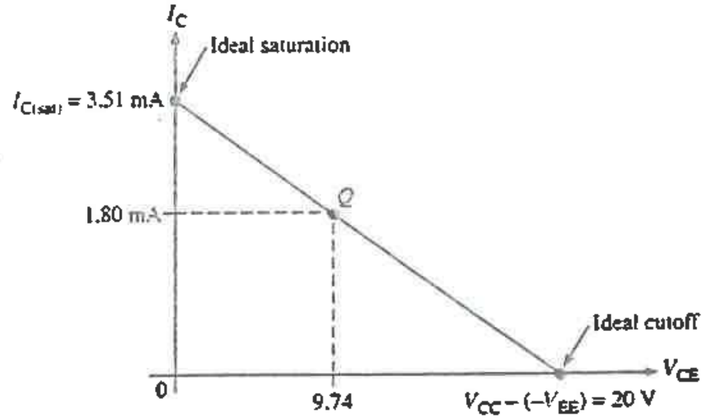
$$V_{CE(cutoff)} = V_{CC} - (-V_{EE}) = 10\text{ V} - (-10\text{ V}) = 20\text{ V}$$

The dc load line, illustrated in Figure 5–14, shows that I_C can increase an amount ideally equal to

$$\Delta I_{C(max)} = I_{C(sat)} - I_{CQ} = 3.51\text{ mA} - 1.80\text{ mA} = 1.71\text{ mA}$$

before saturation is reached. I_C can decrease by 1.80 mA before cutoff is reached. As you can see, this circuit is biased slightly closer to saturation than to cutoff.

FIGURE 5–14



Related Exercise Find I_E, I_C, and V_{CE} for the circuit in Figure 5–13 with the following component values: R_B = 100 kΩ, R_C = 680 Ω, R_E = 3.3 kΩ, V_{CC} = +15 V, and $-V_{EE}$ = −15 V. Assume β_{DC} = 150.

Stability of Emitter Bias

The formula for I_E shows that the emitter bias circuit is dependent on V_{BE} and β_{DC}, both of which change with temperature and current.

$$I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta_{DC}}$$

If $R_E >> R_B/\beta_{DC}$, the equation becomes

$$I_E \cong \frac{V_{EE} - V_{BE}}{R_E}$$

This condition makes I_E independent of β_{DC}.

A further modification can be made if $V_{EE} >> V_{BE}$.

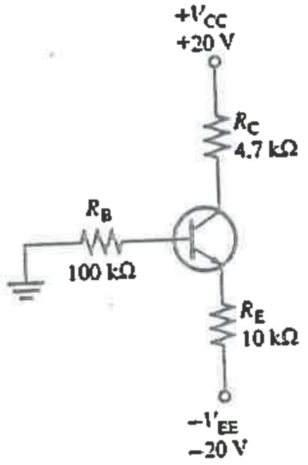
$$I_E \cong \frac{V_{EE}}{R_E}$$

This condition makes I_E independent of V_{BE}.

If I_E is independent of β_{DC} and V_{BE}, then the Q-point is not affected appreciably by variations in these parameters. Thus, emitter bias can provide a stable Q-point if properly designed.

EXAMPLE 5–4 Determine how much the Q-point in Figure 5–15 will change over a temperature range where β_{DC} increases from 85 to 100 and V_{BE} decreases from 0.7 V to 0.6 V.

FIGURE 5–15



Solution For $\beta_{DC} = 85$ and $V_{BE} = 0.7$ V,

$$I_C \cong I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta_{DC}} = \frac{20\text{ V} - 0.7\text{ V}}{10\text{ k}\Omega + 100\text{ k}\Omega/85} = 1.73\text{ mA}$$

$$V_C = V_{CC} - I_C R_C = 20\text{ V} - (1.73\text{ mA})(4.7\text{ k}\Omega) = 11.9\text{ V}$$

$$V_E = -V_{EE} + I_E R_E = -20\text{ V} + (1.73\text{ mA})(10\text{ k}\Omega) = -2.7\text{ V}$$

Therefore,

$$V_{CE} = V_C - V_E = 11.9\text{ V} - (-2.7\text{ V}) = 14.6\text{ V}$$

For $\beta_{DC} = 100$ and $V_{BE} = 0.6$ V,

$$I_C \cong I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta_{DC}} = \frac{20\text{ V} - 0.6\text{ V}}{10\text{ k}\Omega + 100\text{ k}\Omega/100} = 1.85\text{ mA}$$

$$V_C = V_{CC} - I_C R_C = 20\text{ V} - (1.85\text{ mA})(4.7\text{ k}\Omega) = 11.3\text{ V}$$

$$V_E = -V_{EE} + I_E R_E = -20\text{ V} + (1.85\text{ mA})(10\text{ k}\Omega) = -1.5\text{ V}$$

Therefore,

$$V_{CE} = V_C - V_E = 11.3\text{ V} - (-1.5\text{ V}) = 12.8\text{ V}$$

The percent change in I_C as β_{DC} changes from 85 to 100 is

$$\frac{1.85\text{ mA} - 1.73\text{ mA}}{1.73\text{ mA}} \times 100\% = 6.94\%$$

The percent change in V_{CE} is

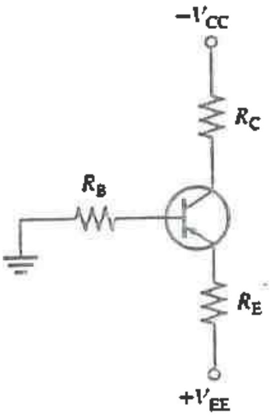
$$\frac{12.8\text{ V} - 14.6\text{ V}}{12.8\text{ V}} \times 100\% = 14.0\%$$

Related Exercise Determine how much the Q-point in Figure 5–15 changes over a temperature range where β_{DC} increases from 65 to 75 and V_{BE} decreases from 0.75 V to 0.59 V. The supply voltages are ±10 V.

Emitter-Biased *PNP*

Figure 5–16 shows a *pnp* transistor with emitter bias. The basic difference is that the polarities of the supply voltages are reversed from those of the *npn*. The operation and analysis are basically the same, as Example 5–5 illustrates.

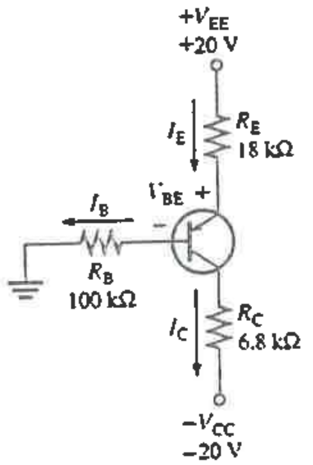
FIGURE 5–16
Emitter-biased pnp transistor.



EXAMPLE 5–5

Determine V_C, V_E, and V_{CE} in the circuit of Figure 5–17. Assume $\beta_{DC} = 100$ and $V_{BE} = 0.7$ V. Notice how the transistor is oriented in this diagram with the positive emitter supply at the top and the negative collector supply at the bottom.

FIGURE 5–17



Solution

$$I_C \cong I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta_{DC}} = \frac{20\text{ V} - 0.7\text{ V}}{18\text{ k}\Omega + 100\text{ k}\Omega/100} = 1.02\text{ mA}$$

$$V_C = -V_{CC} + I_C R_C = -20\text{ V} + (1.02\text{ mA})(6.8\text{ k}\Omega) = 13.1\text{ V}$$

$$V_E = V_{EE} - I_E R_E = 20\text{ V} - (1.02\text{ mA})(18\text{ k}\Omega) = 1.64\text{ V}$$

Therefore,

$$V_{CE} = V_C - V_E = -13.1\text{ V} - 1.64\text{ V} = -14.7\text{ V}$$

Related Exercise Does V_C become more or less negative if R_C is increased? Will an increase in R_C change the collector current significantly? Calculate the collector voltage if R_C is 8.2 kΩ.

SECTION 5–3 REVIEW

1. Why is emitter bias more stable than base bias?
2. For an emitter-biased *npn* transistor, what is the approximate relationship of V_B and V_E? For a *pnp* transistor?
3. What is the main disadvantage of emitter bias?
4. An emitter-biased *pnp* transistor has dc supply voltages of ±15 V. If R_E is 10 kΩ, what is the emitter current?

5–4 ■ VOLTAGE-DIVIDER BIAS

Next, you will study a method of biasing a transistor for linear operation using a resistive voltage-divider. This is the most widely used biasing method, for reasons that you will discover in this section. This method is actually a form of emitter bias using a single supply voltage.

After completing this section, you should be able to

- ■ Analyze a voltage-divider bias circuit
  - ☐ Discuss the effect of the input resistance on the bias circuit
  - ☐ Discuss the stability of voltage-divider bias
  - ☐ Explain how to minimize or essentially eliminate the effects of β_{DC} and V_{BE} on the stability of the Q-point
  - ☐ Discuss voltage-divider bias for a *pnp* transistor

A dc bias voltage at the base of the transistor is developed by a resistive voltage-divider consisting of R_1 and R_2 as shown in Figure 5–18. At point *A*, there are two current paths to ground: one through R_2 and the other through the base-emitter junction of the transistor.

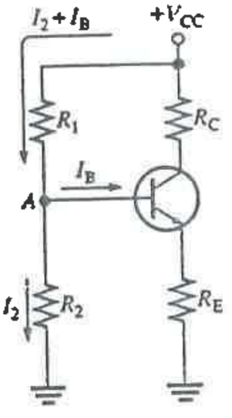
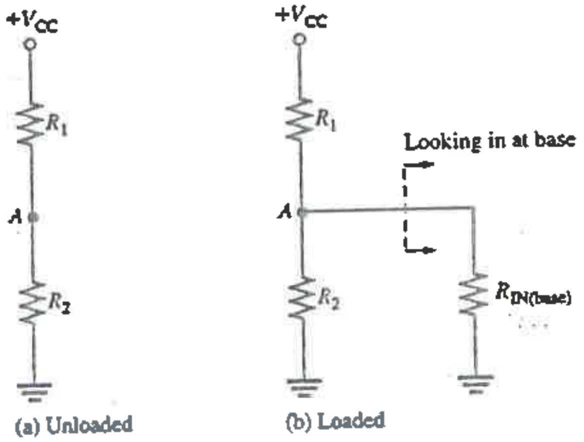


FIGURE 5–18
Voltage-divider bias.

If the base current is much smaller than the current through R_2, the bias circuit can be viewed as a simplified voltage-divider consisting of R_1 and R_2, as indicated in Figure 5–19(a). If I_B is *not* small enough to neglect compared to I_2, then the dc input resistance, $R_{IN(base)}$, from the base of the transistor to ground must be considered. $R_{IN(base)}$ appears in parallel with R_2, as shown in Figure 5–19(b).

FIGURE 5–19

Simplified voltage-divider.



(a) Unloaded (b) Loaded

Input Resistance at the Base

To develop a formula for the dc input resistance at the base of a transistor, we will use the diagram in Figure 5–20. V_{IN} is applied between base and ground, and I_{IN} is the current into the base as shown. By Ohm's law,

$$R_{IN(base)} = \frac{V_{IN}}{I_{IN}}$$

Kirchhoff's voltage law applied around the base-emitter circuit yields

$$V_{IN} = V_{BE} + I_E R_E$$

With the assumption that $V_{BE} << I_E R_E$, the equation reduces to

$$V_{IN} \cong I_E R_E$$

Now, since $I_E \cong I_C = \beta_{DC} I_B$,

$$V_{IN} \cong \beta_{DC} I_B R_E$$

The input current is the base current:

$$I_{IN} = I_B$$

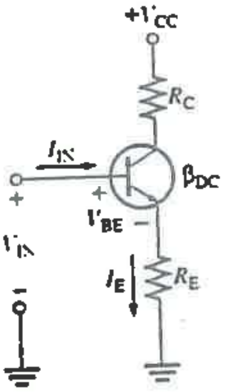
By substitution,

$$R_{IN(base)} = \frac{V_{IN}}{I_{IN}} \cong \frac{\beta_{DC} I_B R_E}{I_B}$$

So,

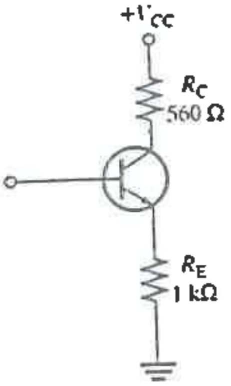
$$R_{IN(base)} \cong \beta_{DC} R_E \qquad (5\text{–}10)$$

FIGURE 5–20
DC input resistance is V_{IN}/I_{IN}.



EXAMPLE 5–6 Determine the dc input resistance at the base of the transistor in Figure 5–21. $\beta_{DC} = 125$.

FIGURE 5–21



Solution $R_{IN(base)} \cong \beta_{DC}R_E = (125)(1\ k\Omega) = 125\ k\Omega$

Related Exercise What is $R_{IN(base)}$ if $\beta_{DC} = 60$ and $R_E = 910\ \Omega$ in Figure 5–21?

Analysis of a Voltage-Divider Bias Circuit

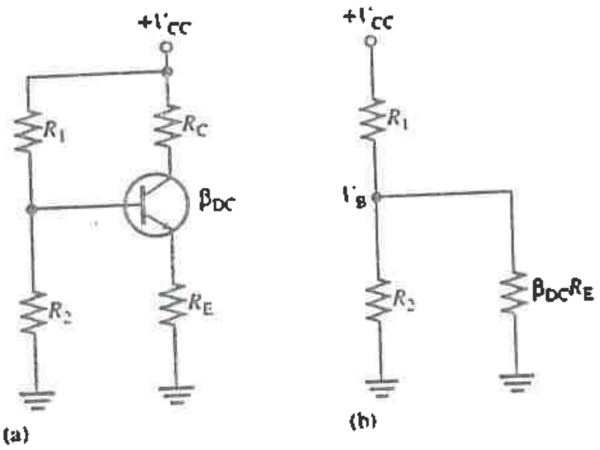
A voltage-divider biased *npn* transistor is shown in Figure 5–22(a). Let's begin the analysis by determining the voltage at the base using the voltage-divider formula, which is developed as follows.

$$R_{IN(base)} \cong \beta_{DC}R_E$$

The total resistance from base to ground is

$$R_2 \parallel \beta_{DC}R_E$$

FIGURE 5–22
An npn transistor with voltage-divider bias.



(a) (b)

A voltage-divider is formed by R_1 and the resistance from base to ground in parallel with R_2 as shown in Figure 5–22(b). Applying the voltage-divider formula yields

$$V_B = \left(\frac{R_2 \parallel \beta_{DC}R_E}{R_1 + (R_2 \parallel \beta_{DC}R_E)}\right)V_{CC} \qquad (5\text{–}11)$$

If $\beta_{DC}R_E >> R_2$, then the formula simplifies to

$$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} \qquad (5\text{–}12)$$

Once you know the base voltage, you can determine the emitter voltage, which equals V_B less the value of the base-emitter drop (V_{BE}).

$$V_E = V_B - V_{BE}$$

The emitter current can be found by using Ohm's law.

$$I_E = \frac{V_E}{R_E}$$

Once you know I_E, you can find all the other circuit values.

$$I_C \cong I_E$$

$$I_C \cong \frac{V_B - V_{BE}}{R_E} \qquad (5\text{–}13)$$

$$V_C = V_{CC} - I_C R_C$$
$$V_{CE} = V_C - V_E$$

Also, you can express V_{CE} in terms of I_C by using Kirchhoff's voltage law as follows:

$$V_{CC} - I_C R_C - I_E R_E - V_{CE} = 0$$

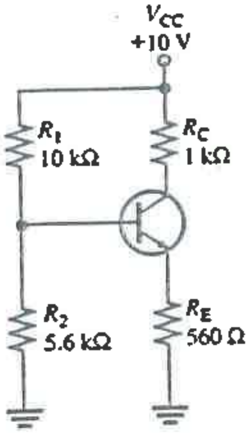
Since $I_C \cong I_E$,

$$V_{CE} \cong V_{CC} - I_C R_C - I_C R_E$$

$$V_{CE} \cong V_{CC} - I_C(R_C + R_E) \qquad (5\text{–}14)$$

EXAMPLE 5–7 Determine V_{CE} and I_C in Figure 5–23, where $\beta_{DC} = 100$.

FIGURE 5–23



Solution First, determine the dc input resistance at the base to see if it can be neglected.

$$R_{IN(base)} = \beta_{DC} R_E = (100)(560\ \Omega) = 56\ k\Omega$$

A common rule-of-thumb is that if two resistors are in parallel and one is at least ten times the other, the total resistance is taken to be approximately equal to the smallest value although, in some cases, this may result in unacceptable inaccuracy.

In this case, $R_{IN(base)} = 10R_2$, so neglect $R_{IN(base)}$. In the related exercise, you will rework this example taking $R_{IN(base)}$ into account and compare the difference. Proceed with the analysis by determining the base voltage:

$$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{5.6\ k\Omega}{15.6\ k\Omega}\right)10\ V = 3.59\ V$$

So,

$$V_E = V_B - V_{BE} = 3.59\ V - 0.7\ V = 2.89\ V$$

and

$$I_E = \frac{V_E}{R_E} = \frac{2.89\ V}{560\ \Omega} = 5.16\ mA$$

Therefore,

$$I_C \cong 5.16\ mA$$

and

$$V_{CE} \cong V_{CC} - I_C(R_C + R_E) = 10\ \text{V} - 5.16\ \text{mA}(1.56\ \text{k}\Omega) = 1.95\ \text{V}$$

Since $V_{CE} > 0$ V (or a few tenths of a volt), you know that the transistor is *not* in saturation.

Related Exercise Rework this example taking into account $R_{IN(base)}$ and compare the results.

5–5 ■ COLLECTOR-FEEDBACK BIAS

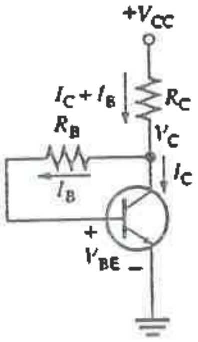
Another type of bias arrangement is the collector-feedback circuit. This type of circuit is a negative feedback connection that provides a relatively stable Q-point by reducing the effect of variations in β_{DC}. It is also a simple circuit in terms of the components required.

After completing this section, you should be able to

- Analyze a collector-feedback bias circuit
  - ☐ Discuss the effect of negative feedback
  - ☐ Explain how the collector feedback maintains a relatively stable Q-point over temperature

In Figure 5–28, the base resistor R_B is connected to the collector rather than to V_{CC}, as in the base bias arrangement discussed earlier. The collector voltage provides the bias for the base-emitter junction. The negative feedback creates an "offsetting" effect that tends to keep the Q-point stable. If I_C tries to increase, it drops more voltage across R_C, thereby causing V_C to decrease. When V_C decreases, there is a decrease in voltage across R_B, which decreases I_B. The decrease in I_B produces less I_C which, in turn, drops less voltage across R_C and thus offsets the decrease in V_C.

FIGURE 5–28
Collector-feedback bias.



Analysis of Collector Feedback

By Ohm's law, we can express the base current as

$$I_B = \frac{V_C - V_{BE}}{R_B} \qquad (5\text{–}16)$$

Let's assume that $I_C >> I_B$. The collector voltage is

$$V_C \cong V_{CC} - I_C R_C$$

Also,

$$I_B = \frac{I_C}{\beta_{DC}}$$

Substituting for I_B and V_C in Equation (5–16), we get

$$\frac{I_C}{\beta_{DC}} = \frac{V_{CC} - I_C R_C - V_{BE}}{R_B}$$

We can rearrange the terms so that

$$\frac{I_C R_B}{\beta_{DC}} + I_C R_C = V_{CC} - V_{BE}$$

Then we can solve for I_C as follows:

$$I_C(R_C + R_B/\beta_{DC}) = V_{CC} - V_{BE}$$

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + R_B/\beta_{DC}} \qquad (5\text{–}17)$$

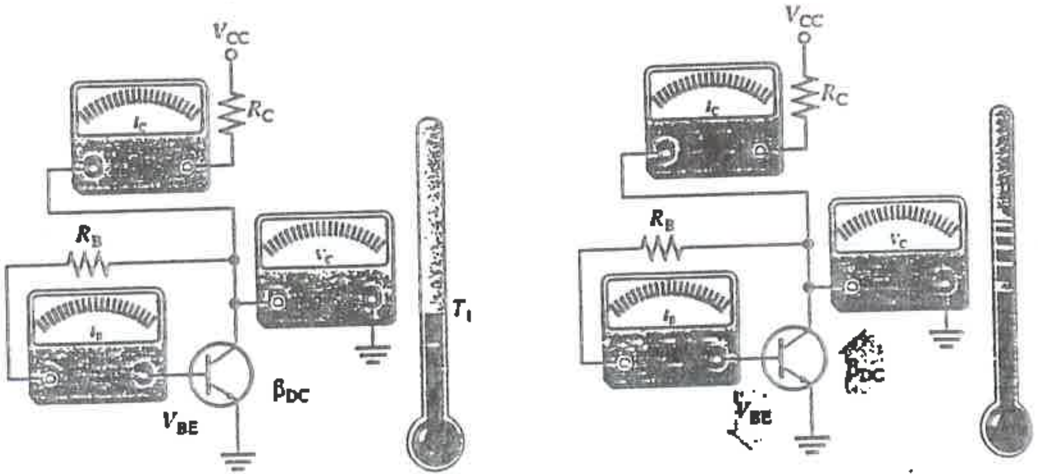
Since the emitter is ground, $V_{CE} = V_C$.

$$V_{CE} = V_{CC} - I_C R_C \qquad (5\text{–}18)$$

Stability Over Temperature

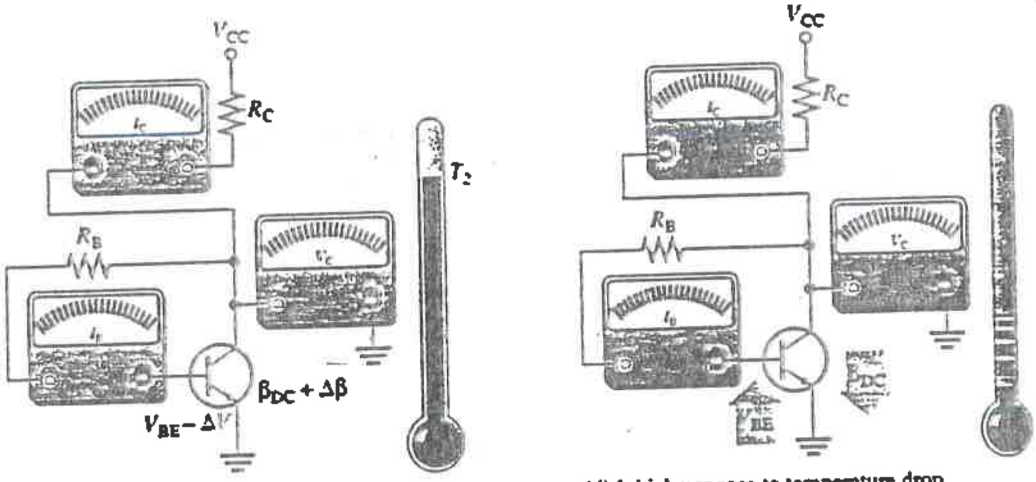
Equation (5–17) shows that the collector current is dependent to some extent on β_{DC} and V_{BE}. This dependency, of course, can be minimized by making $R_C >> R_B/\beta_{DC}$ and $V_{CC} >> V_{BE}$. An important feature of collector-feedback bias is that it essentially eliminates the β_{DC} and V_{BE} dependency even if the stated conditions are not met.

As you have learned, β_{DC} varies directly with temperature, and V_{BE} varies inversely with temperature. Refer to Figure 5–29. The circuit has initial values of I_B, I_C, and V_{CE} as indicated in part (a). In part (b), as the temperature goes up, β_{DC} goes up and V_{BE} goes down. The increase in β_{DC} acts to increase I_C. The decrease in V_{BE} acts to increase I_B which, in turn also acts to increase I_C. As I_C tries to increase, the voltage drop across R_C also tries to increase. This tends to reduce the collector voltage and therefore the voltage



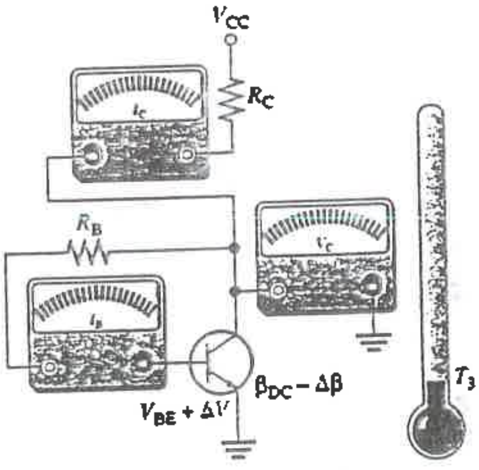
(a) Stabilized at initial temperature, T_1

(b) Initial response to temperature rise



(c) Stabilized at higher temperature, T_2

(d) Initial response to temperature drop



(e) Stabilized at lower temperature, T_3

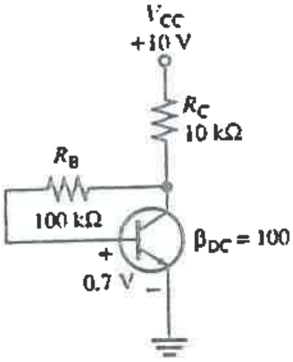
FIGURE 5–29
Collector-feedback stabilization of Q-point values over temperature.

across R_B, thus reducing I_B and offsetting the attempted increase in I_C and the attempted decrease in V_C. The result is that the collector-feedback circuit maintains a stable Q-point, as indicated in Figure 5–29(c).

The reverse action occurs when the temperature decreases, as illustrated in Figure 5–29(d) and (e).

EXAMPLE 5–10 Calculate the Q-point values (I_C and V_{CE}) for the circuit in Figure 5–30.

FIGURE 5–30



Solution Use Equation (5–17):

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + R_B/\beta_{DC}} = \frac{10\text{ V} - 0.7\text{ V}}{10\text{ k}\Omega + 100\text{ k}\Omega/100} = 845\ \mu\text{A}$$

The collector-to-emitter voltage is

$$V_{CE} = V_{CC} - I_C R_C = 10\text{ V} - (845\ \mu\text{A})(10\text{ k}\Omega) = 1.55\text{ V}$$

Related Exercise Calculate the Q-point values in Figure 5–30 for $\beta_{DC} = 250$.

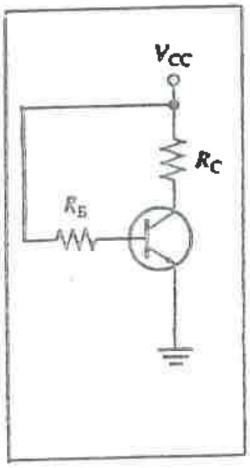
SECTION 5–5 REVIEW

1. Explain how an increase in β_{DC} causes a reduction in base current in a collector-feedback circuit.
2. In a certain collector-feedback circuit, $R_B = 47\text{ k}\Omega$, $R_C = 2.2\text{ k}\Omega$, and $V_{CC} = 15$ V. If $I_C = 5$ mA, what is I_B?

SUMMARY OF TRANSISTOR BIAS CIRCUITS

npn transistors are shown. Supply voltage polarities are reversed for *pnp* transistors.

BASE BIAS



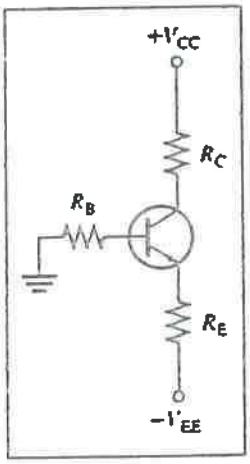
- Q-point values ($I_C \cong I_E$)
- Collector current:

$$I_C = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right)$$

- Collector-to-emitter voltage:

$$V_{CE} = V_{CC} - I_C R_C$$

EMITTER BIAS



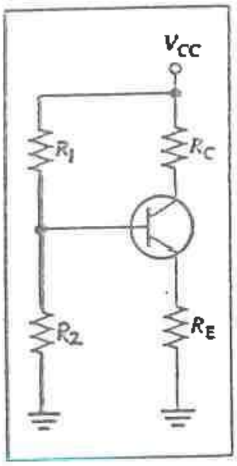
- Q-point values ($I_C \cong I_E$)
- Collector current:

$$I_C \cong \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta_{DC}}$$

- Collector-to-emitter voltage:

$$V_{CE} \cong V_{CC} + V_{EE} - I_C(R_C + R_E)$$

VOLTAGE-DIVIDER BIAS



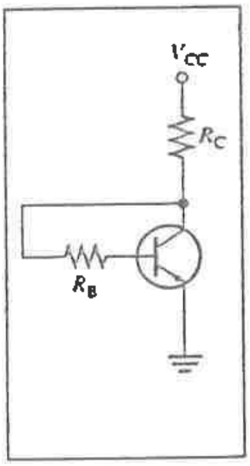
- Q-point values ($I_C \cong I_E$)
- Collector current:

$$I_C \cong \frac{\left(\frac{R_2}{R_1 + R_2}\right)V_{CC} - V_{BE}}{R_E}$$

- Collector-to-emitter voltage:

$$V_{CE} \cong V_{CC} - I_C(R_C + R_E)$$

COLLECTOR-FEEDBACK BIAS



- Q-point values ($I_C \cong I_E$)
- Collector current:

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + R_B/\beta_{DC}}$$

- Collector-to-emitter voltage:

$$V_{CE} = V_{CC} - I_C R_C$$