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# **Logic and Computer Design Fundamentals**

## **Sequential Circuits**

### **Part 1 - Storage Elements**

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# Overview

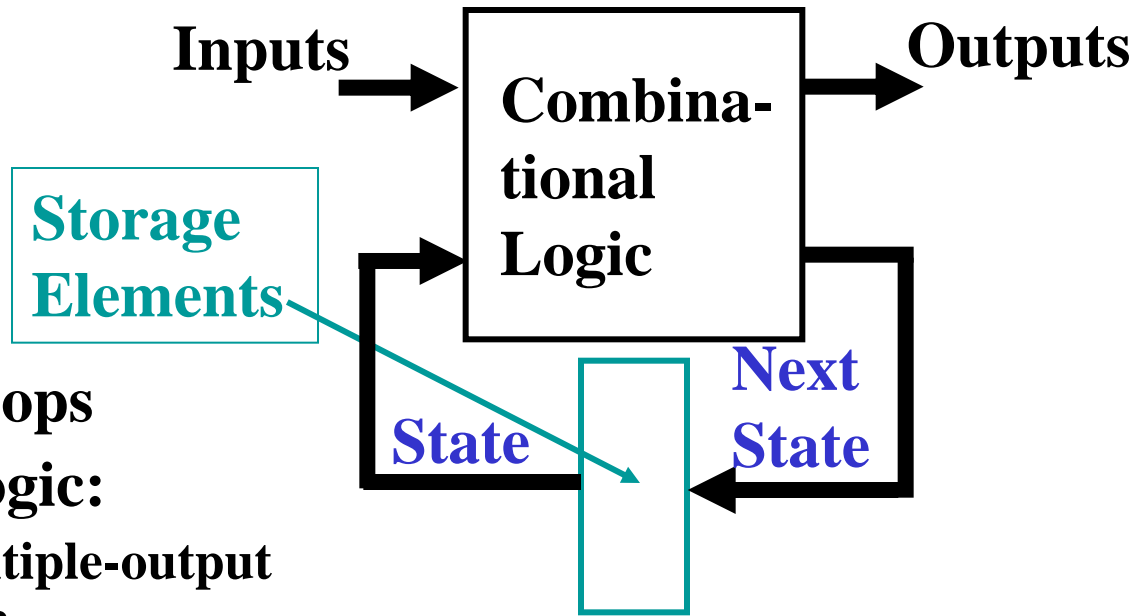
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- **Part 1 - Storage Elements**
  - **Introduction to sequential circuits**
  - **Types of sequential circuits**
  - **Storage elements**
    - **Latches**
    - **Flip-flops**
- **Part 2 - Sequential Circuit Analysis**
- **Part 3 - Sequential Circuit Design**
- **Part 4 – State Machine Design**

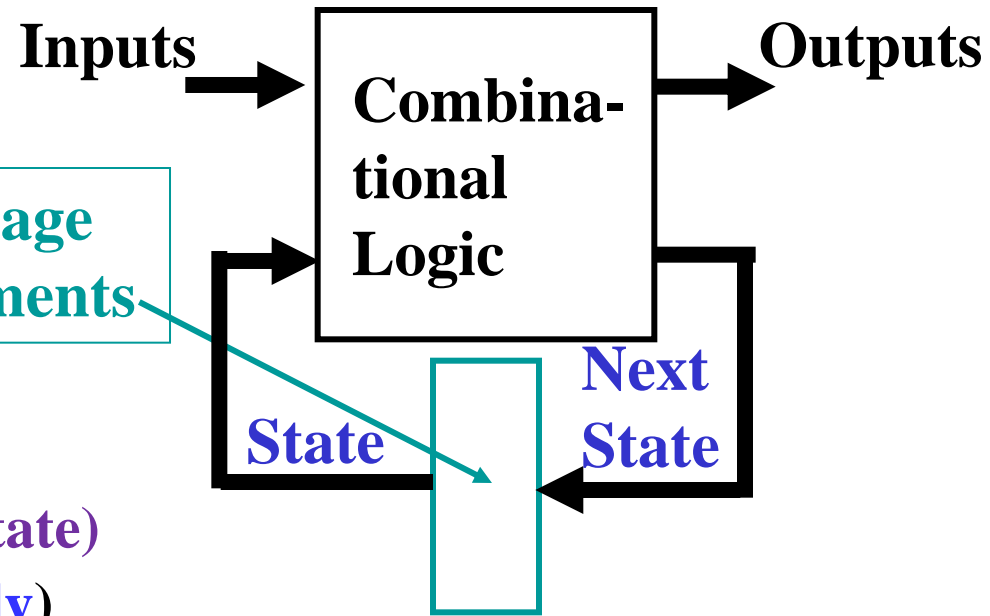
# Introduction to Sequential Circuits

- A Sequential circuit contains:

- Storage elements: Latches or Flip-Flops
- Combinational Logic:
  - Implements a multiple-output switching function
  - Inputs are signals from the outside.
  - Outputs are signals to the outside.
  - Other inputs, State or Present State, are signals from storage elements.
  - The remaining outputs, Next State are inputs to storage elements.



# Introduction to Sequential Circuits



- **Combinatorial Logic**
  - *Next state function*  
 $\text{Next State} = f(\text{Inputs}, \text{State})$
  - *Output function (Mealy)*  
 $\text{Outputs} = g(\text{Inputs}, \text{State})$
  - *Output function (Moore)*  
 $\text{Outputs} = h(\text{State})$
- **Output function type depends on specification and affects the design significantly**

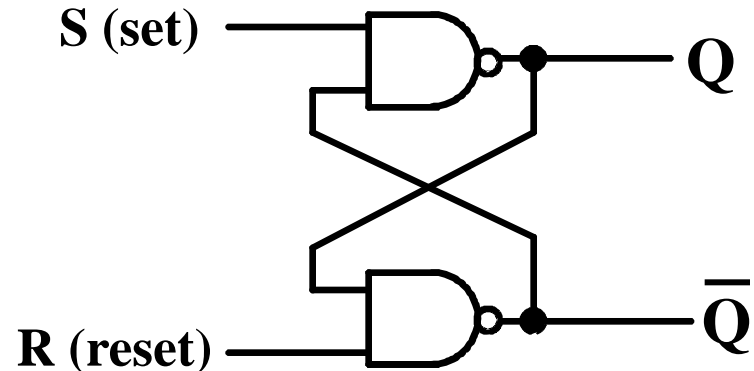
# Types of Sequential Circuits

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- Depends on the times at which:
  - storage elements observe their inputs, and
  - storage elements change their state
- Synchronous
  - Behavior defined from knowledge of its signals at discrete instances of time
  - Storage elements observe inputs and can **change state only in relation to a timing signal** (clock pulses from a clock)
- Asynchronous
  - Behavior defined from knowledge of inputs an **any instant of time** and the order in continuous time in which inputs change
  - Nevertheless, the synchronous abstraction makes **complex designs** tractable!

# Basic (NAND) $\bar{S}$ – $\bar{R}$ Latch

- “Cross-Coupling”  
two NAND gates gives  
the  $\bar{S}$  - $\bar{R}$  Latch:



- Which has the time  
sequence behavior:

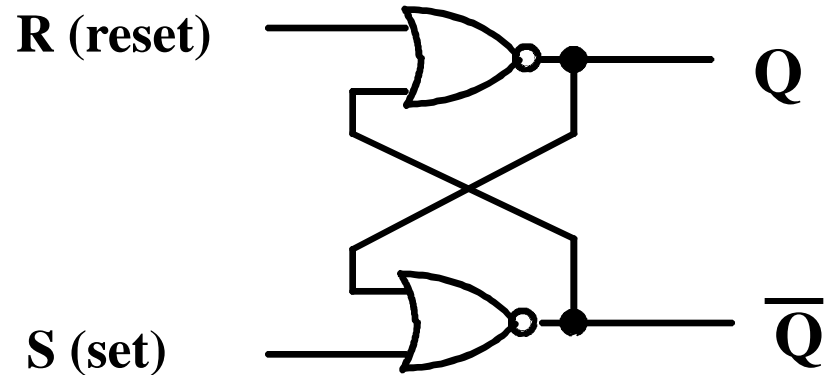
Time

R	S	Q	$\bar{Q}$	Comment
1	1	?	?	Stored state unknown
1	0	1	0	“Set” Q to 1
1	1	1	0	Now Q “remembers” 1
0	1	0	1	“Reset” Q to 0
1	1	0	1	Now Q “remembers” 0
0	0	1	1	Both go high
1	1	?	?	Unstable!

- $S = 0, R = 0$  is  
forbidden as  
input pattern

# Basic (NOR) S – R Latch

- Cross-coupling two NOR gates gives the S – R Latch:
- Which has the time sequence behavior:

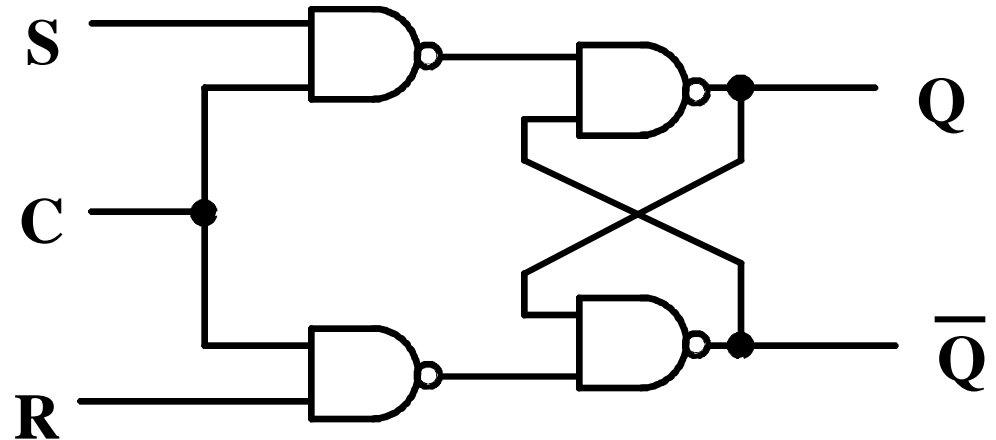


Time ↓

R	S	Q	$\bar{Q}$	Comment
0	0	?	?	Stored state unknown
0	1	1	0	“Set” Q to 1
0	0	1	0	Now Q “remembers” 1
1	0	0	1	“Reset” Q to 0
0	0	0	1	Now Q “remembers” 0
1	1	0	0	Both go low
0	0	?	?	Unstable!

# Clocked S - R Latch

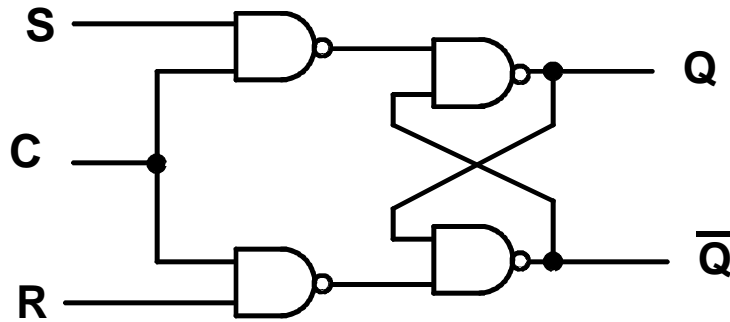
- Adding two NAND gates to the basic  $\overline{S}$  -  $\overline{R}$  NAND latch gives the clocked S - R latch:



- Has a time sequence behavior similar to the basic S-R latch except that the S and R inputs are only observed when the line C is high.
- C means “control” or “clock”.

# Clocked S - R Latch (continued)

- The Clocked S-R Latch can be described by a table:



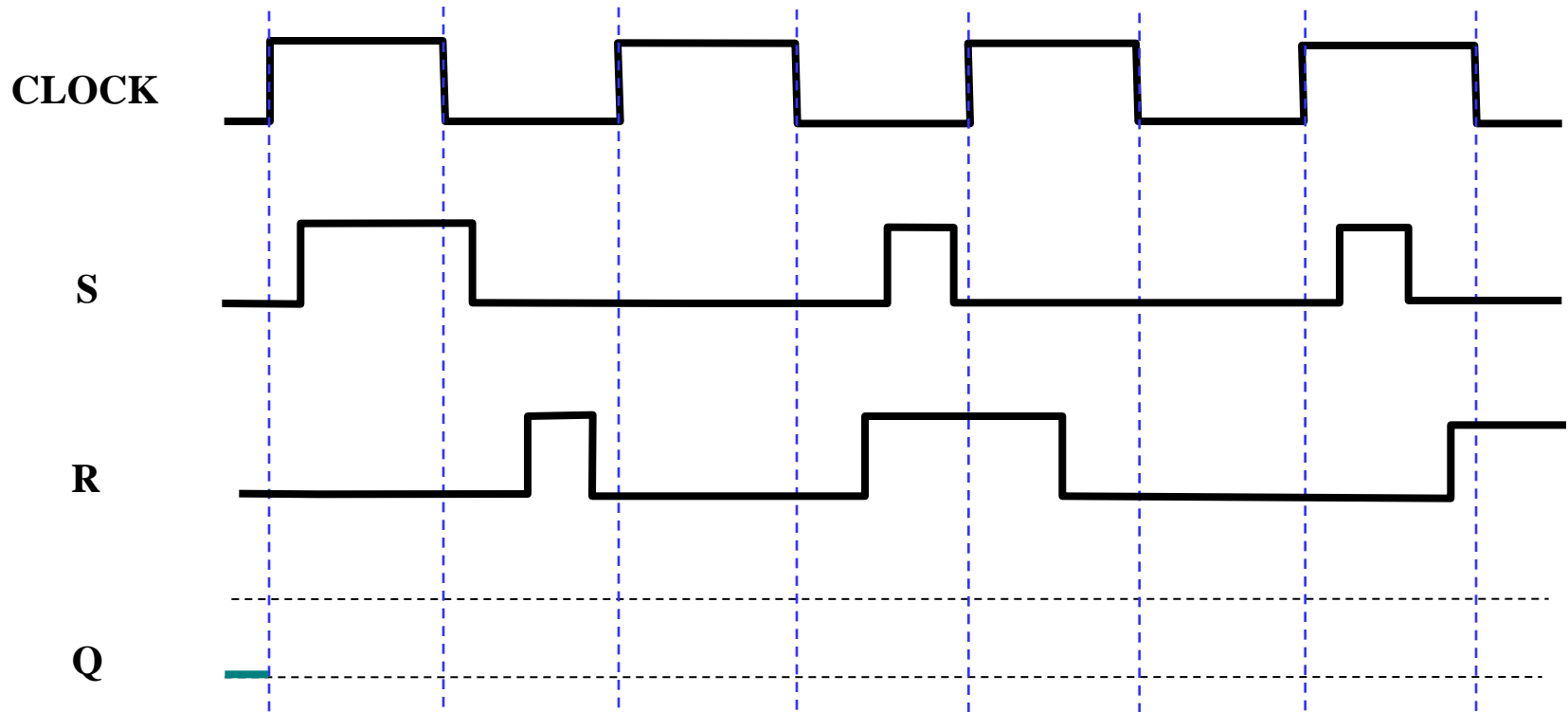
Q(t)	S	R	Q(t+1)	Comment
0	0	0	0	No change
0	0	1	0	Clear Q
0	1	0	1	Set Q
0	1	1	???	Indeterminate
1	0	0	1	No change
1	0	1	0	Clear Q
1	1	0	1	Set Q
1	1	1	???	Indeterminate

- The table describes what happens after the clock [at time (t+1)] based on:

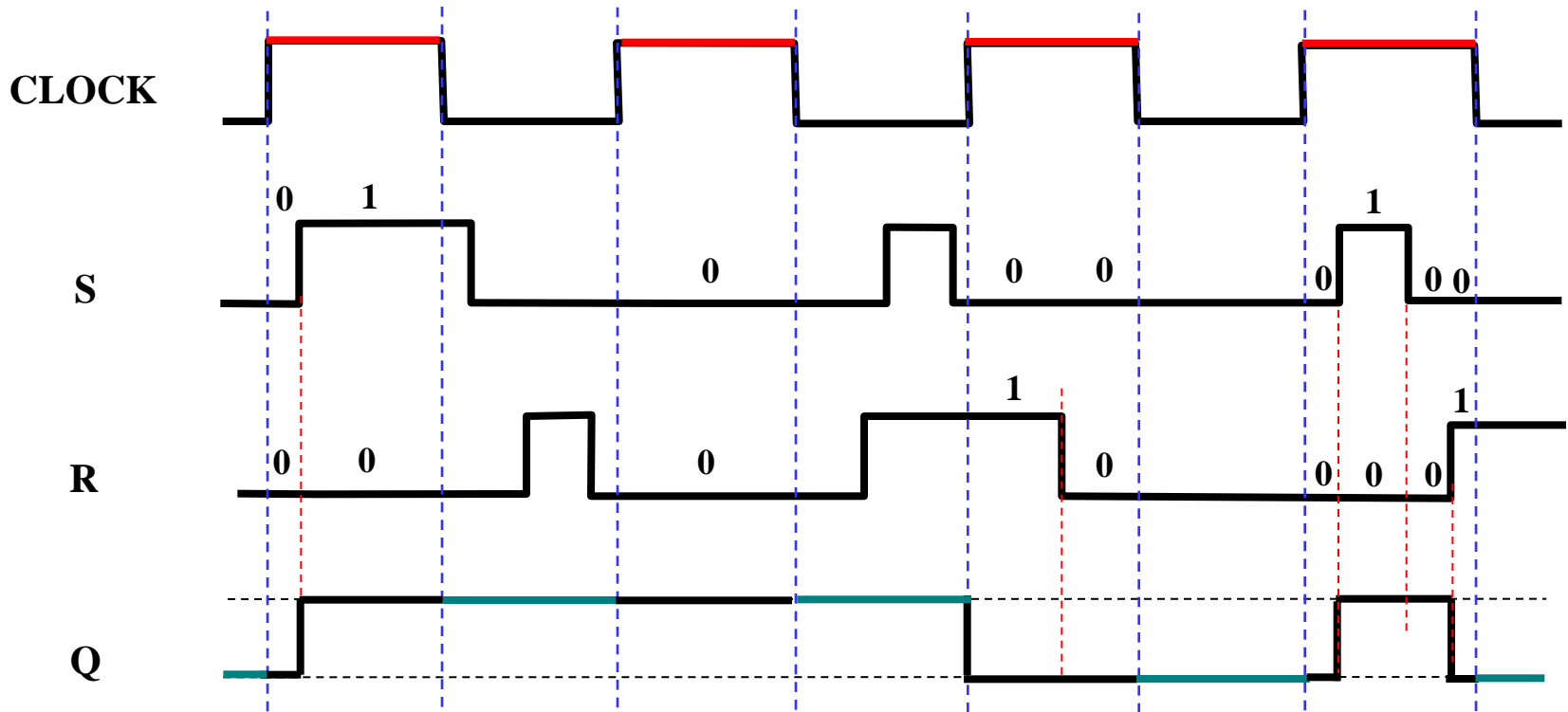
- current inputs (S,R) and
- current state Q(t).

# Clocked S - R Latch – Example 1

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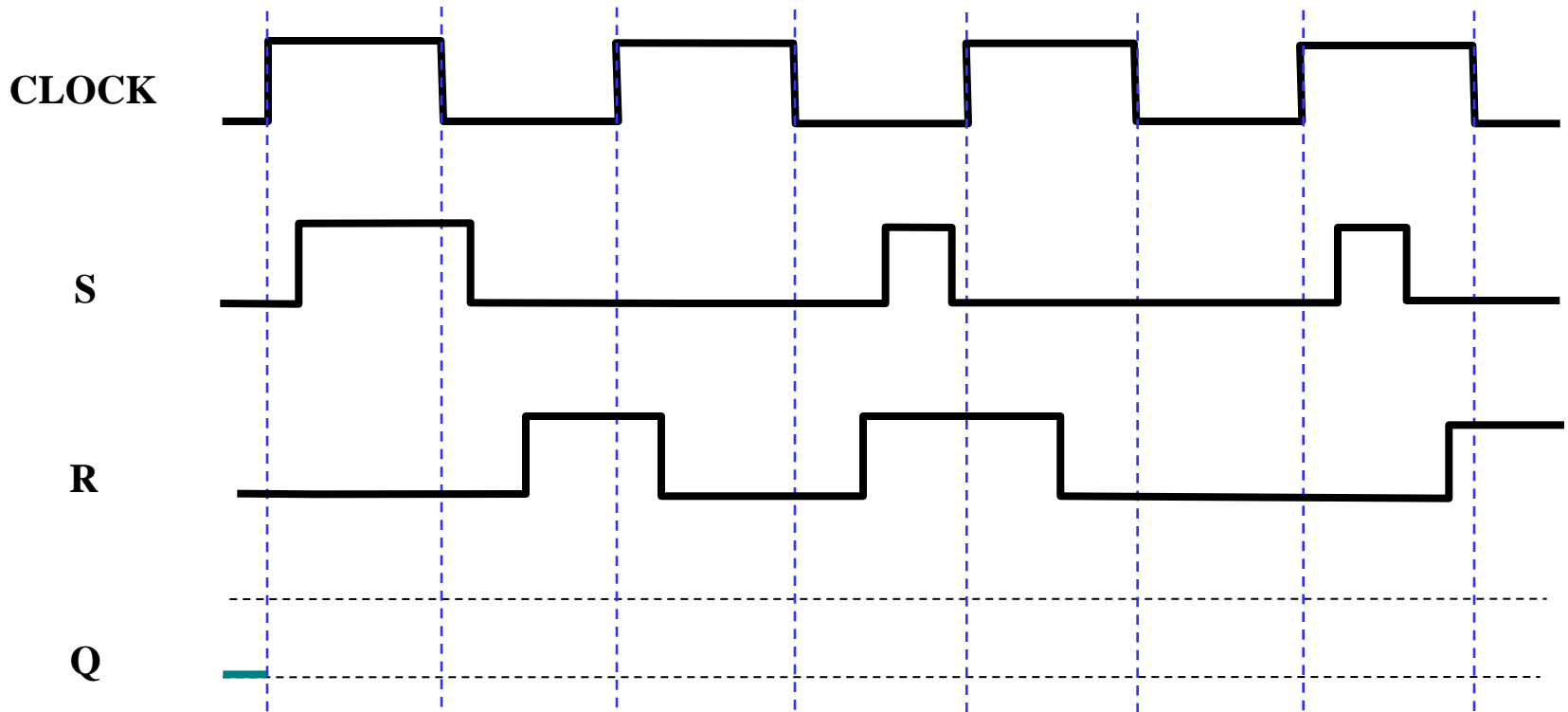


# Clocked S - R Latch – Example 1

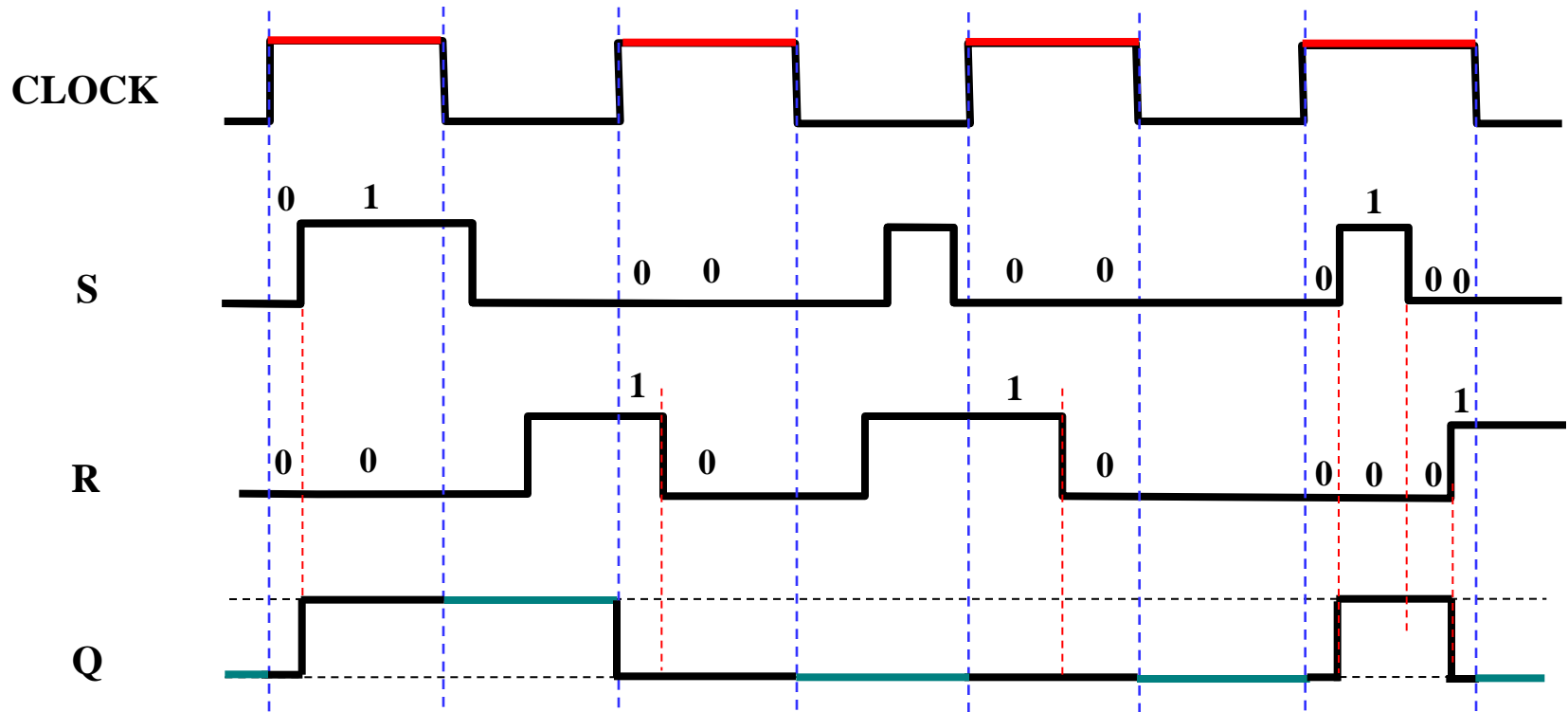


# Clocked S - R Latch – Example 2

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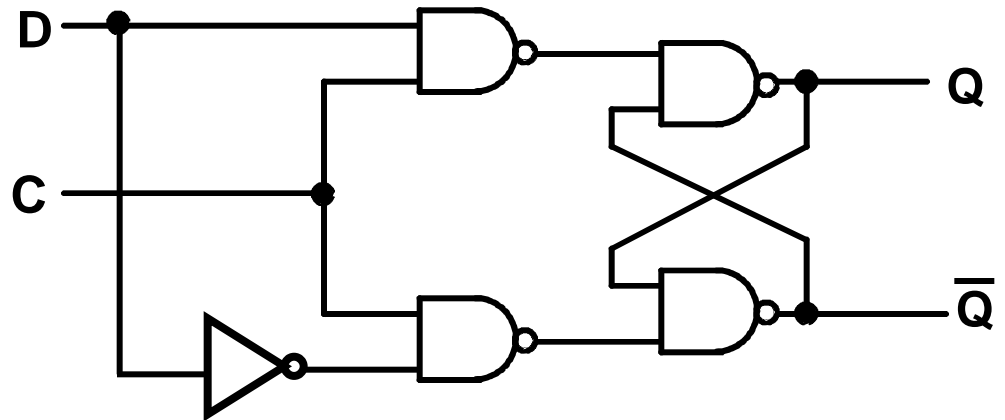


# Clocked S - R Latch – Example 2

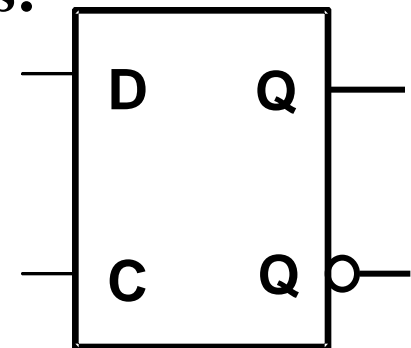


# D Latch

- Adding an inverter to the S-R Latch, gives the D Latch:
- Note that there are no “indeterminate” states!



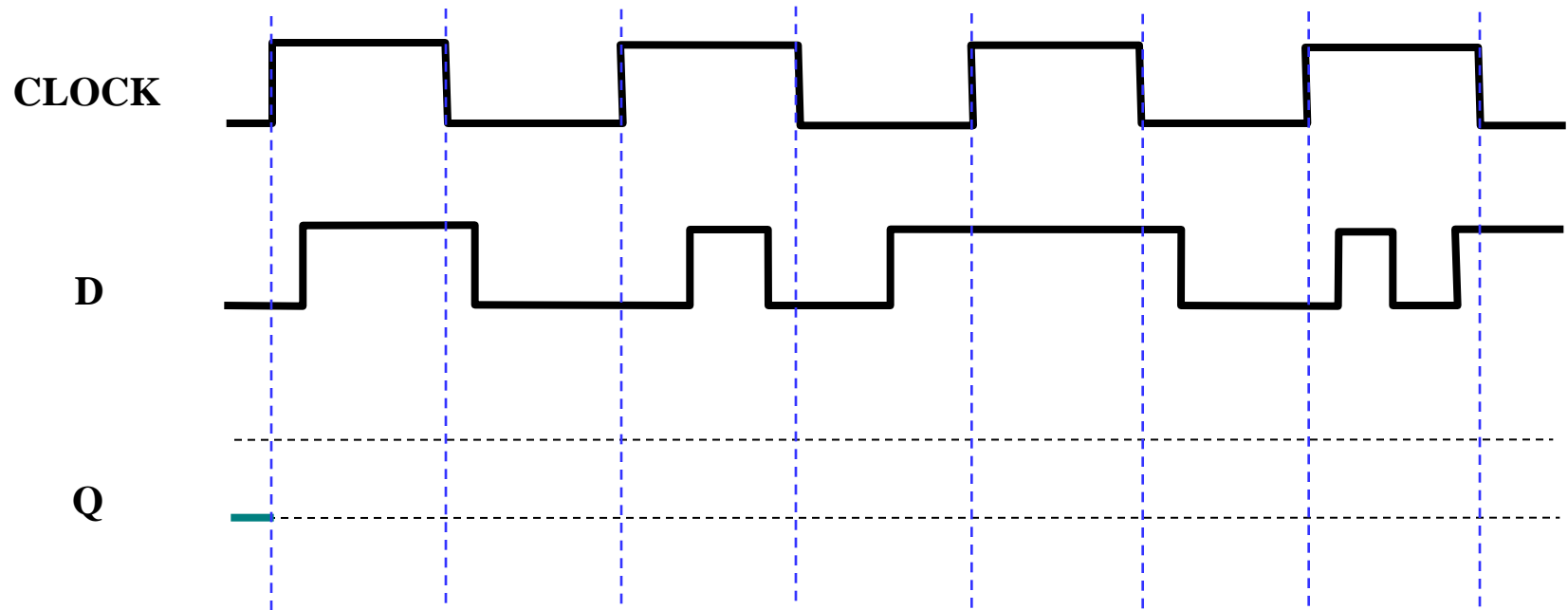
The graphic symbol for a D Latch is:



Q	D	Q(t+1)	Comment
0	0	0	No change
0	1	1	Set Q
1	0	0	Clear Q
1	1	1	No Change

# D Latch – Example 1

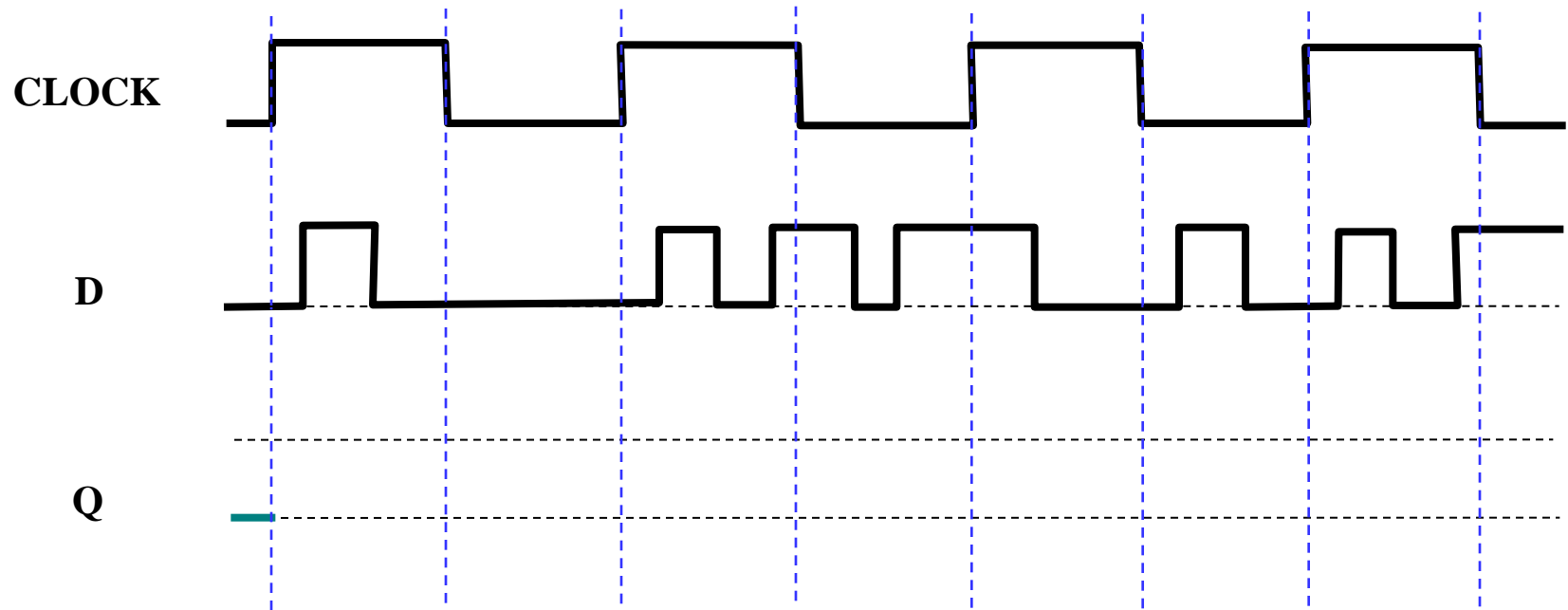
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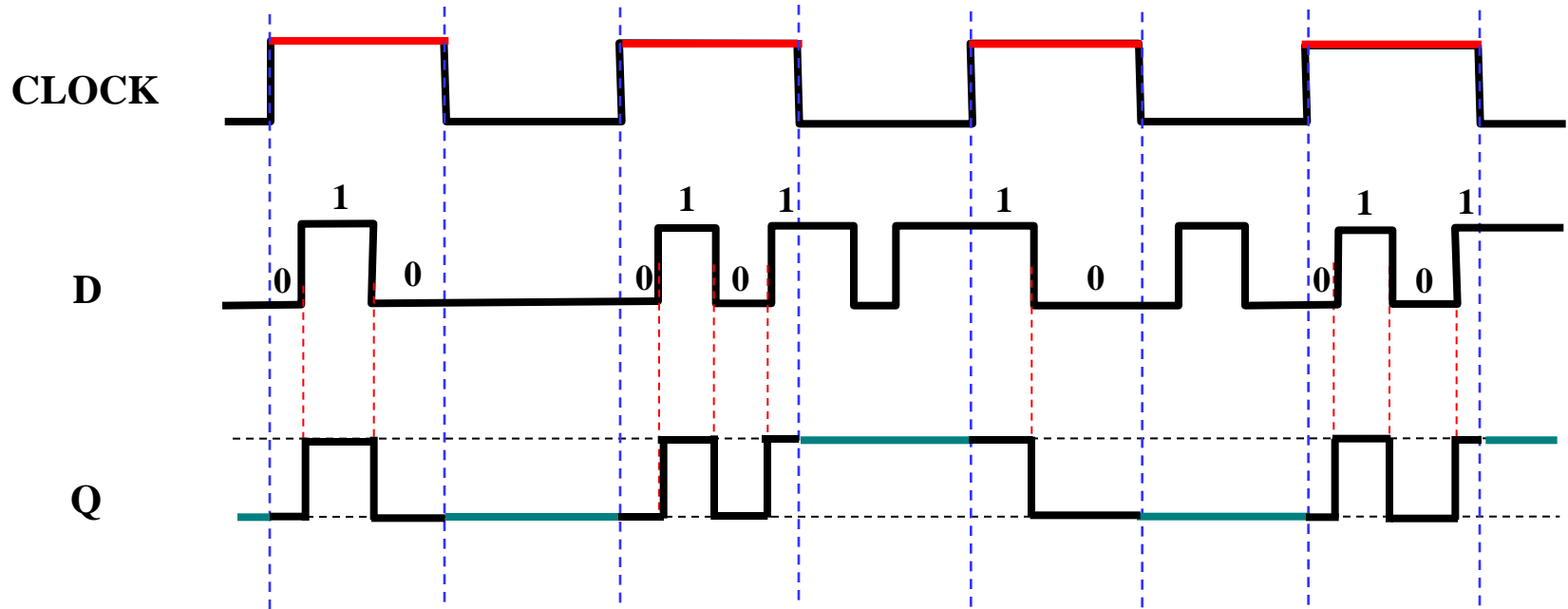


# D Latch – Example 2

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# D Latch – Example 2



# Flip-Flops

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- **The latch timing problem**
- **Master-slave flip-flop**
- **Edge-triggered flip-flop**
- **Standard symbols for storage elements**
- **Direct inputs to flip-flops**

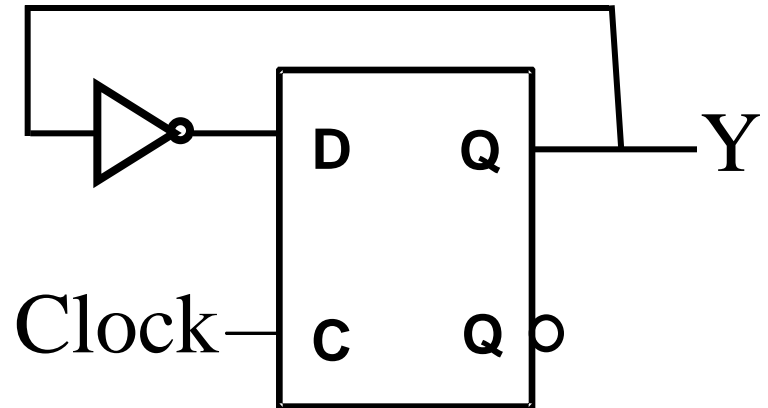
# The Latch Timing Problem

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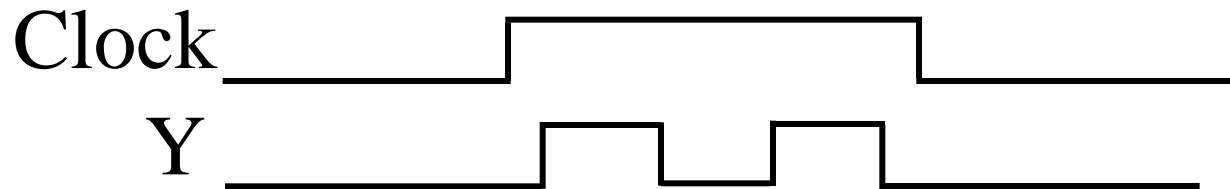
- **In a sequential circuit, paths may exist through combinational logic:**
  - **From one storage element to another**
  - **From a storage element back to the same storage element**
- **The combinational logic between a latch output and a latch input may be as simple as an interconnect**
- **For a clocked D-latch, the output  $Q$  depends on the input  $D$  whenever the clock input  $C$  has value 1**

# The Latch Timing Problem (continued)

- Consider the following circuit:



- Suppose that initially  $Y = 0$ .



- As long as  $C = 1$ , the value of  $Y$  continues to change!
- The changes are based on the delay present on the loop through the connection from  $Y$  back to  $Y$ .
- This behavior is clearly unacceptable.
- **Desired behavior:  $Y$  changes only once per clock pulse**

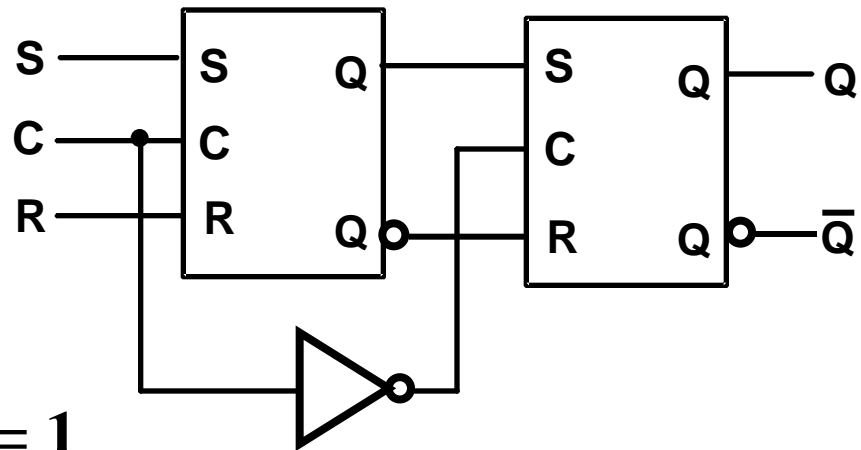
# The Latch Timing Problem (continued)

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- A solution to the latch timing problem is to break the closed path from Y to Y within the storage element
- The commonly-used, path-breaking solutions replace the clocked D-latch with:
  - a master-slave flip-flop
  - an edge-triggered flip-flop

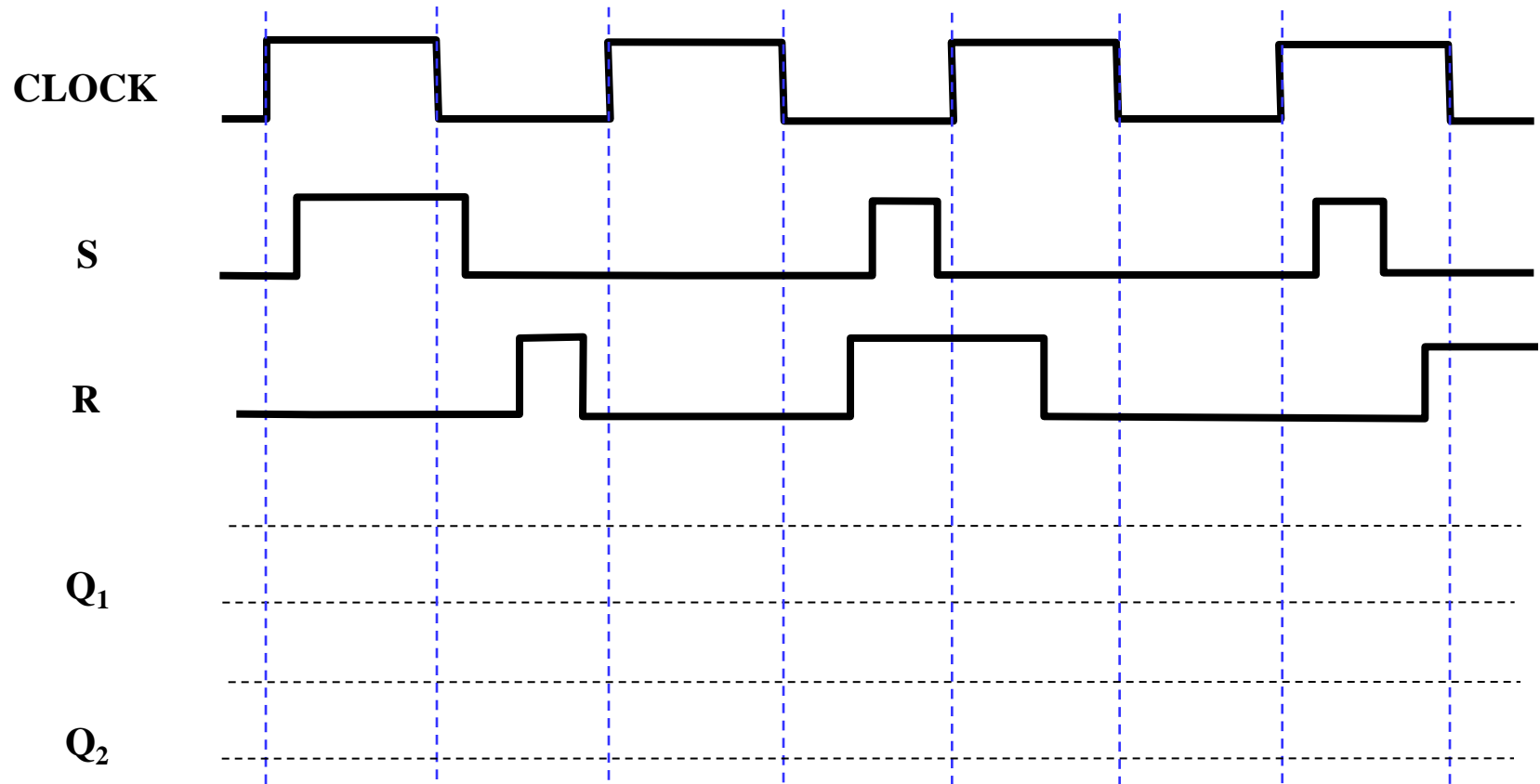
# S-R Master-Slave Flip-Flop

- Consists of two clocked S-R latches in series with the clock on the second latch inverted
- The input is observed by the first latch with  $C = 1$
- The output is changed by the second latch with  $C = 0$
- The path from input to output is broken by the difference in clocking values ( $C = 1$  and  $C = 0$ ).
- The behavior demonstrated by the example with D driven by Y given previously is prevented since the clock must change from 1 to 0 before a change in Y based on D can occur.

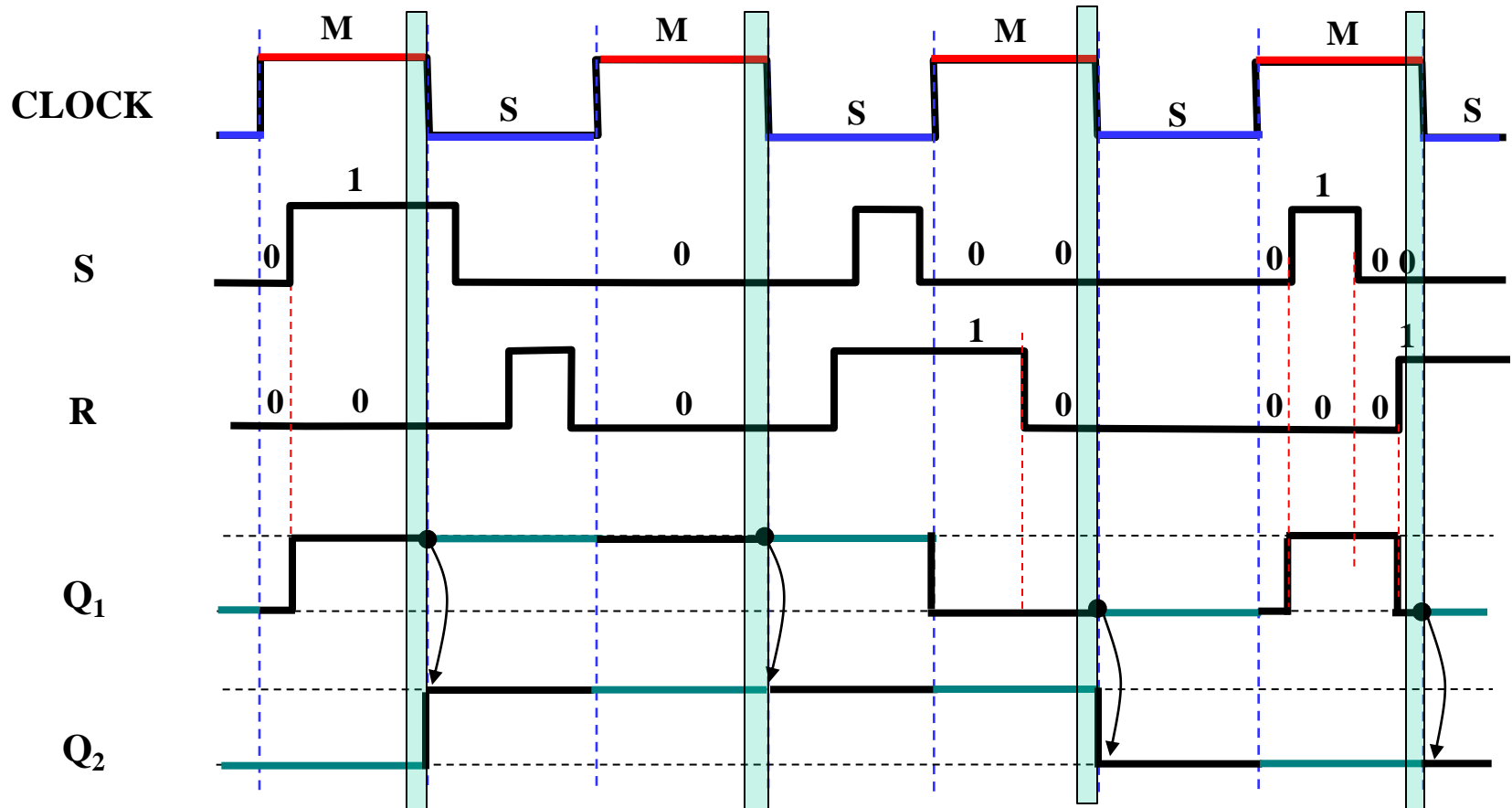


# S-R Master-Slave Flip-Flop – Example 1

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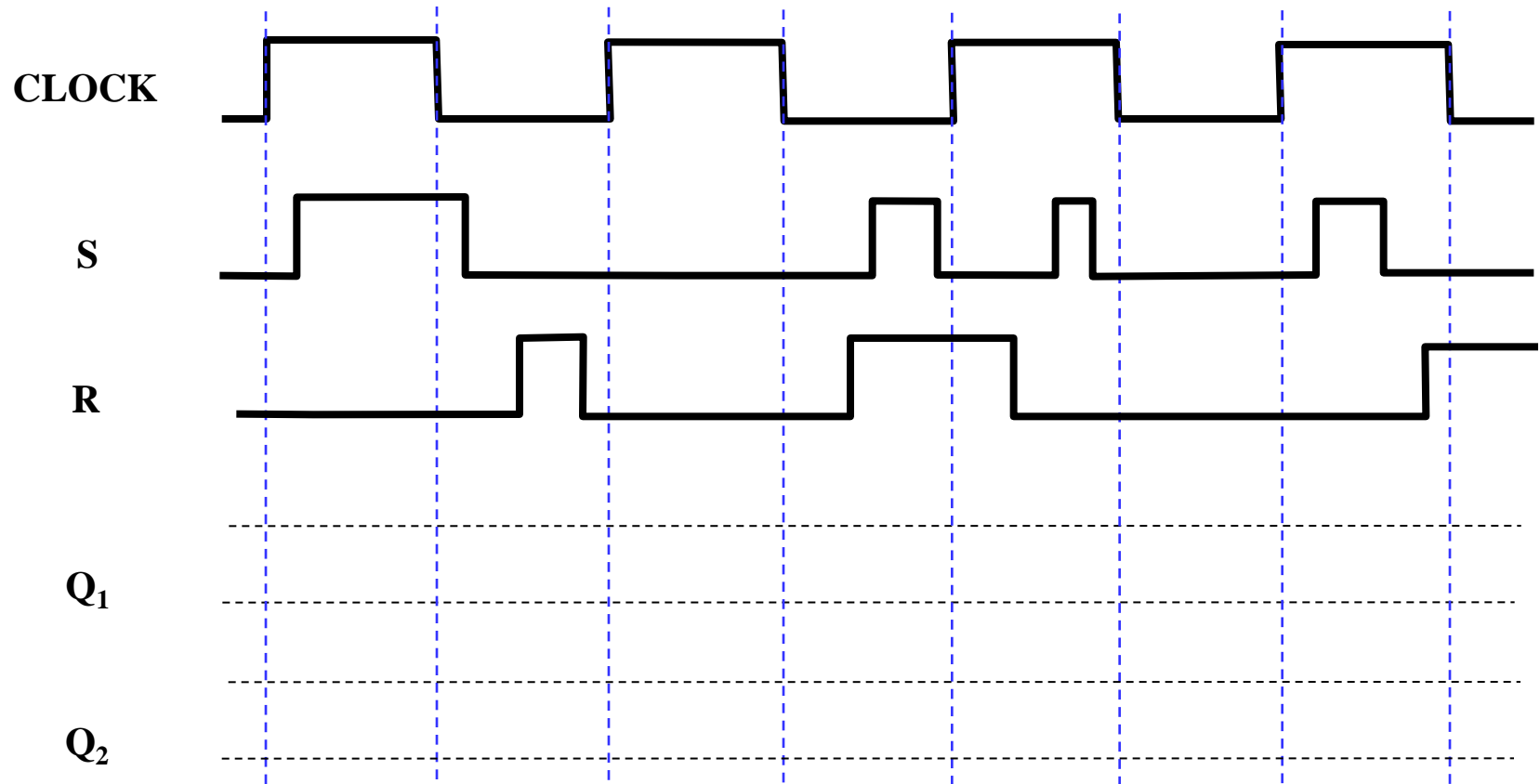


# S-R Master-Slave Flip-Flop – Example 1

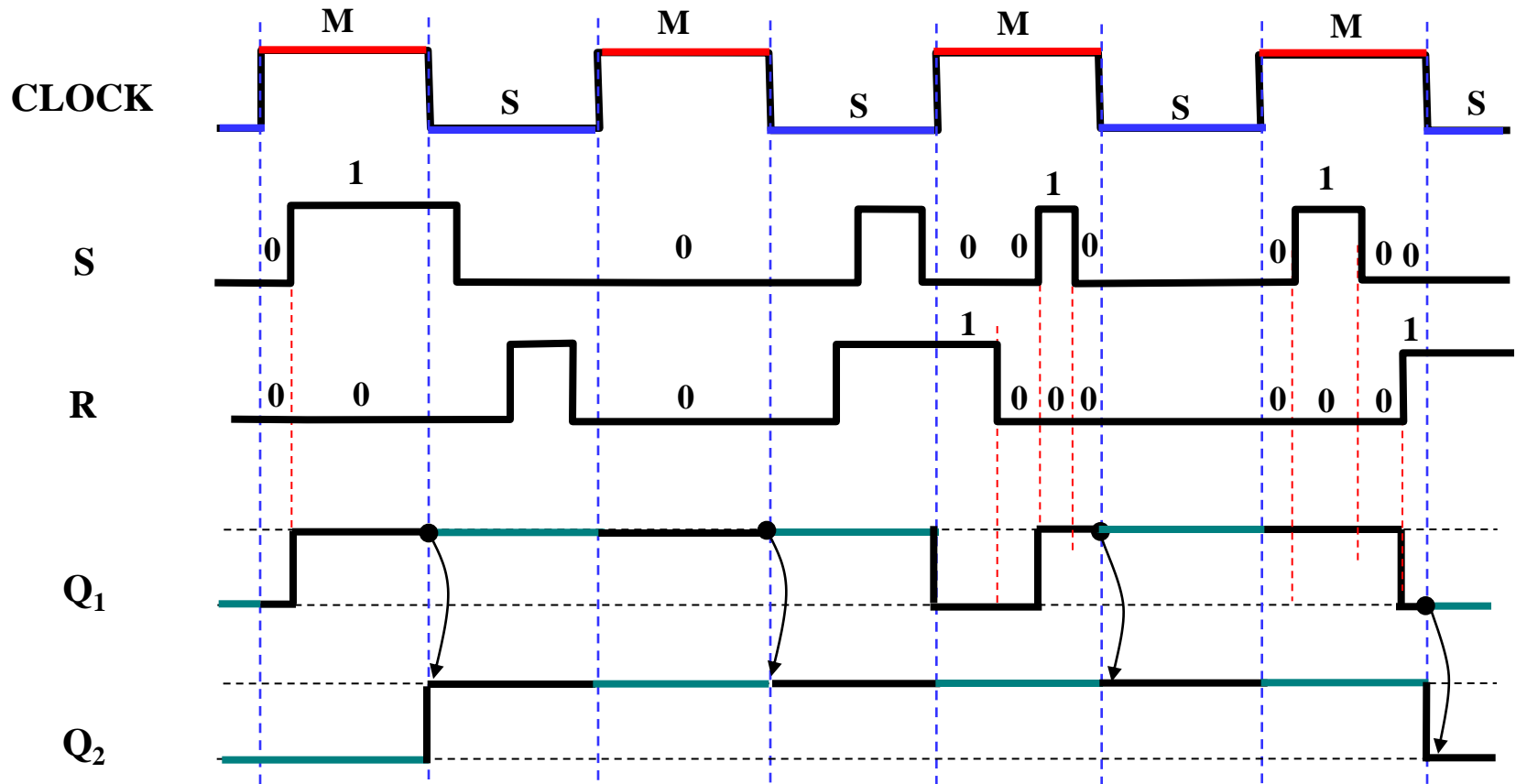


# S-R Master-Slave Flip-Flop – Example 2

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# S-R Master-Slave Flip-Flop – Example 2



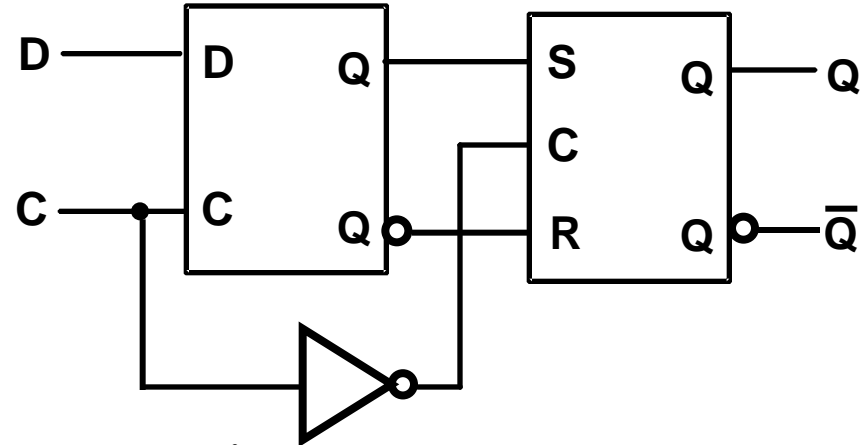
# Flip-Flop Solution

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- Use edge-triggering instead of master-slave
- An *edge-triggered* flip-flop **ignores the pulse while it is at a constant level** and **triggers only during a transition** of the clock signal
- Edge-triggered flip-flops can **be built** directly at the **electronic circuit level**, **or**
- A **master-slave D flip-flop** which **also exhibits edge-triggered behavior** can be used.

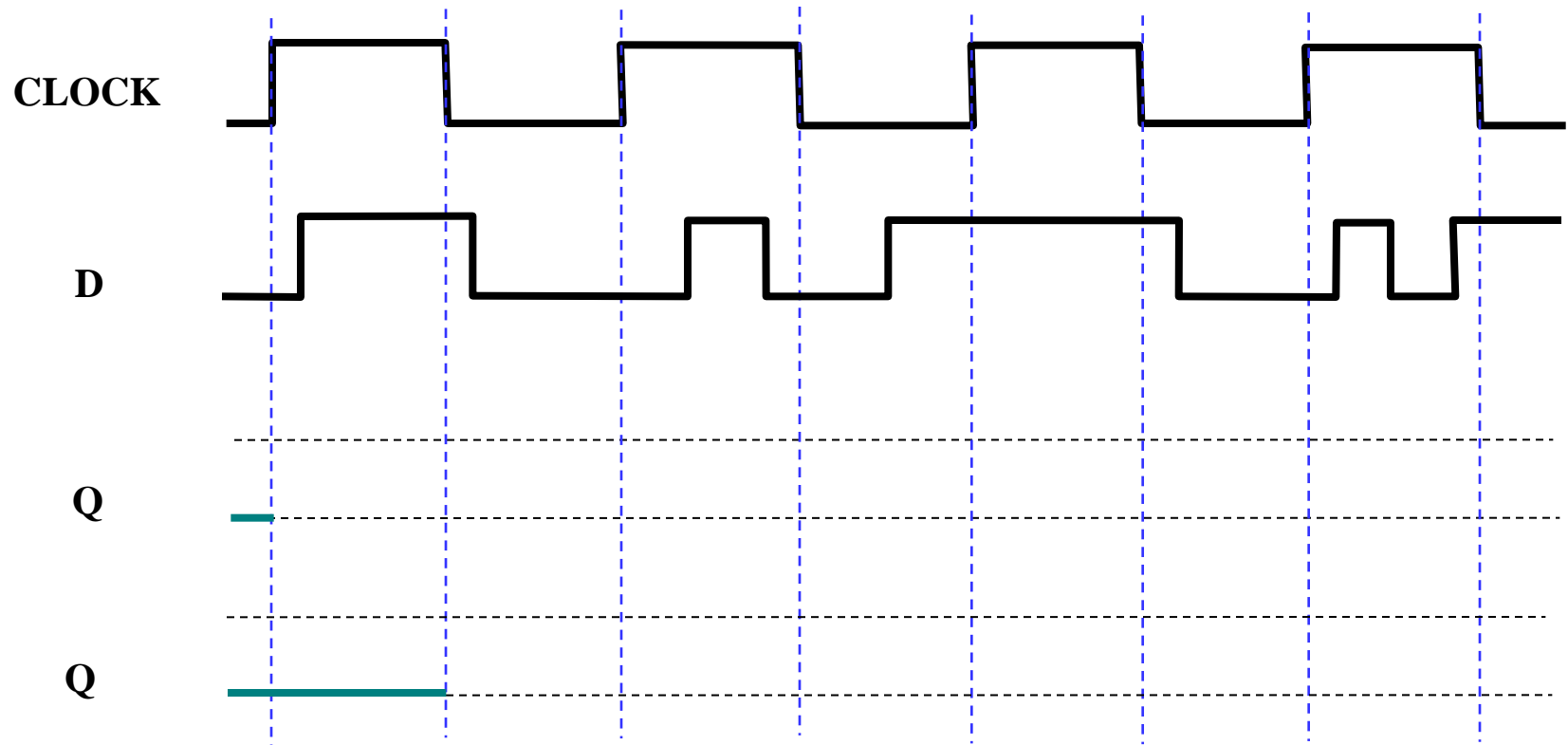
# Edge-Triggered D Flip-Flop

- The edge-triggered D flip-flop is the same as the master-slave D flip-flop
- It can be formed by:
  - Replacing the first clocked S-R latch with a clocked D latch or
  - Adding a D input and inverter to a master-slave S-R flip-flop
- The delay of the S-R master-slave flip-flop can be avoided since the 1s-catching behavior is not present with D replacing S and R inputs
- The change of the D flip-flop output is associated with the **negative edge (falling edge)** at the end of the pulse
- It is called a *negative-edge triggered* flip-flop



# Edge-Triggered D Flip-Flop – Example 1

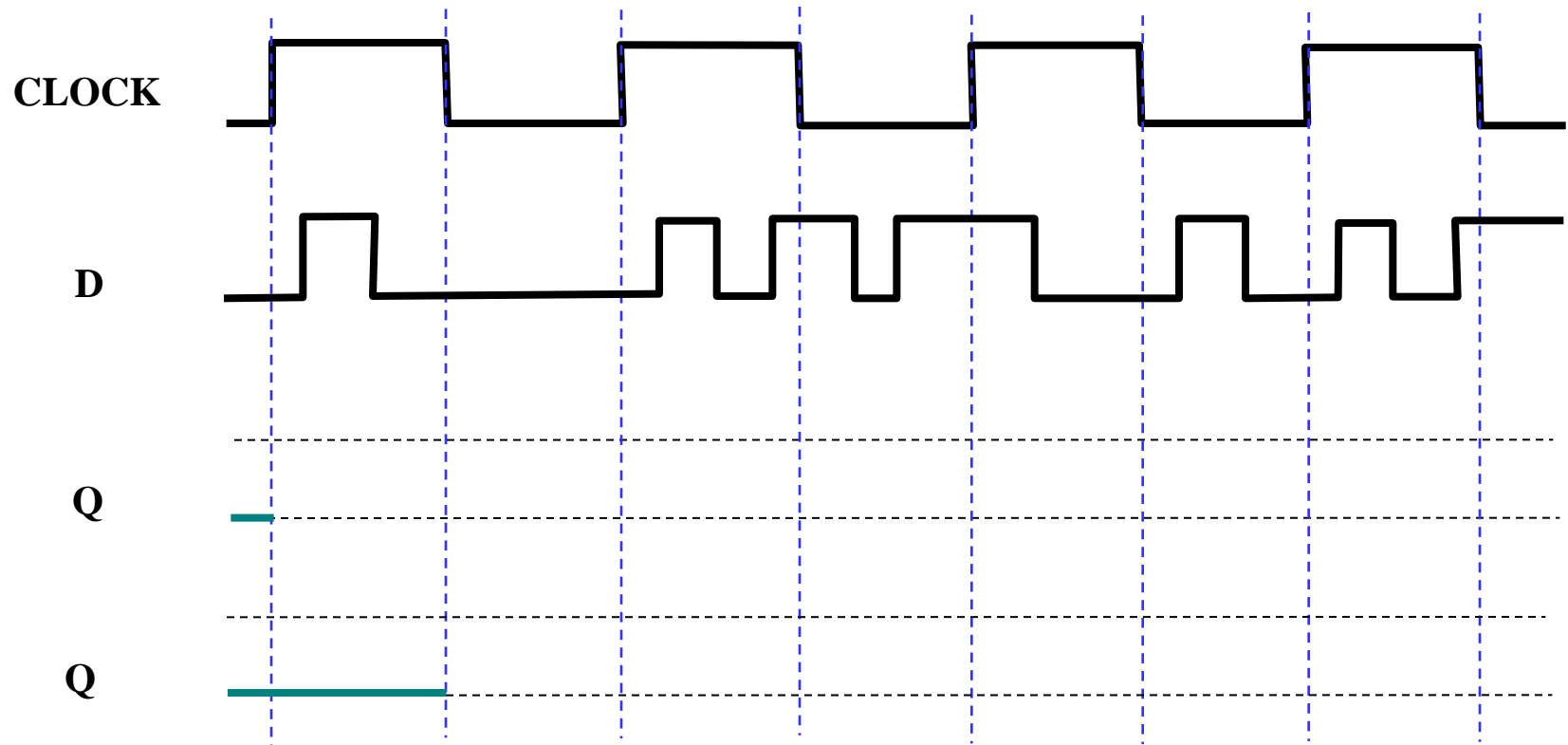
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# Edge-Triggered D Flip-Flop – Example 2

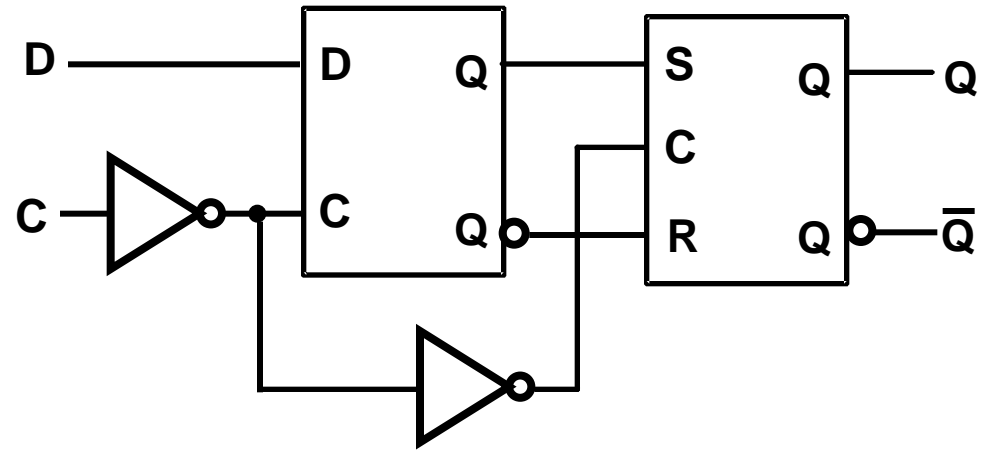
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# Positive-Edge Triggered D Flip-Flop

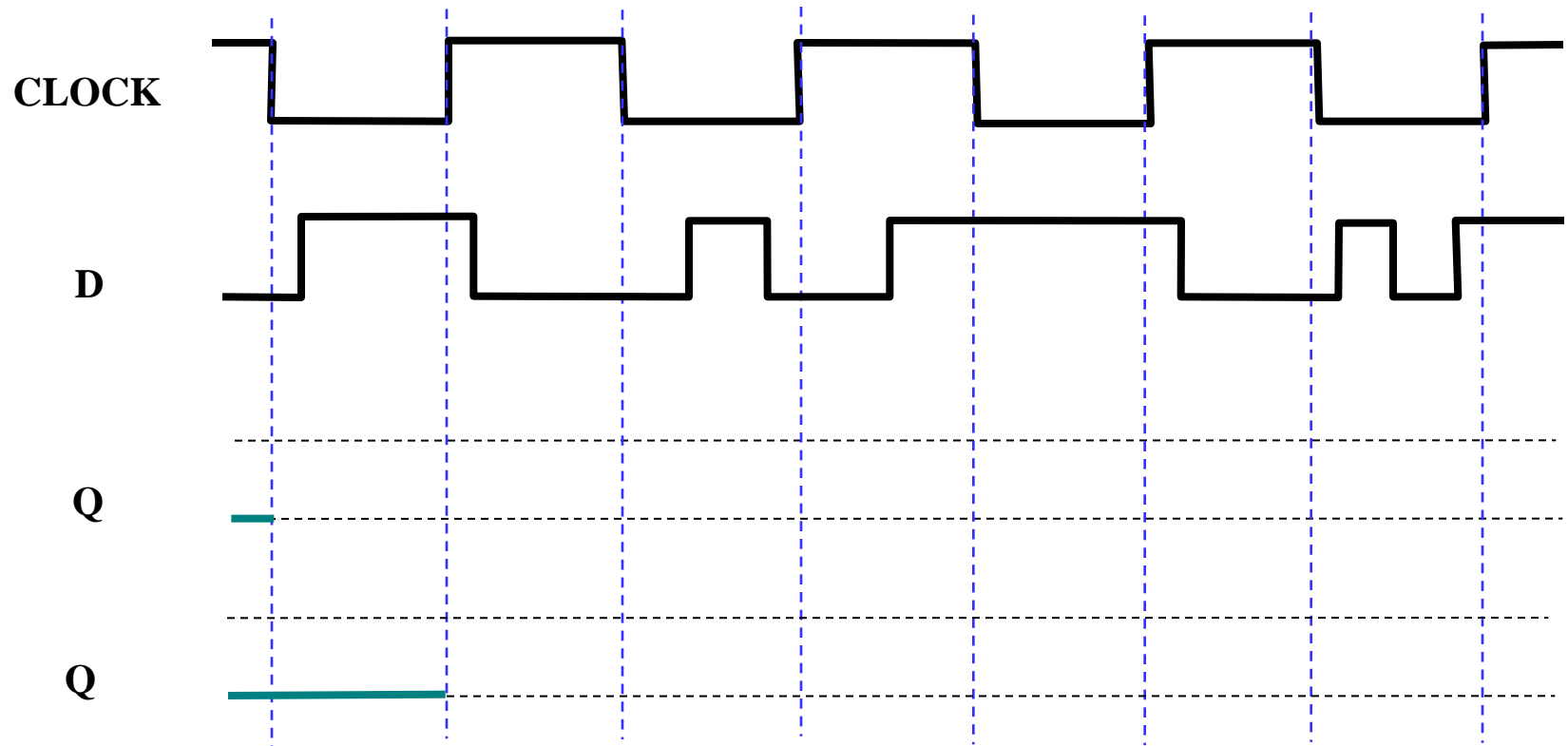
- Formed by adding inverter to clock input



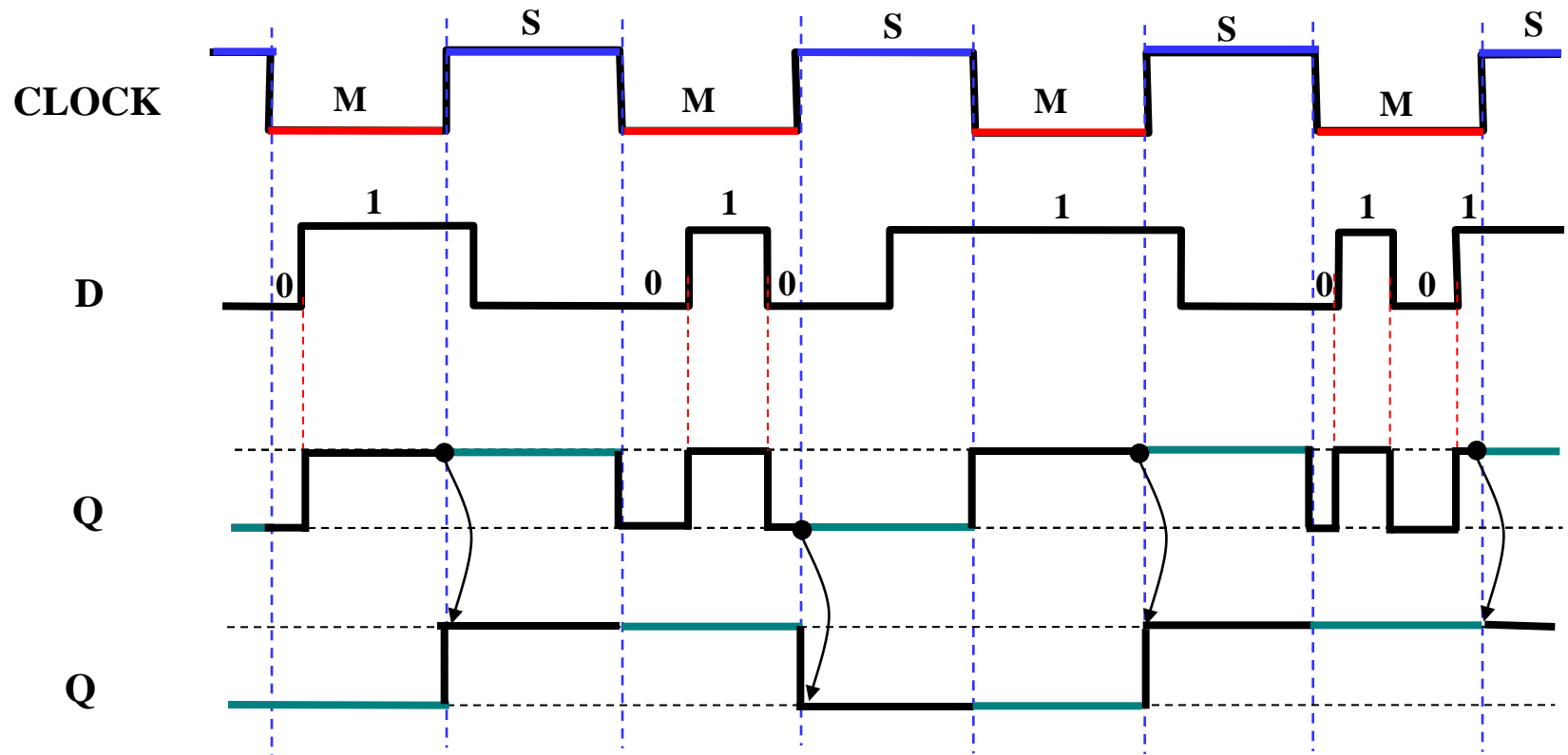
- Q changes to the value on D applied at the **positive clock (rising edge)** edge within timing constraints to be specified
- Our choice as the standard flip-flop for most sequential circuits

# Positive-Edge Triggered D Flip-Flop – Example 1

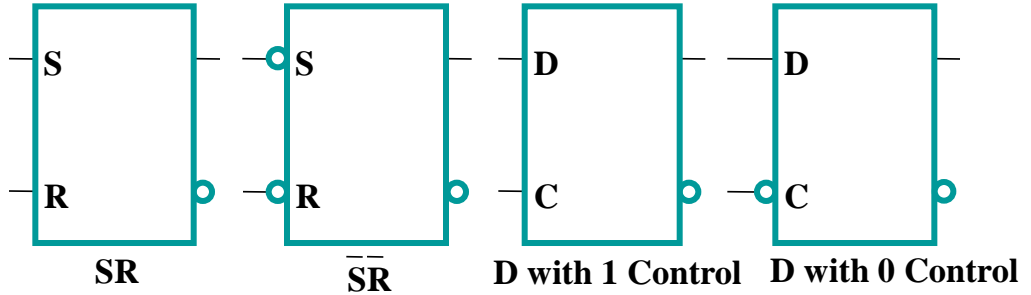
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# Positive-Edge Triggered D Flip-Flop – Example 1

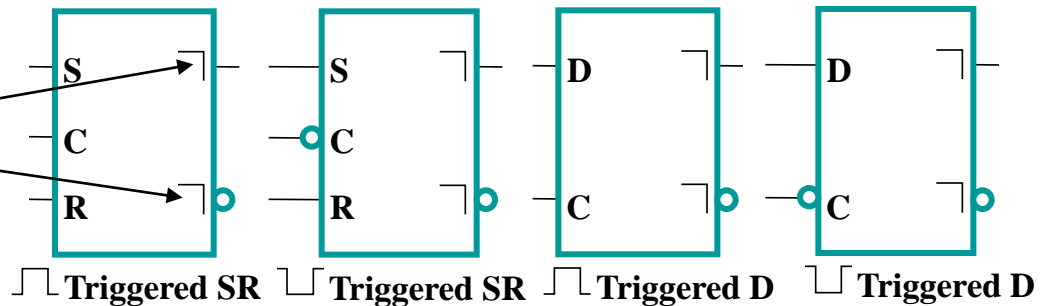


# Standard Symbols for Storage Elements



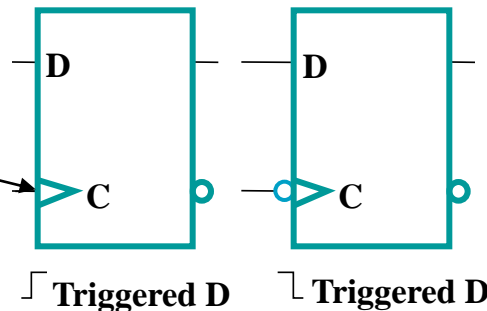
(a) Latches

- **Master-Slave:**  
Postponed output indicators



(b) Master-Slave Flip-Flops

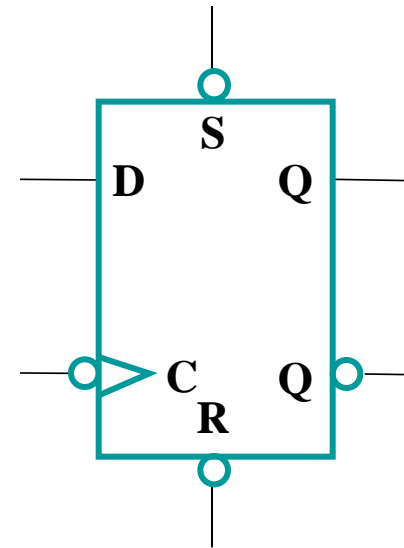
- **Edge-Triggered:**  
Dynamic indicator



(c) Edge-Triggered Flip-Flops

# Direct Inputs

- At power up or at reset, all or part of a sequential circuit usually is initialized to a known state before it begins operation
- This initialization is often done outside of the clocked behavior of the circuit, i.e., **asynchronously**.
- Direct R and/or S inputs that control the state of the latches within the flip-flops are used for this initialization.
- For the example flip-flop shown
  - **0 applied to  $\overline{R}$  resets the flip-flop to the 0 state**
  - **0 applied to  $\overline{S}$  sets the flip-flop to the 1 state**



# Other Flip-Flop Types

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- **J-K and T flip-flops**
  - Behavior
  - Implementation
- **Basic descriptors for understanding and using different flip-flop types**
  - Characteristic tables
  - Characteristic equations
  - Excitation tables
- **For actual use, see Reading Supplement - Design and Analysis Using J-K and T Flip-Flops**

# J-K Flip-flop

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## ■ Behavior

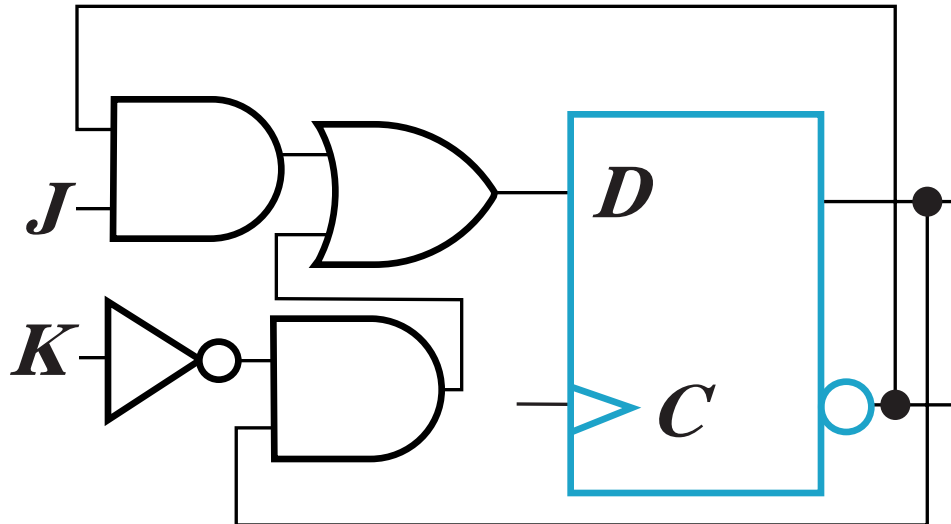
- Same as S-R flip-flop with J analogous to S and K analogous to R
- Except that  $J = K = 1$  is allowed, and
- **For  $J = K = 1$ , the flip-flop changes to the *opposite state***
- As a master-slave, has same “**1s catching**” behavior as S-R flip-flop
- If the master changes to the wrong state, that state will be passed to the slave
  - E.g., if master falsely set by  $J = 1, K = 1$  cannot reset it during the current clock cycle



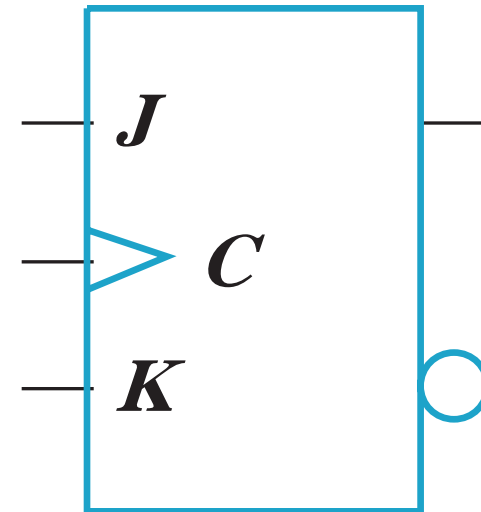
# J-K Flip-flop (continued)

## Implementation

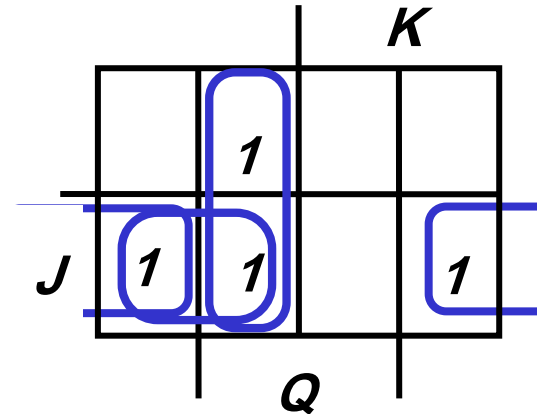
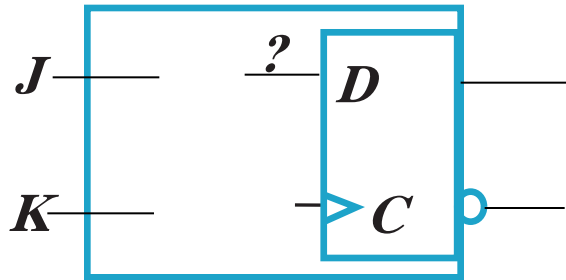
- To avoid 1s catching behavior, one solution used is to use an **edge-triggered D** as the core of the flip-flop



## Symbol

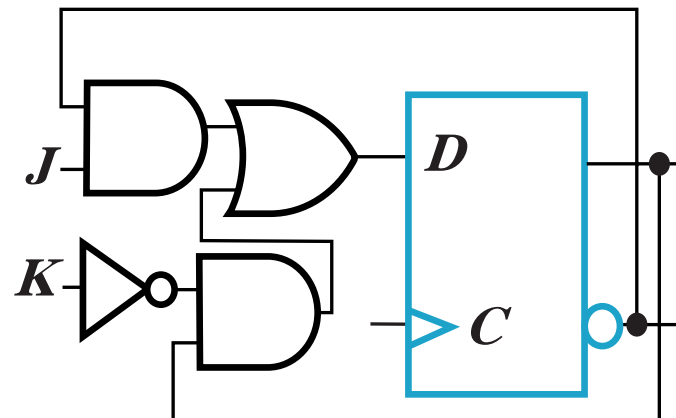


# J-K Flip-flop (continued)



$$D = JQ' + K'Q$$

J	K	Q	Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



# T Flip-flop

---

- **Behavior**

- **Has a single input T**

- **For  $T = 0$ , no change to state**
- **For  $T = 1$ , changes to opposite state**

- **Same as a J-K flip-flop with  $J = K = T$**

- **As a master-slave, has same “1s catching” behavior as J-K flip-flop**

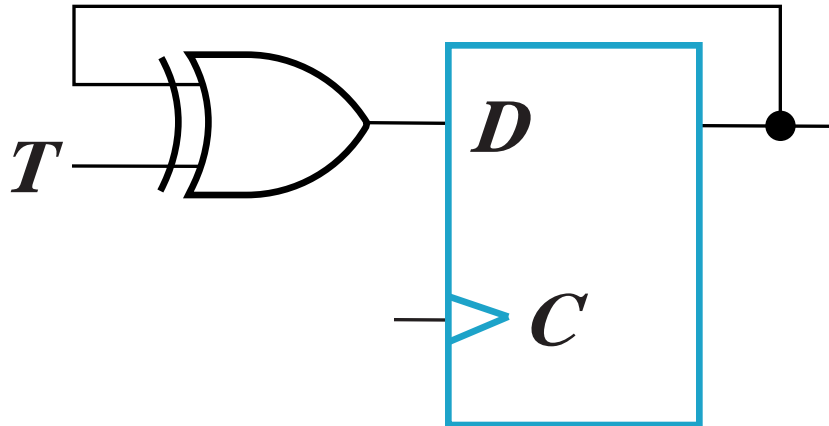
- **Cannot be initialized to a known state using the T input**

- **Reset (asynchronous or synchronous) essential**

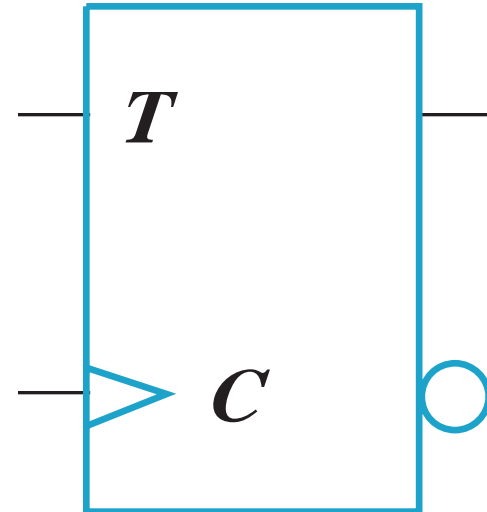
# T Flip-flop (continued)

## Implementation

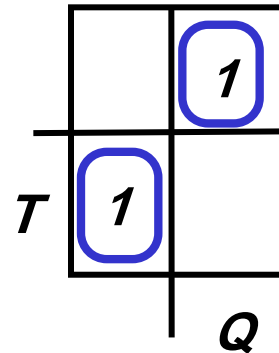
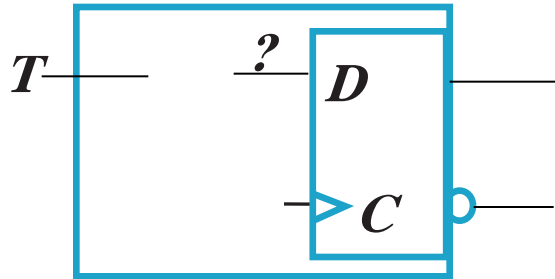
- To avoid 1s catching behavior, one solution used is to use an **edge-triggered D** as the core of the flip-flop



## Symbol

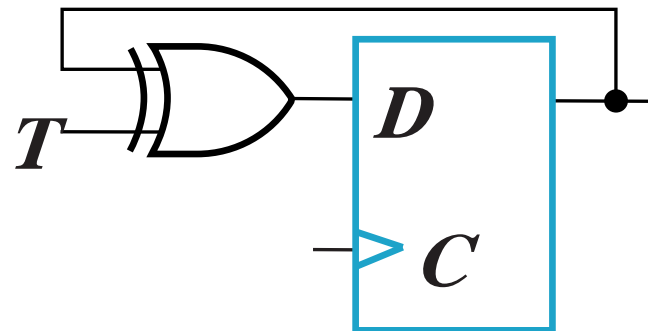


# T Flip-flop (continued)



$$D = T \oplus Q$$

T	Q	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0



# Basic Flip-Flop Descriptors

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- **Used in analysis**
  - ***Characteristic table*** - defines the next state of the flip-flop in terms of flip-flop inputs and current state
  - ***Characteristic equation*** - defines the next state of the flip-flop as a Boolean function of the flip-flop inputs and the current state
- **Used in design**
  - ***Excitation table*** - defines the flip-flop input variable values as function of the current state and next state

# D Flip-Flop Descriptors

---

- **Characteristic Table**

<i>D</i>	<i>Q(t+1)</i>	<i>Operation</i>
<i>0</i>	<i>0</i>	<i>Reset</i>
<i>1</i>	<i>1</i>	<i>Set</i>

- **Characteristic Equation**

$$Q(t+1) = D$$

- **Excitation Table**

<i>Q(t+1)</i>	<i>D</i>	<i>Operation</i>
<i>0</i>	<i>0</i>	<i>Reset</i>
<i>1</i>	<i>1</i>	<i>Set</i>

# T Flip-Flop Descriptors

---

- **Characteristic Table**

<i>T</i>	<i>Q(t+1)</i>	<i>Operation</i>
<i>0</i>	<i>Q(t)</i>	<i>No change</i>
<i>1</i>	$\overline{Q(t)}$	<i>Complement</i>

- **Characteristic Equation**

$$Q(t+1) = T \oplus Q$$

- **Excitation Table**

<i>Q(t+1)</i>	<i>T</i>	<i>Operation</i>
<i>Q(t)</i>	<i>0</i>	<i>No change</i>
$\overline{Q(t)}$	<i>1</i>	<i>Complement</i>

# S-R Flip-Flop Descriptors

- Characteristic Table

<i>S</i>	<i>R</i>	<i>Q(t+1)</i>	<i>Operation</i>
<i>0</i>	<i>0</i>	<i>Q(t)</i>	<i>No change</i>
<i>0</i>	<i>1</i>	<i>0</i>	<i>Reset</i>
<i>1</i>	<i>0</i>	<i>1</i>	<i>Set</i>
<i>1</i>	<i>1</i>	<i>?</i>	<i>Undefined</i>

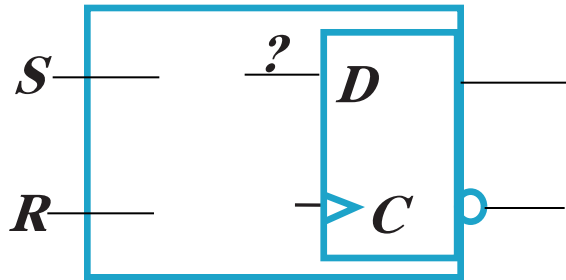
- Characteristic Equation

$$Q(t+1) = S + \bar{R} Q, S \cdot R = 0$$

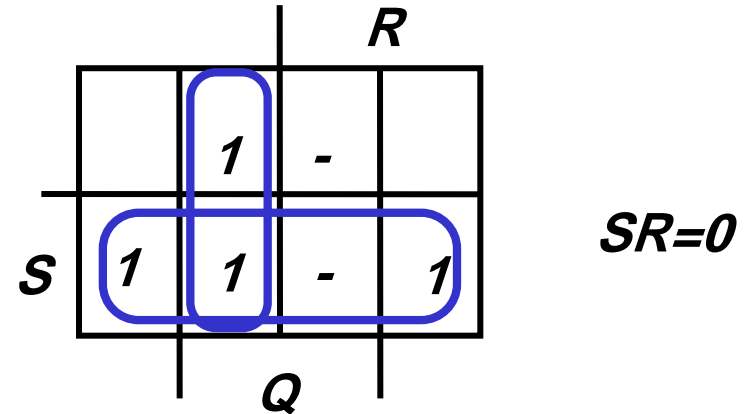
- Excitation Table

<i>Q(t)</i>	<i>Q(t+1)</i>	<i>S</i>	<i>R</i>	<i>Operation</i>
<i>0</i>	<i>0</i>	<i>0</i>	<i>X</i>	<i>No change</i>
<i>0</i>	<i>1</i>	<i>1</i>	<i>0</i>	<i>Set</i>
<i>1</i>	<i>0</i>	<i>0</i>	<i>1</i>	<i>Reset</i>
<i>1</i>	<i>1</i>	<i>X</i>	<i>0</i>	<i>No change</i>

# S-R Flip-flop



S	R	Q	Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X



$$D = S + R'Q, \quad SR = 0$$

# J-K Flip-Flop Descriptors

- Characteristic Table

<i>J</i>	<i>K</i>	<i>Q(t+1)</i>	<i>Operation</i>
<i>0</i>	<i>0</i>	<i>Q(t)</i>	<i>No change</i>
<i>0</i>	<i>1</i>	<i>0</i>	<i>Reset</i>
<i>1</i>	<i>0</i>	<i>1</i>	<i>Set</i>
<i>1</i>	<i>1</i>	$\overline{Q(t)}$	<i>Complement</i>

- Characteristic Equation

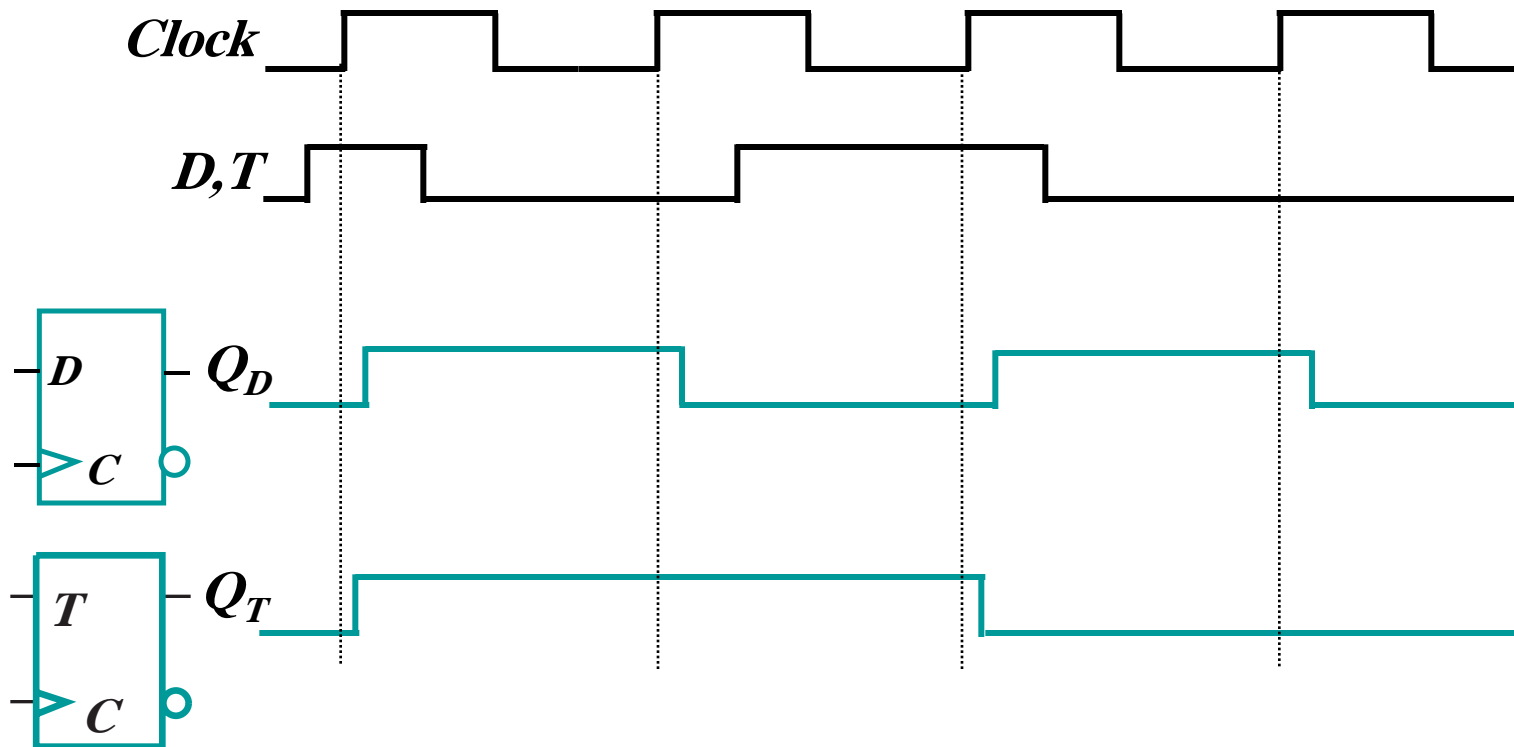
$$Q(t+1) = J \overline{Q} + \overline{K} Q$$

- Excitation Table

<i>Q(t)</i>	<i>Q(t+1)</i>	<i>J</i>	<i>K</i>	<i>Operation</i>
<i>0</i>	<i>0</i>	<i>0</i>	<i>X</i>	<i>No change</i>
<i>0</i>	<i>1</i>	<i>1</i>	<i>X</i>	<i>Set</i>
<i>1</i>	<i>0</i>	<i>X</i>	<i>1</i>	<i>Reset</i>
<i>1</i>	<i>1</i>	<i>X</i>	<i>0</i>	<i>No Change</i>

# Example 1: Flip-flop Behavior

- Use the characteristic tables to find the output waveforms for the flip-flops shown:





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