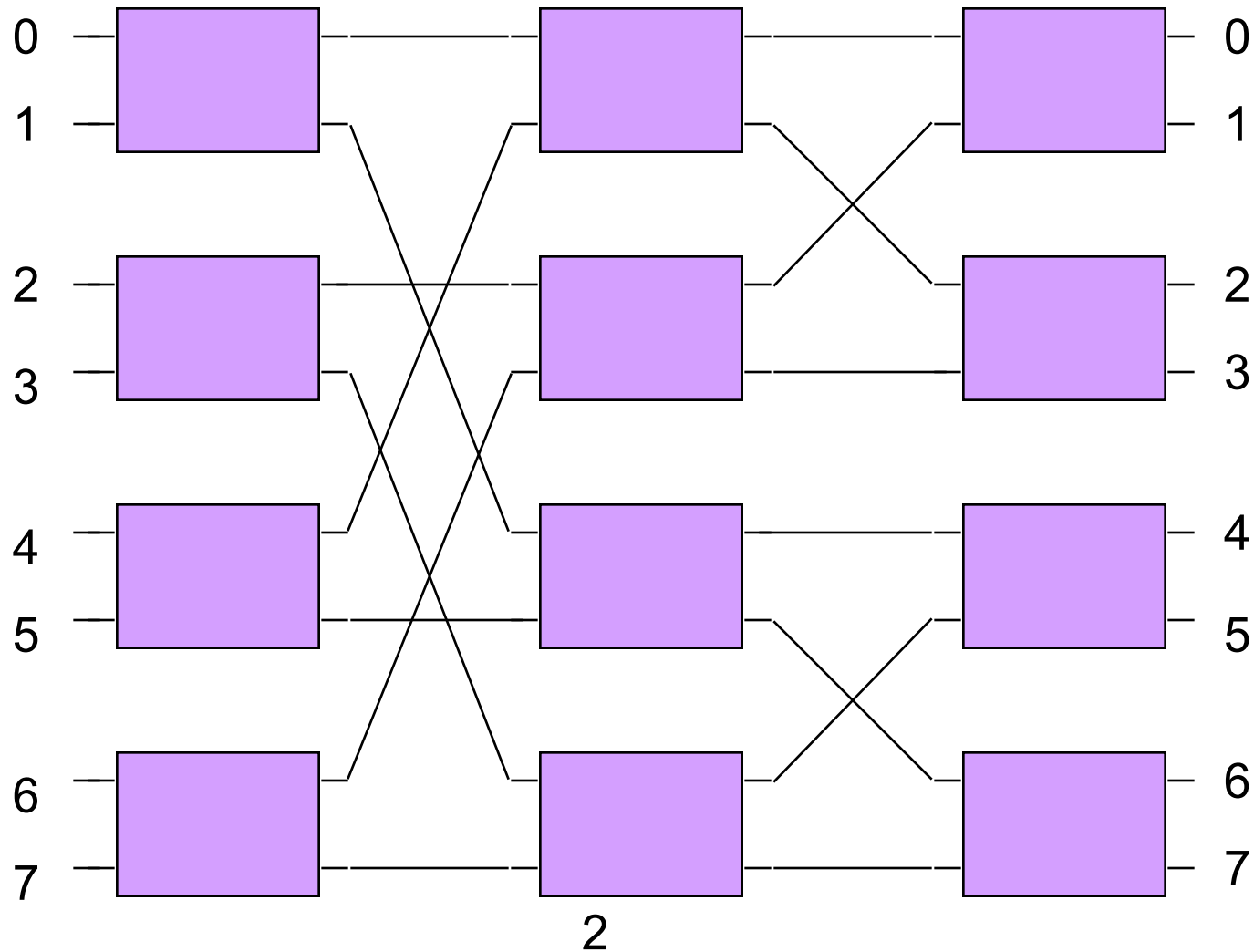


# Delta Network

- The delta network is one example of a multistage interconnection network that can be used as a switch fabric
- The delta network is an example of a banyan network
- In banyan networks, there is a single path from each input port to each output port
- A delta network looks like the following...

# 8 x 8 DELTA NETWORK

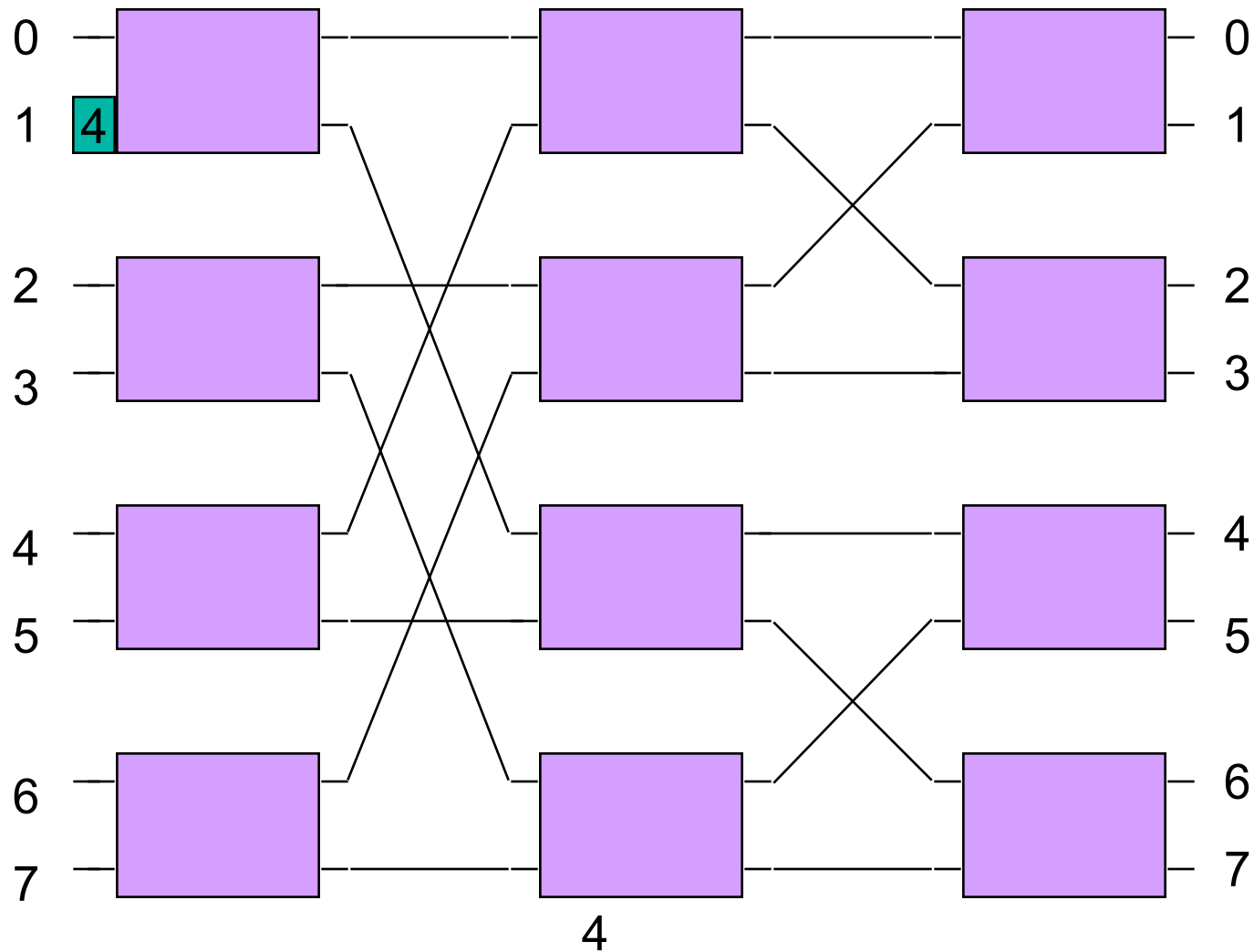


# Self Routing

- Delta network has self-routing property
- The path for a cell to take to reach its destination can be determined directly from its routing tag (i.e., destination port id)
- Stage k of the MIN looks at bit k of the tag
- If bit k is 0, then send cell out upper port
- If bit k is 1, then send cell out lower port
- Works for every possible input port (really!)

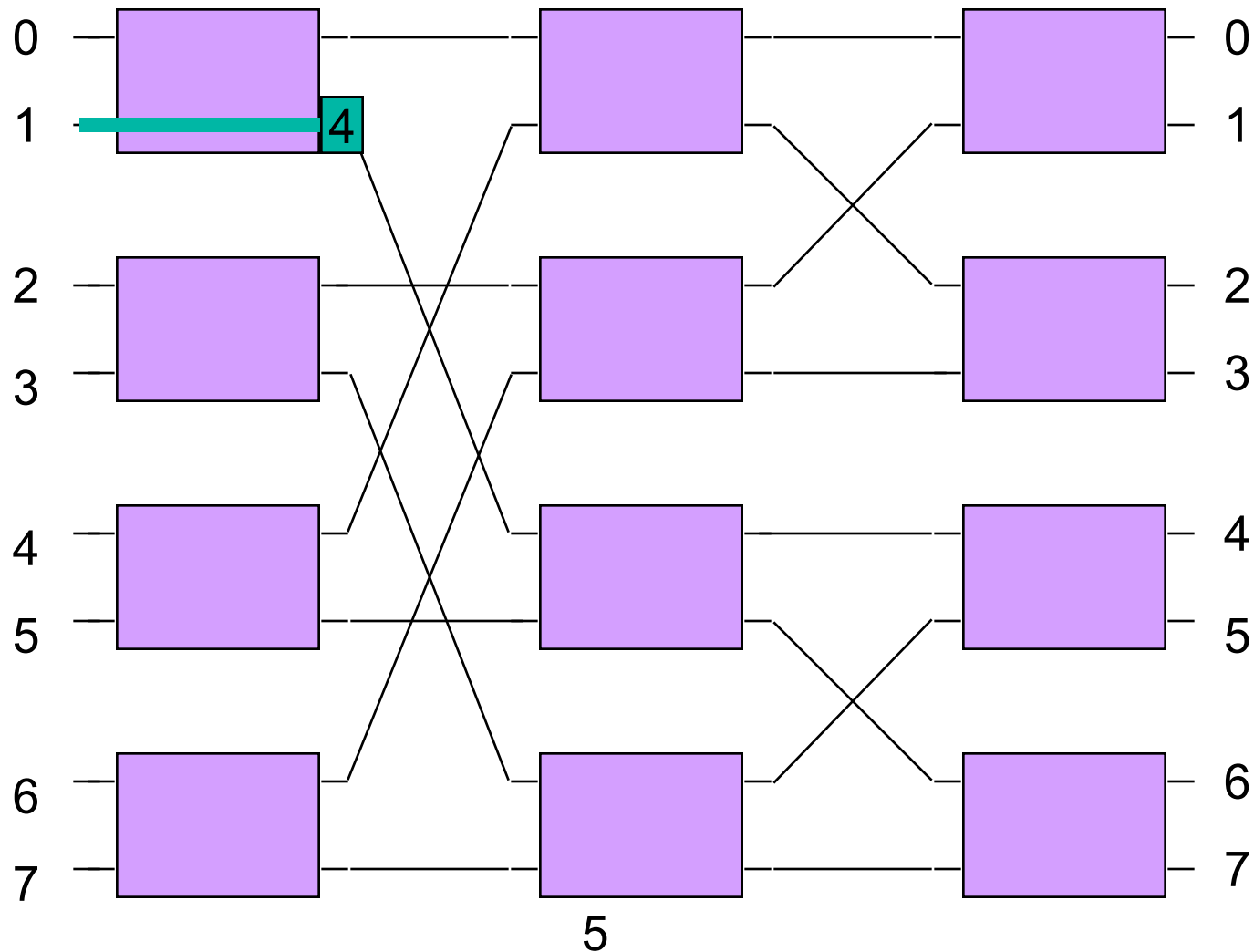
# Example of Self Routing

Cell destined for output port 4 ( $= 100_2$ )



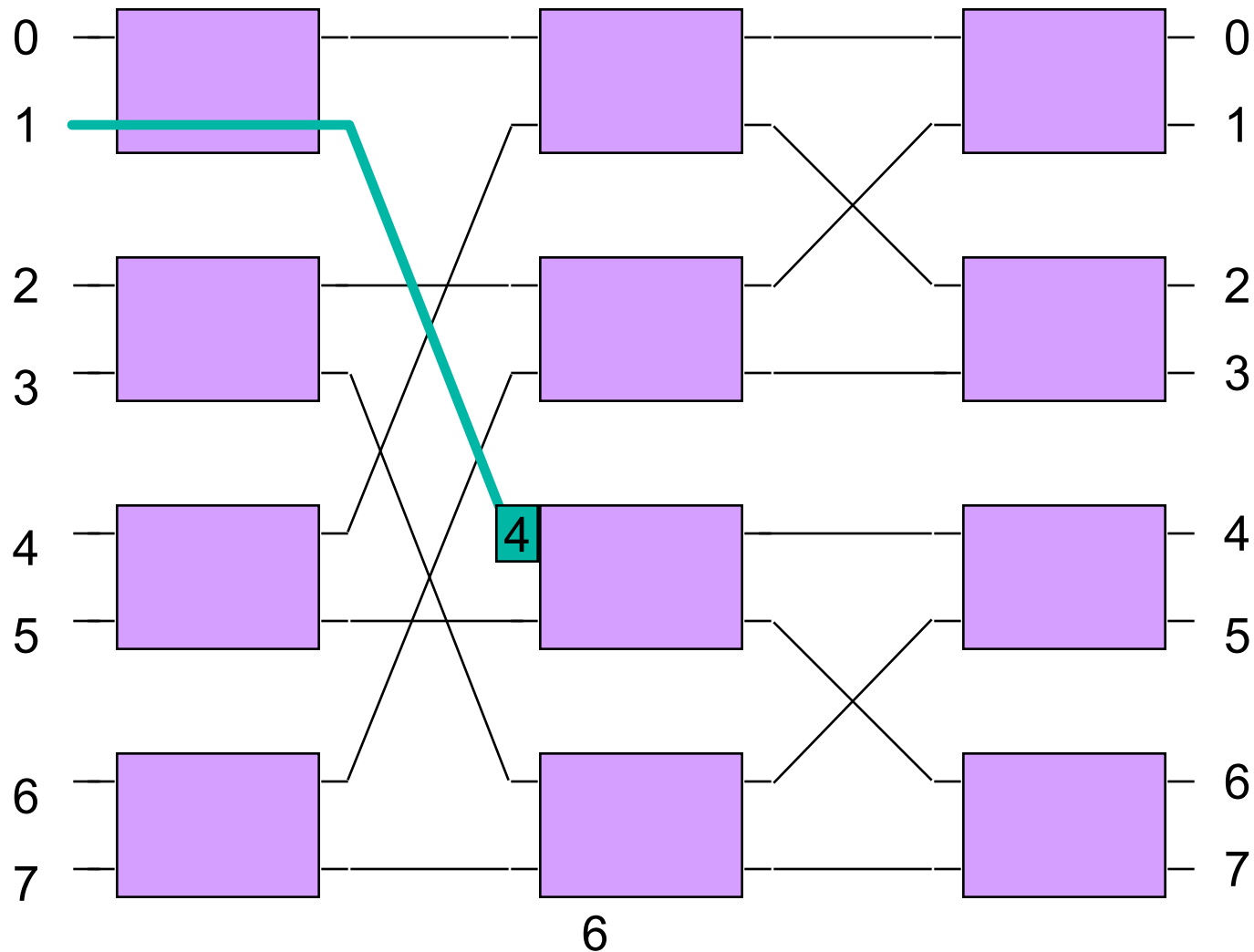
# Example of Self Routing

Cell destined for output port 4 ( $= 100_2$ )



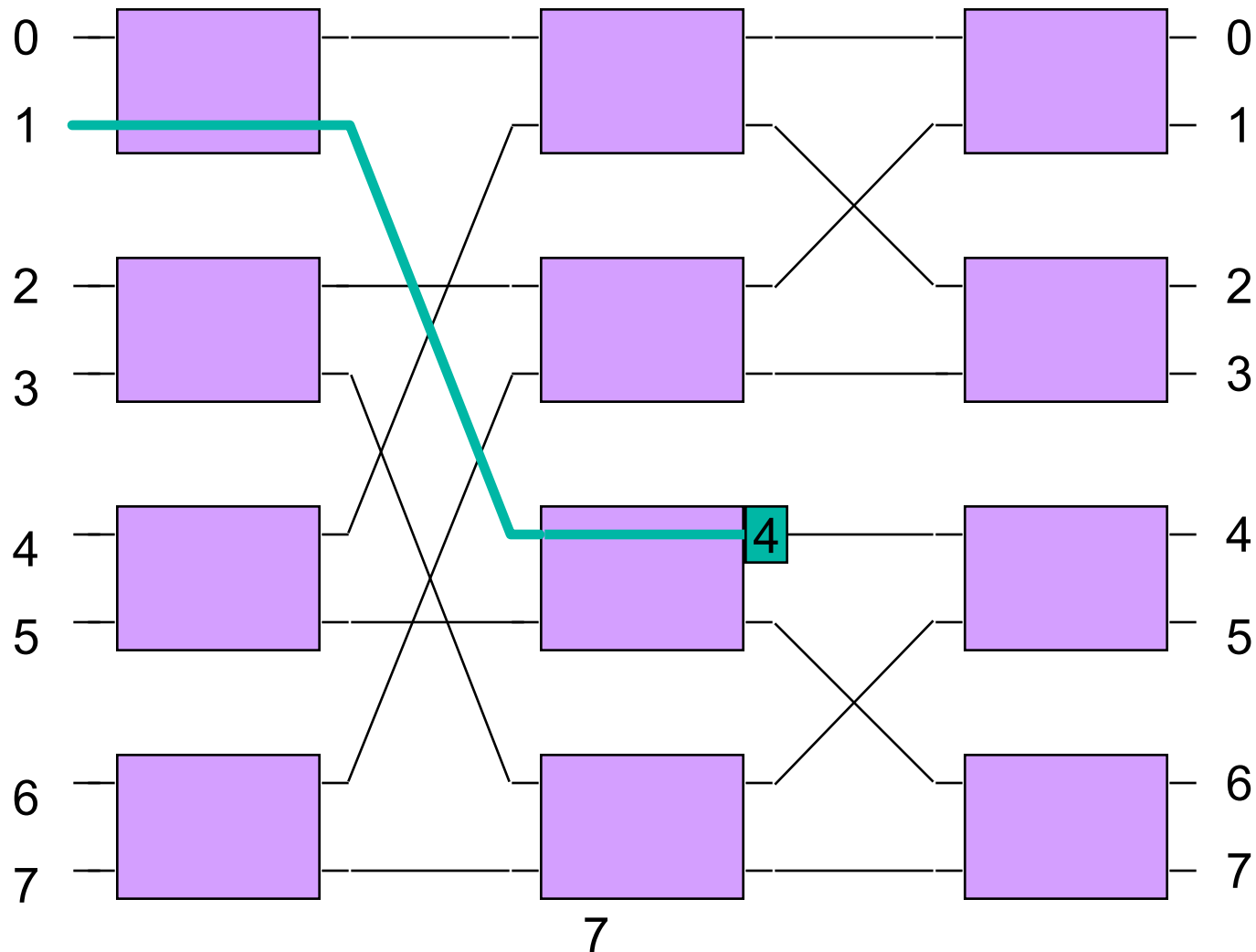
# Example of Self Routing

Cell destined for output port 4 ( $= 100_2$ )



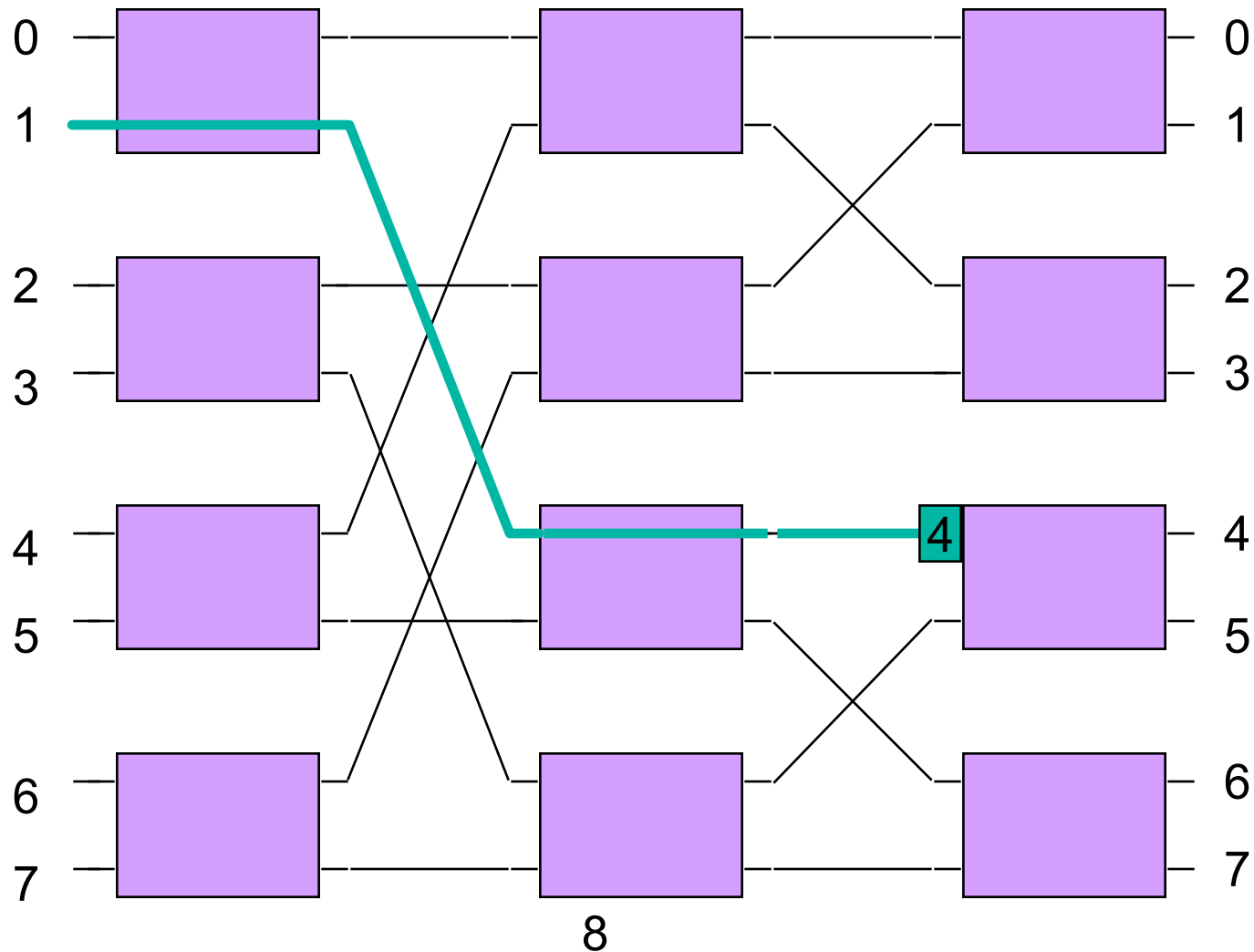
# Example of Self Routing

Cell destined for output port 4 ( $= 100_2$ )



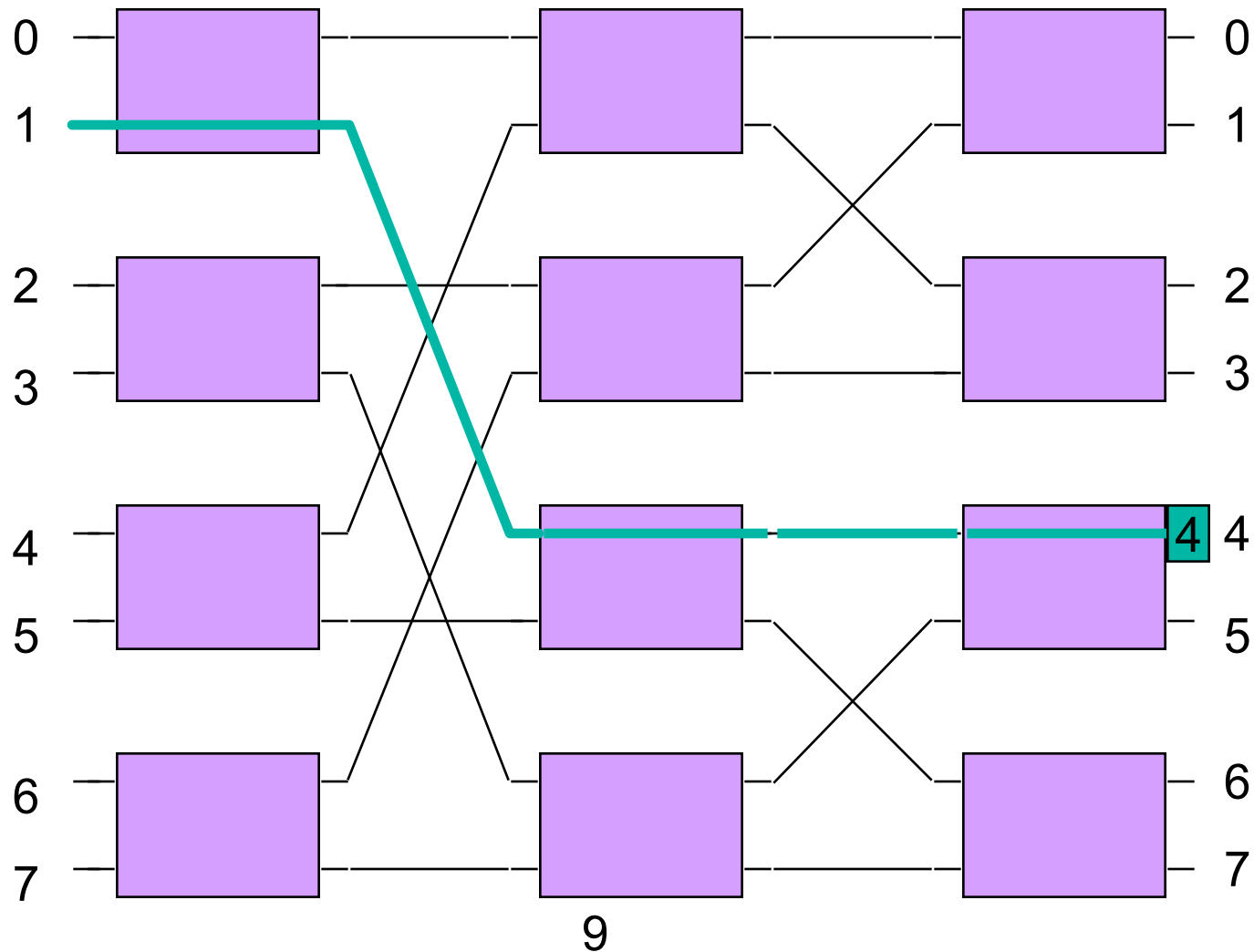
# Example of Self Routing

Cell destined for output port 4 ( $= 100_2$ )



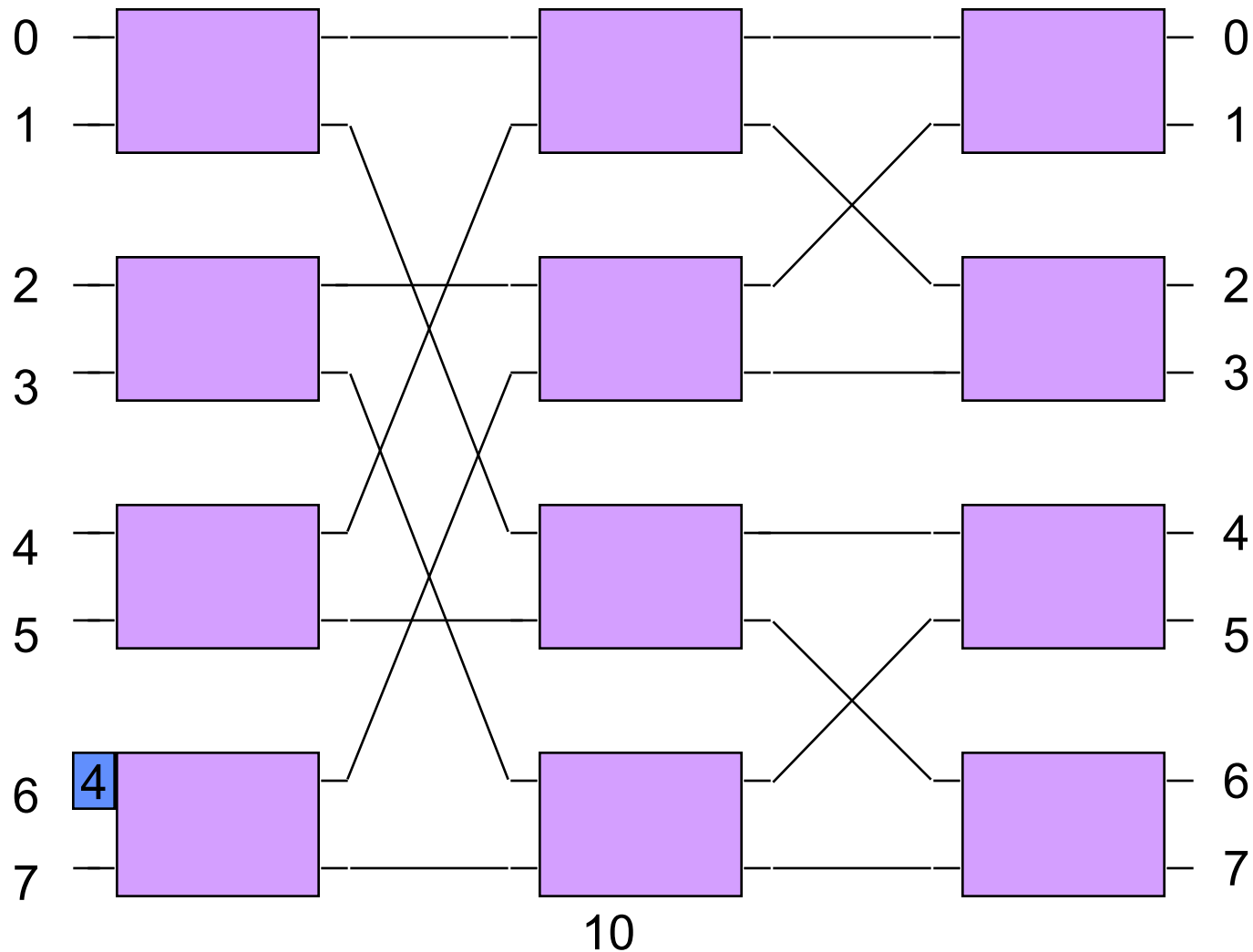
# Example of Self Routing

Cell destined for output port 4 ( $= 100_2$ )



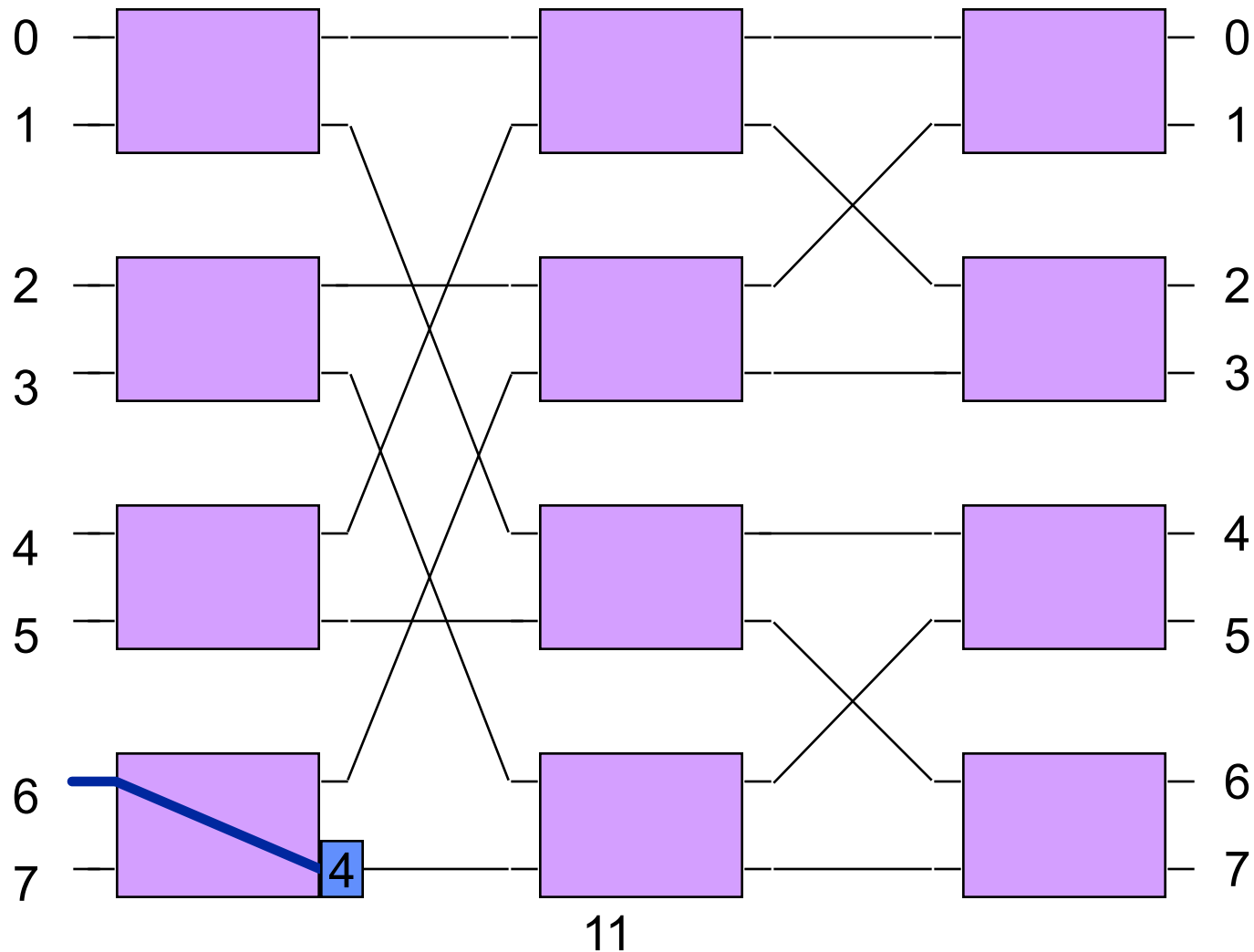
# Example of Self Routing

Cell destined for output port 4 ( $= 100_2$ )



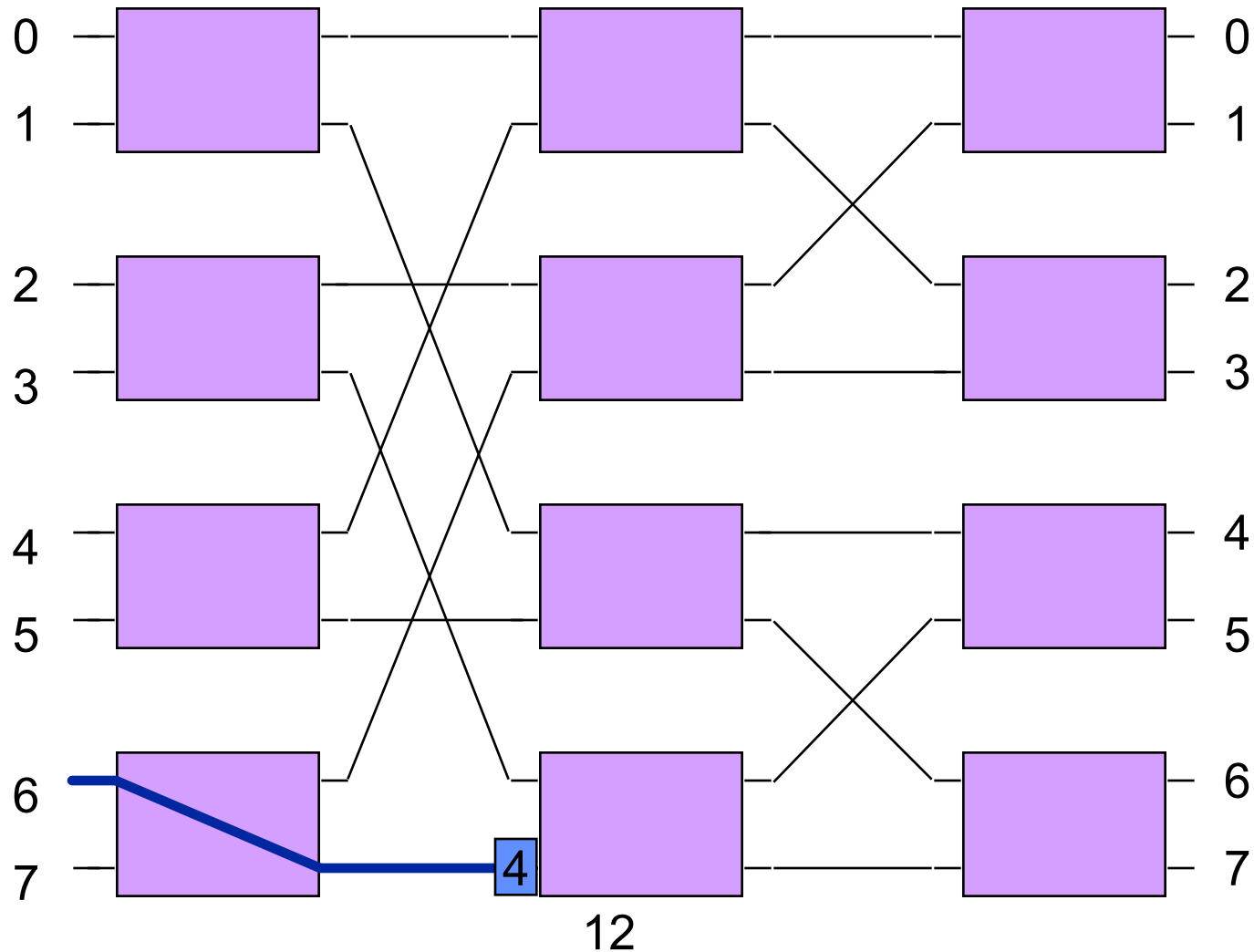
# Example of Self Routing

Cell destined for output port 4 ( $= 100_2$ )



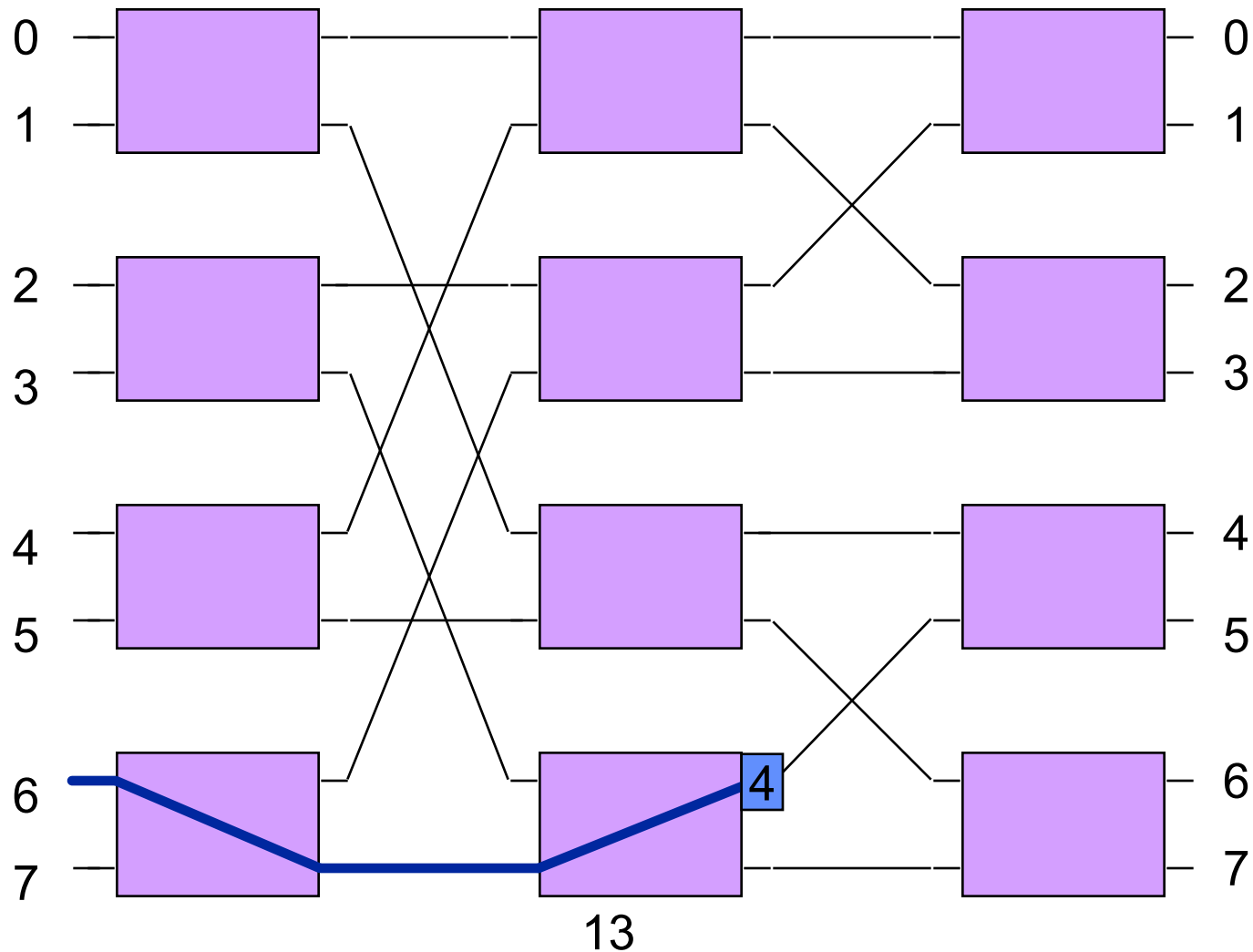
# Example of Self Routing

Cell destined for output port 4 ( $= 100_2$ )



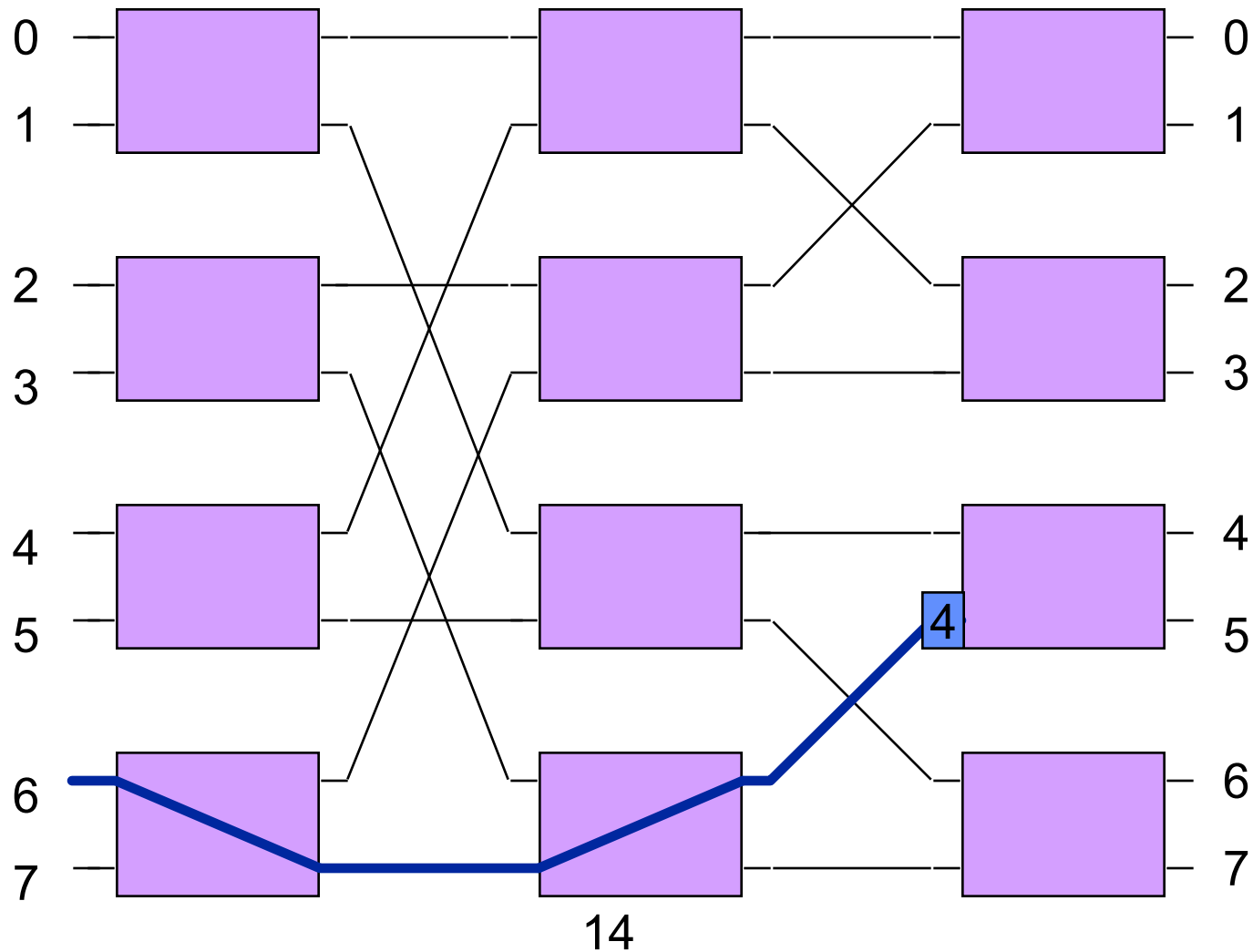
# Example of Self Routing

Cell destined for output port 4 ( $= 100_2$ )



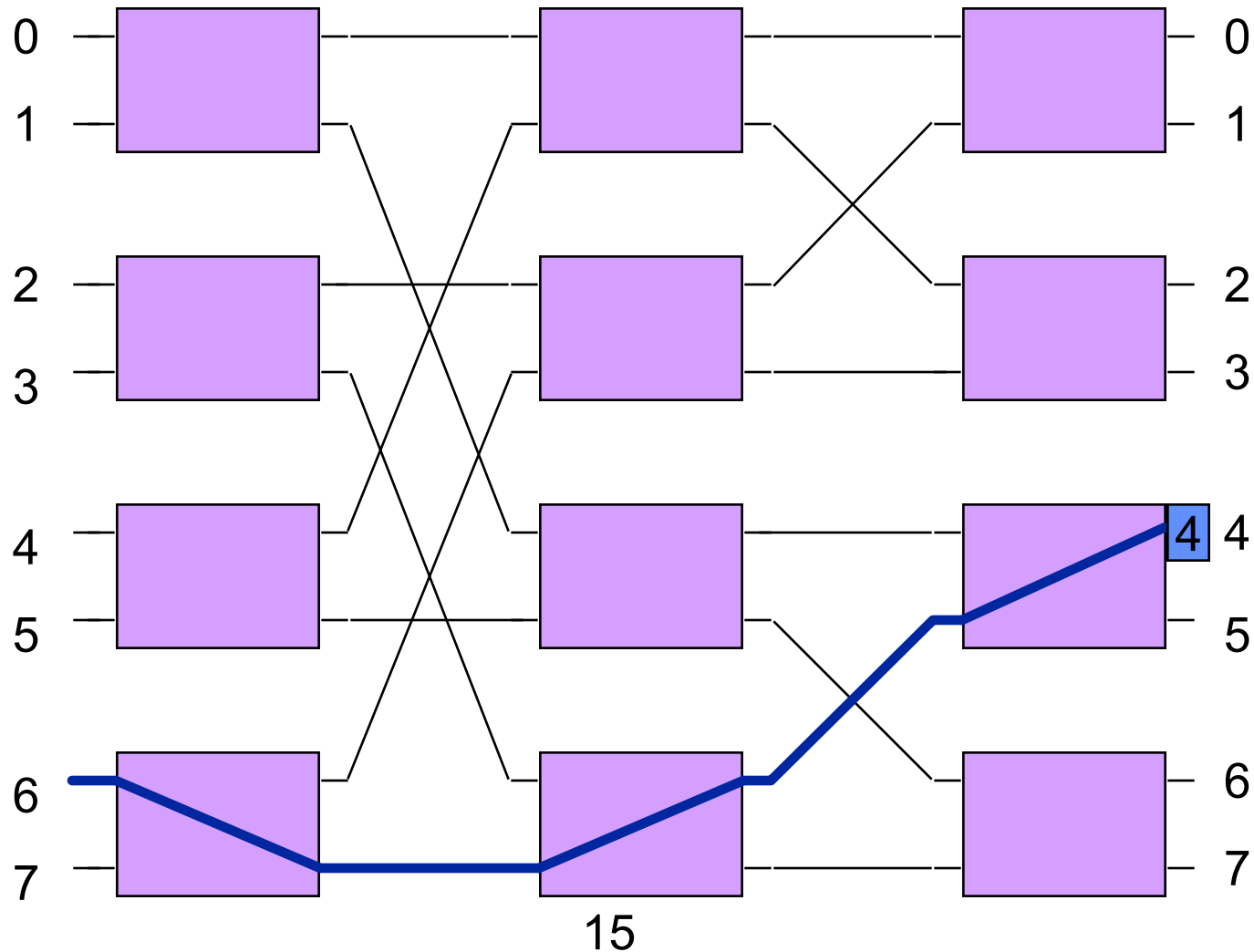
# Example of Self Routing

Cell destined for output port 4 ( $= 100_2$ )

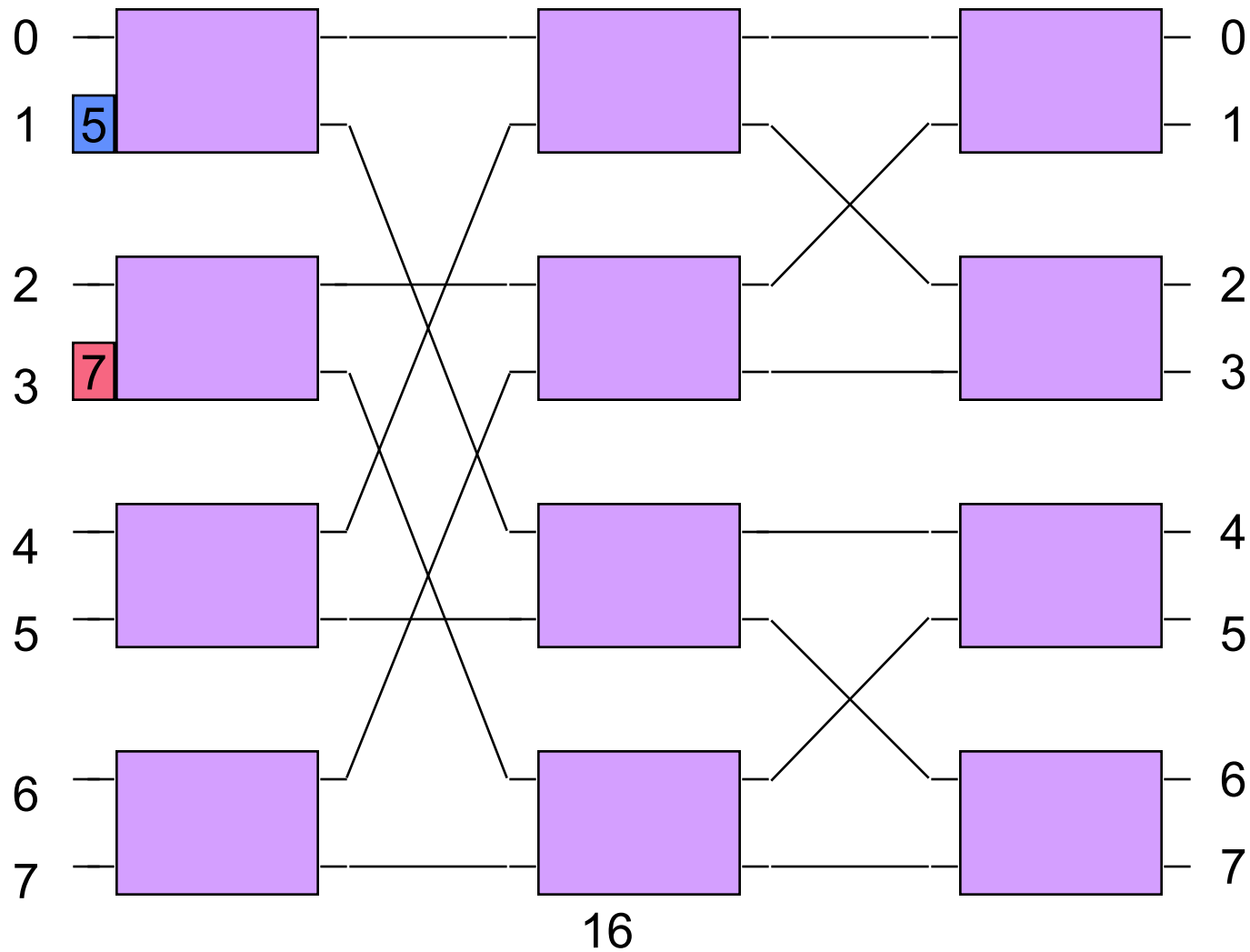


# Example of Self Routing

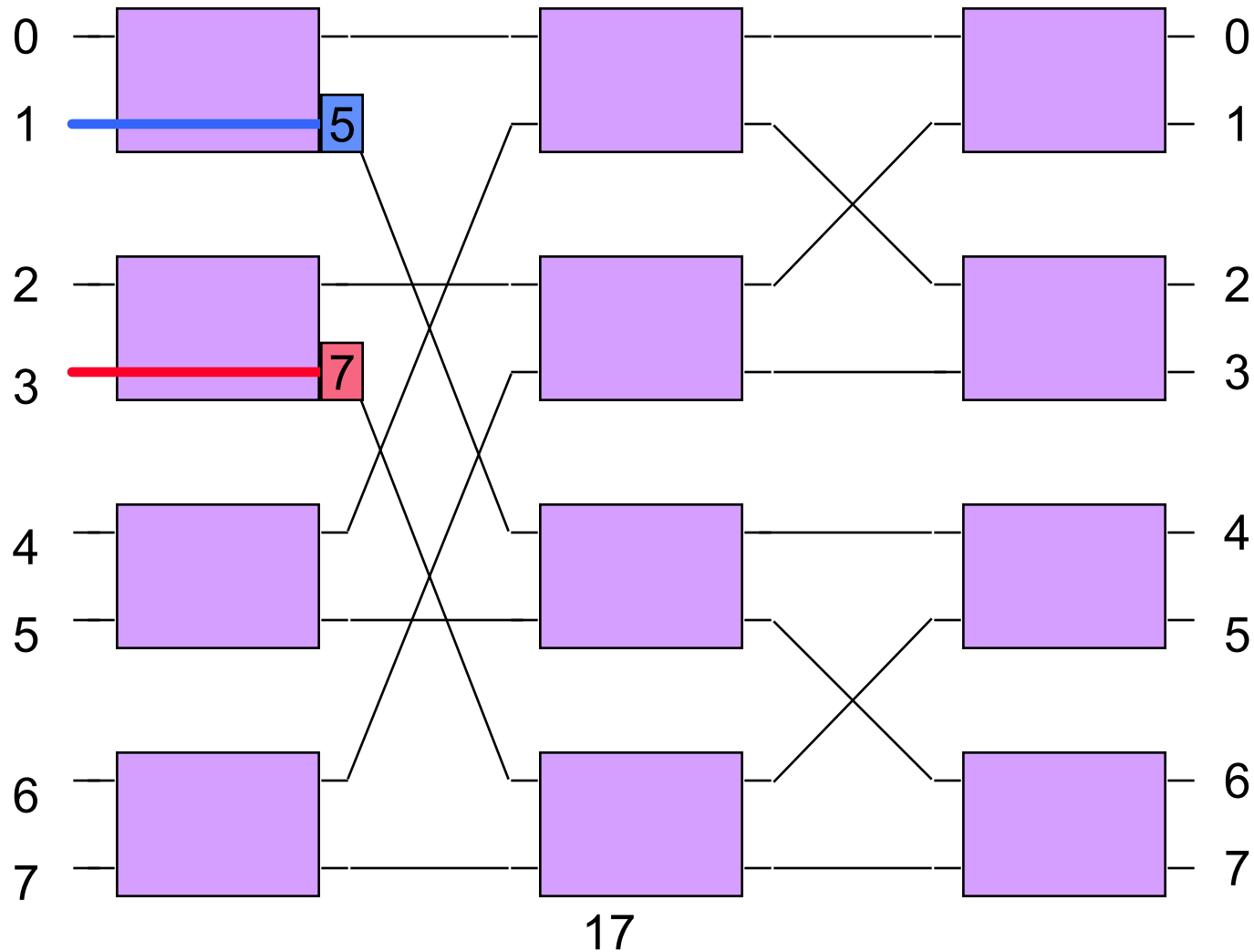
Cell destined for output port 4 ( $= 100_2$ )



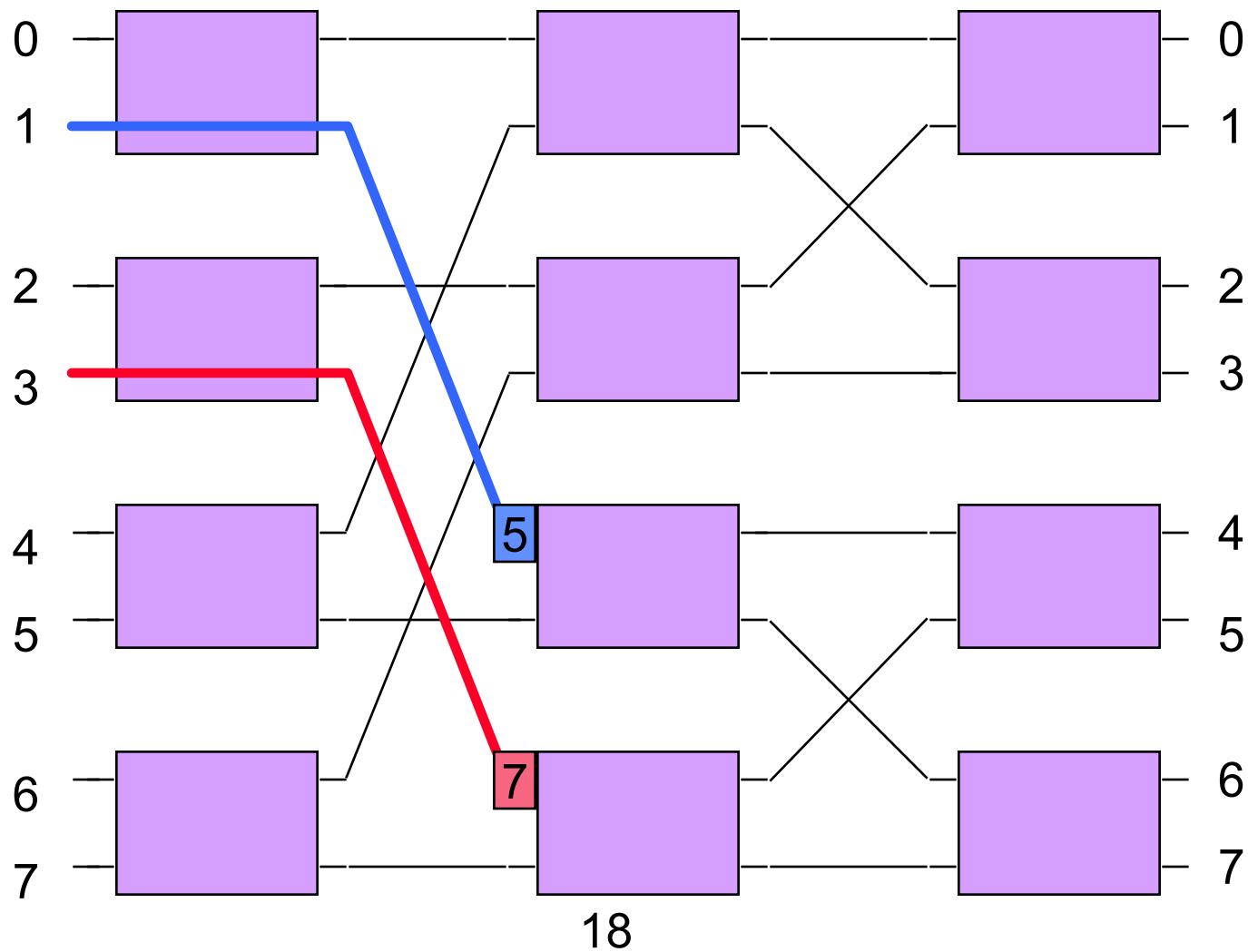
# Multiple Concurrent Paths



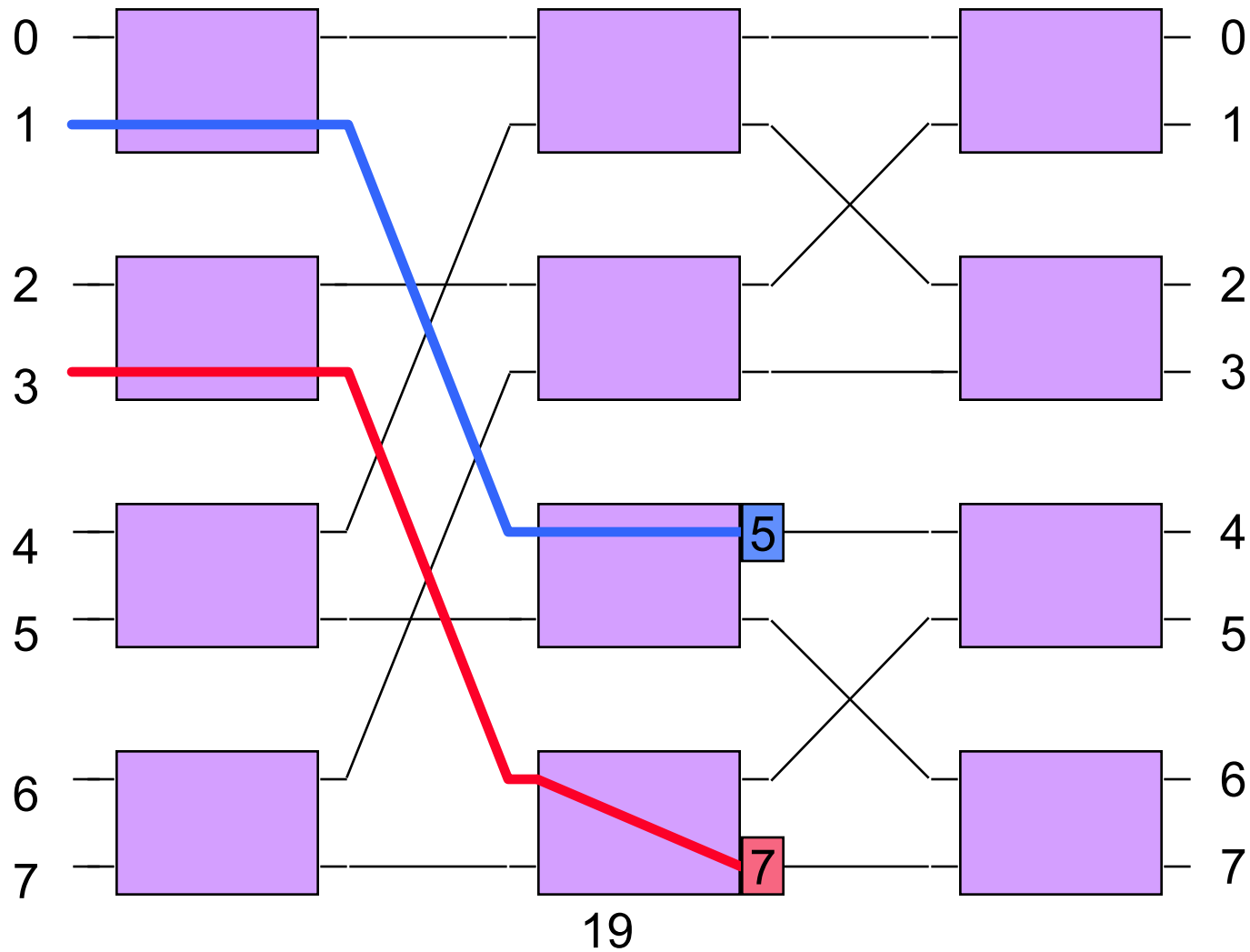
# Multiple Concurrent Paths



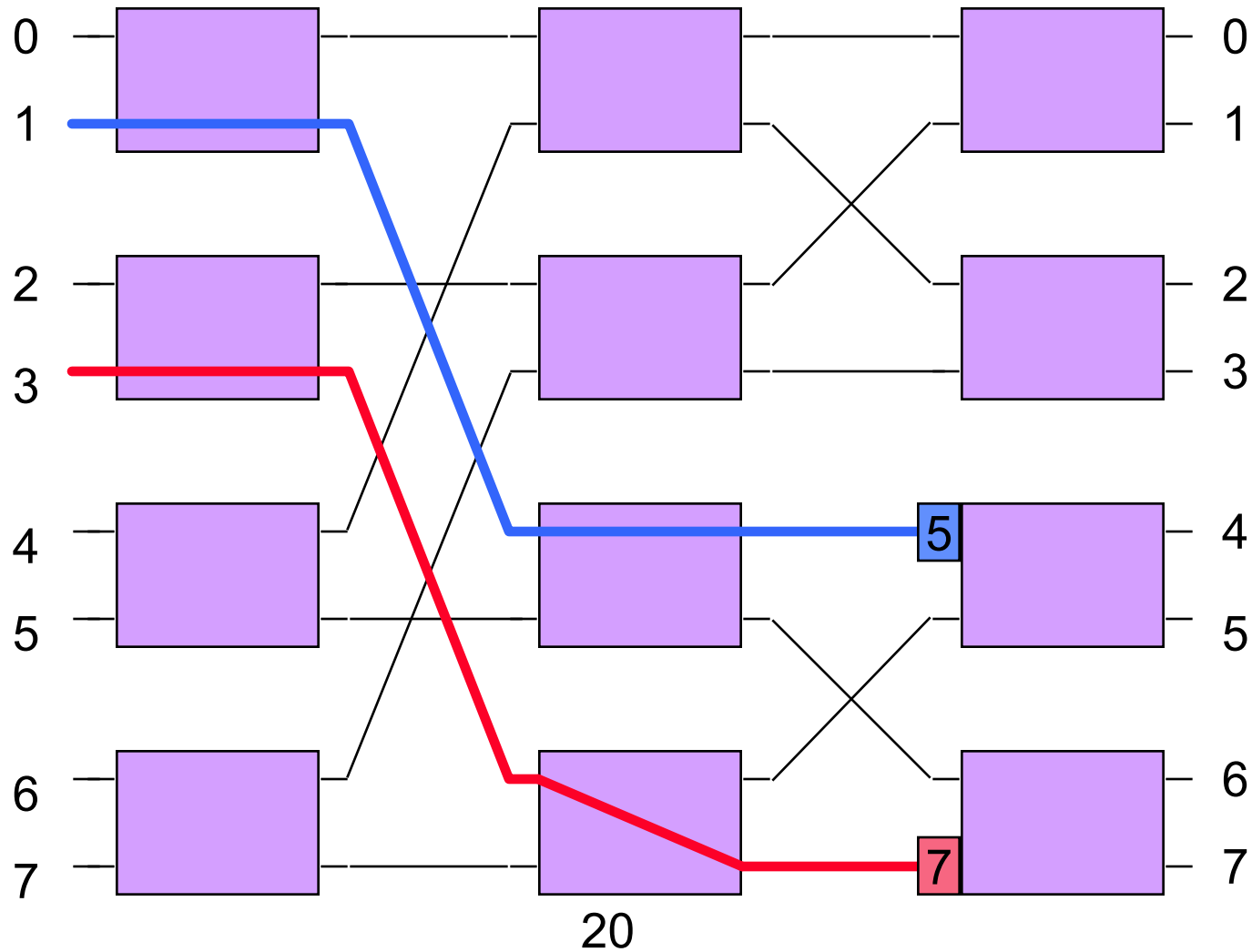
# Multiple Concurrent Paths



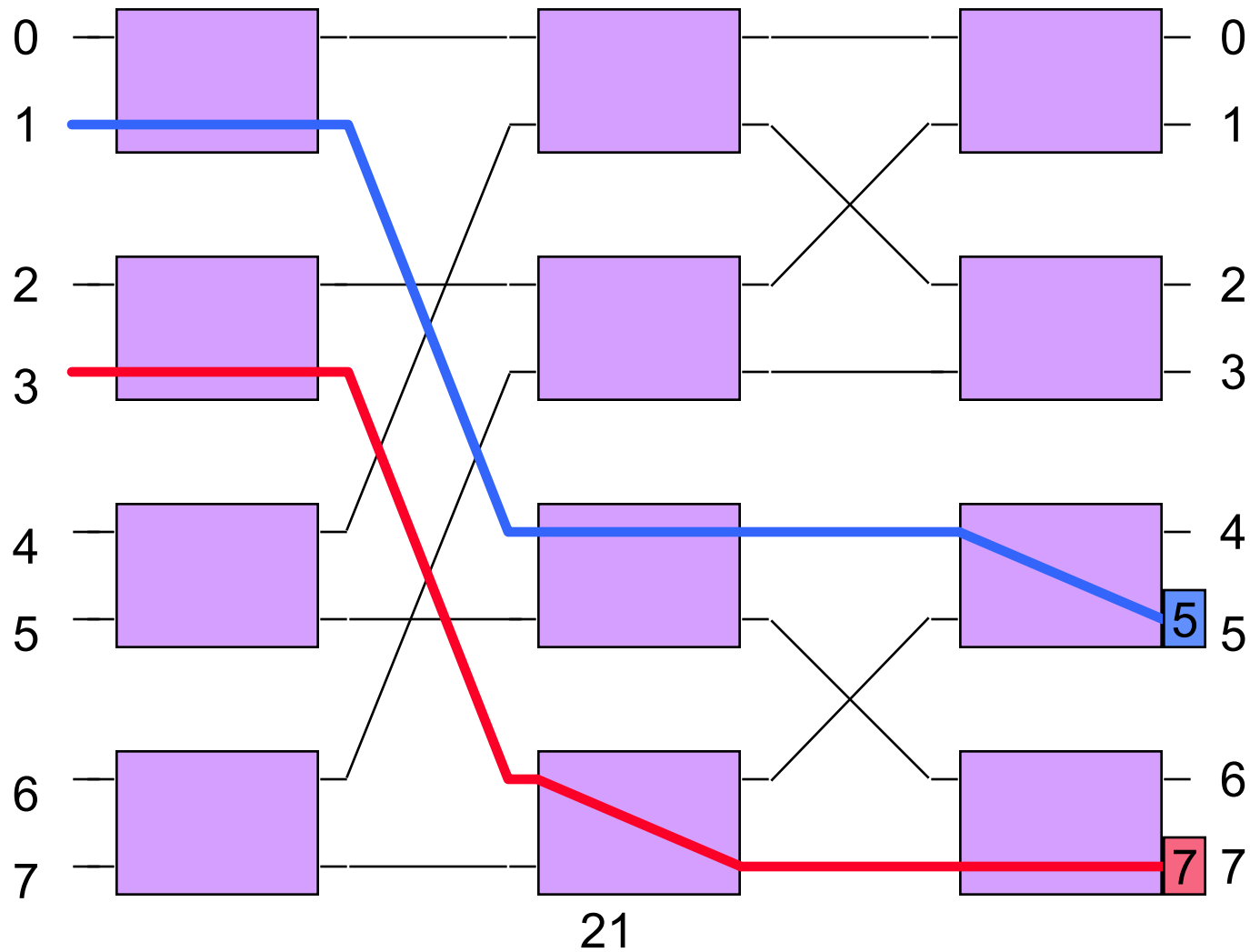
# Multiple Concurrent Paths



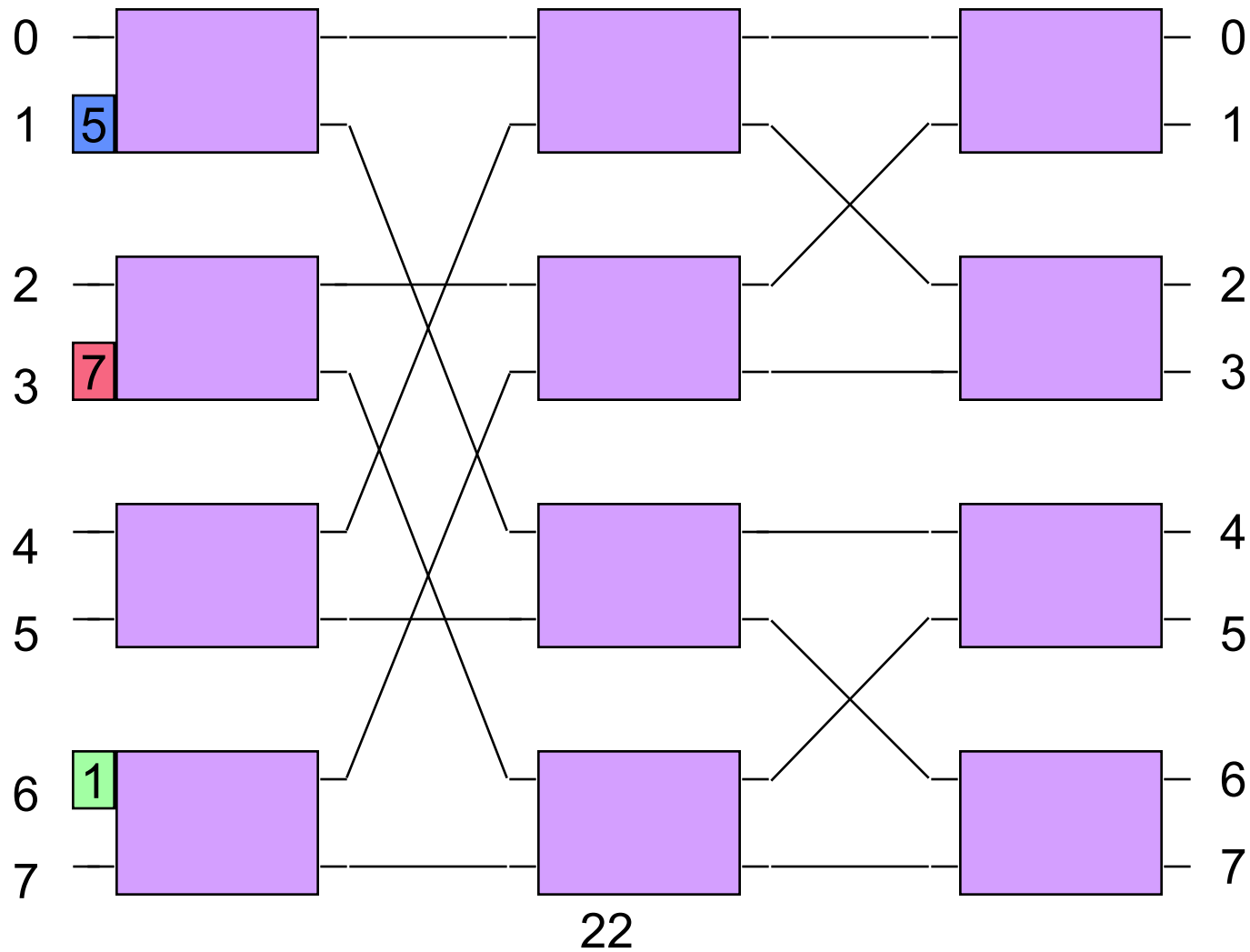
# Multiple Concurrent Paths



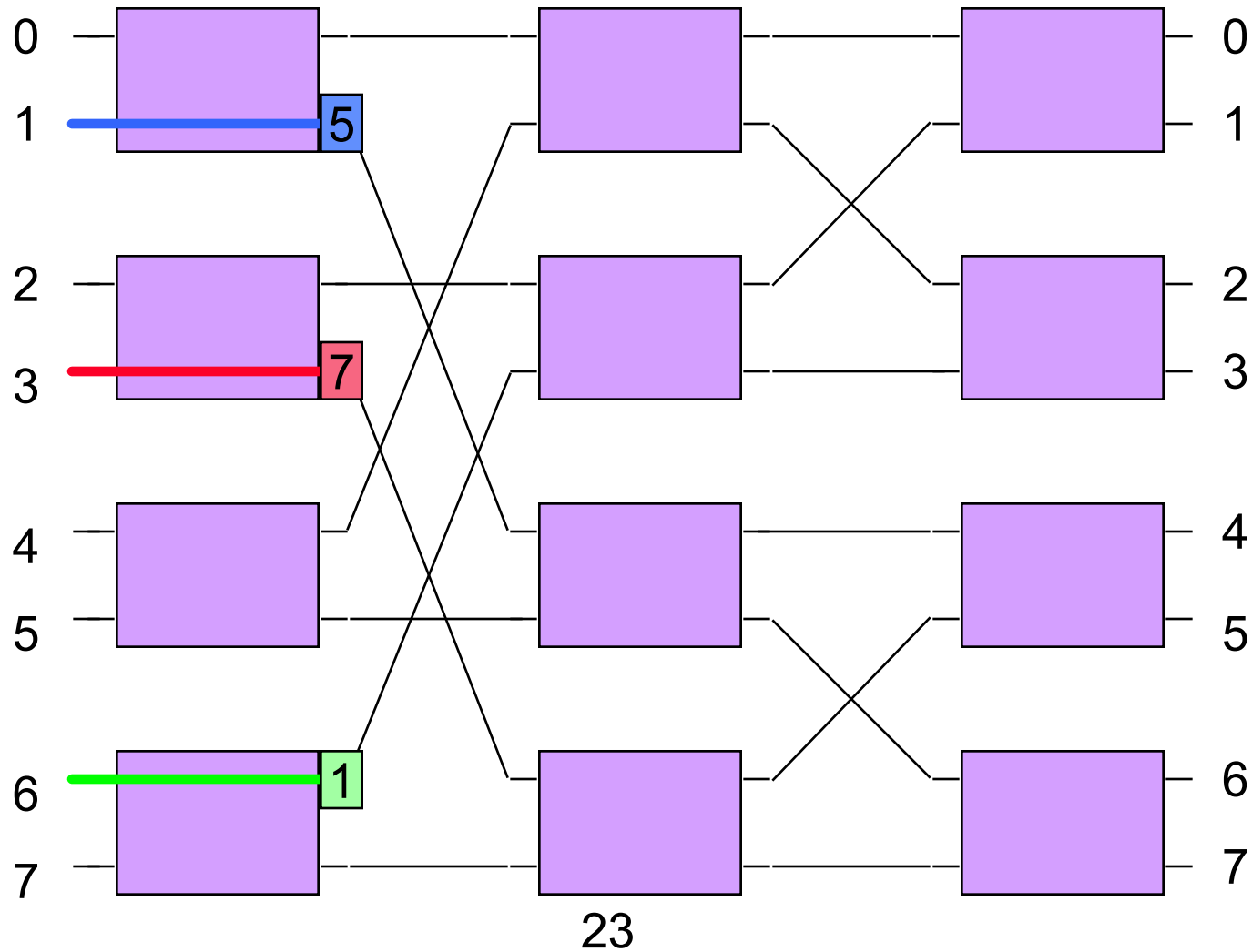
# Multiple Concurrent Paths



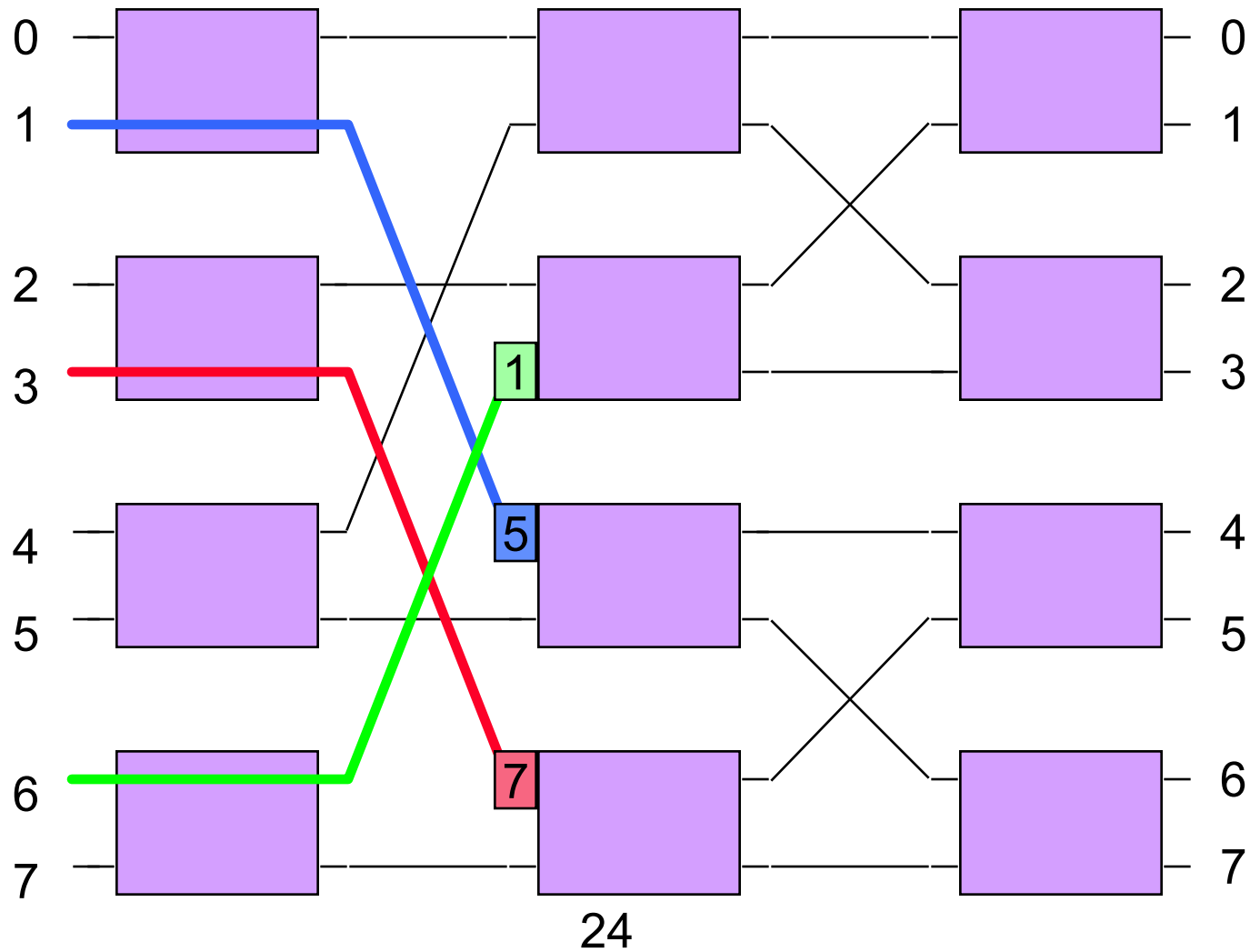
# Multiple Concurrent Paths



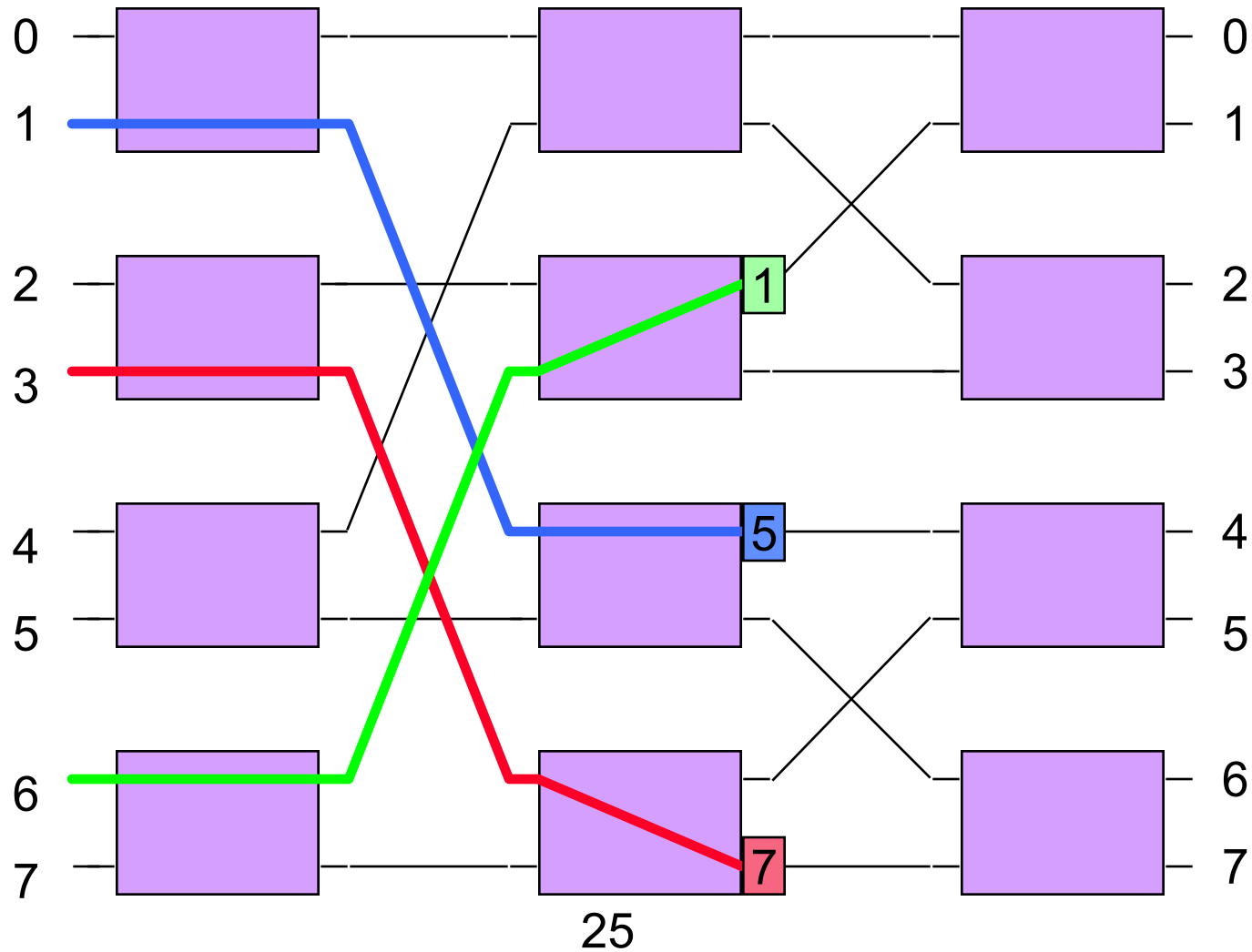
# Multiple Concurrent Paths



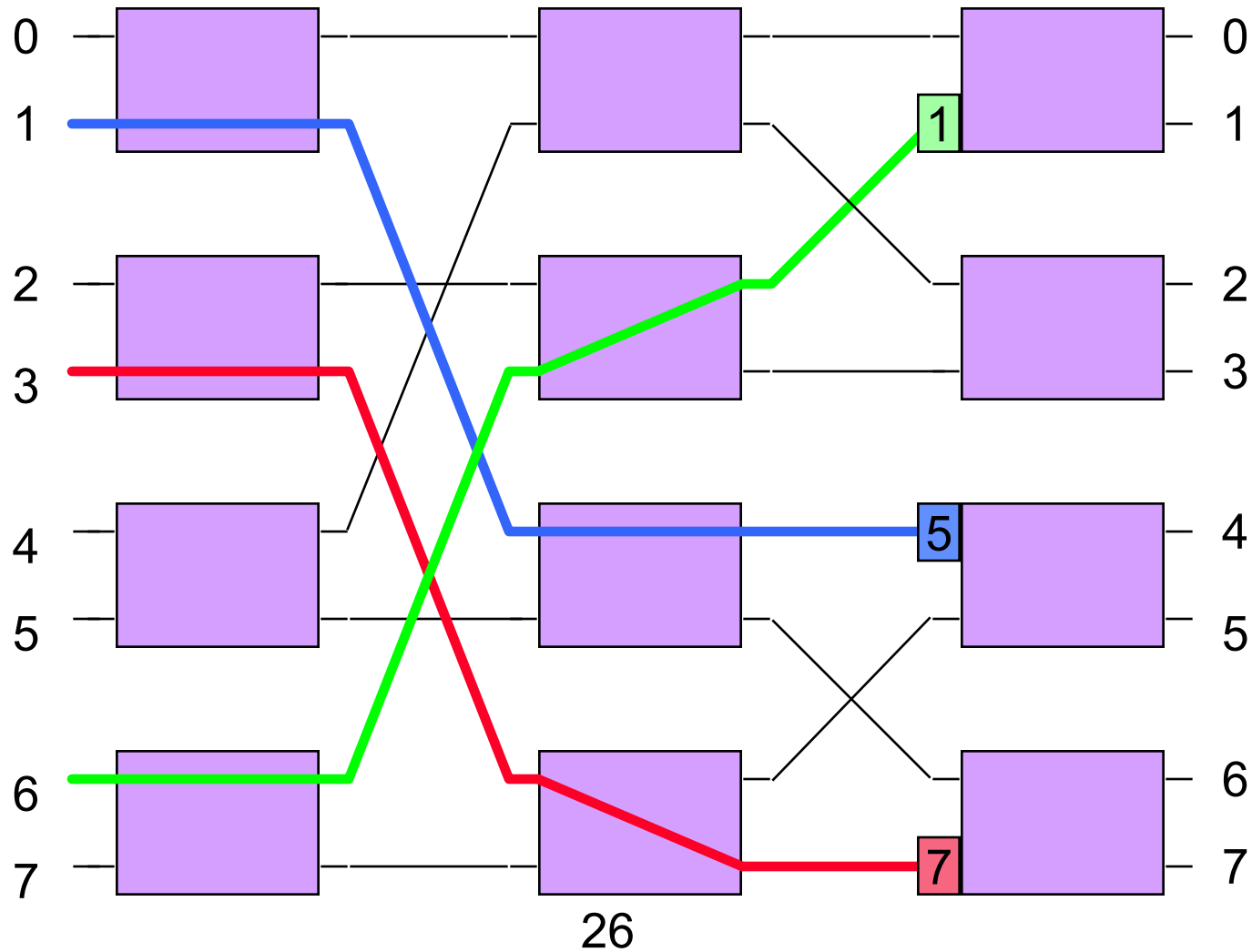
# Multiple Concurrent Paths



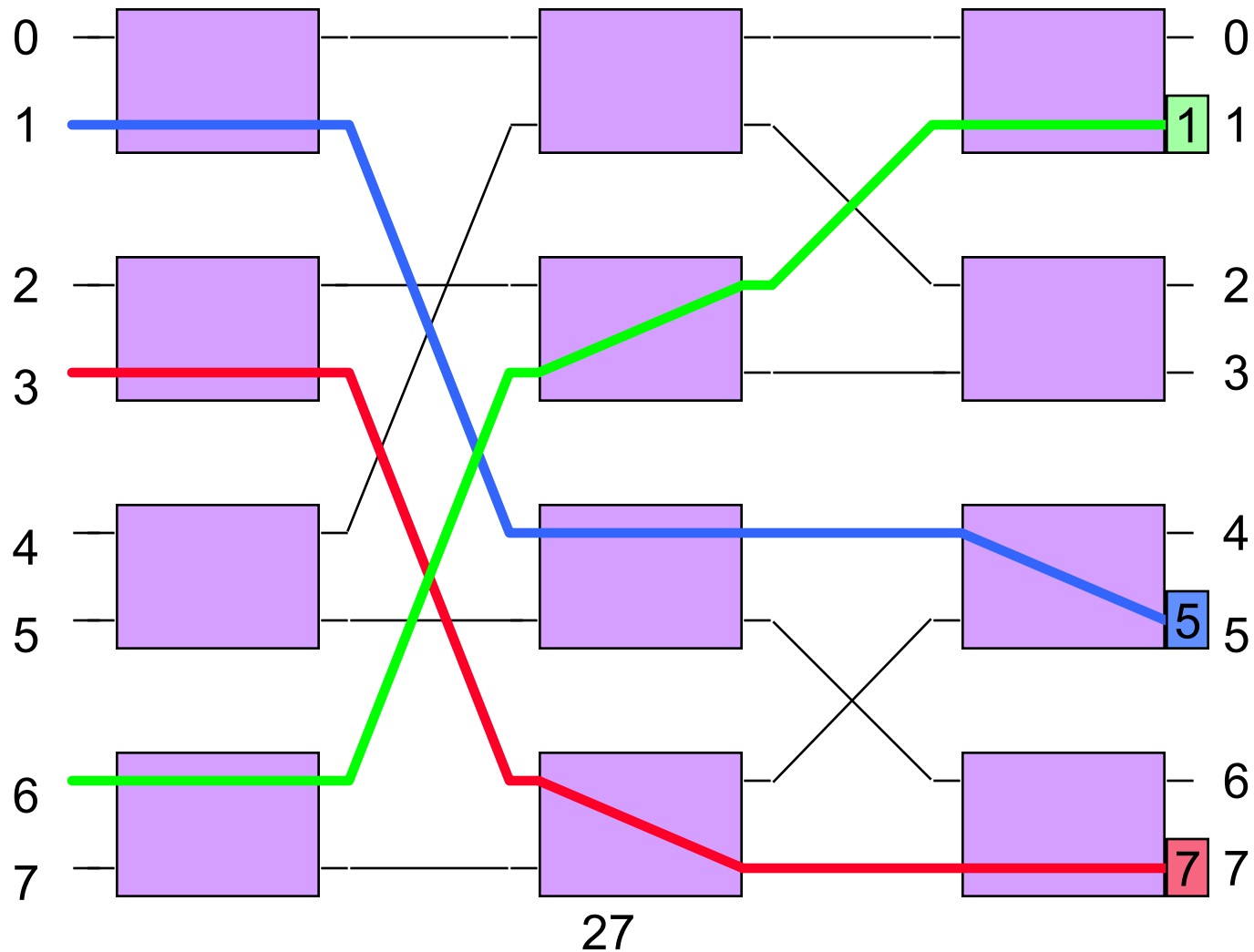
# Multiple Concurrent Paths



# Multiple Concurrent Paths



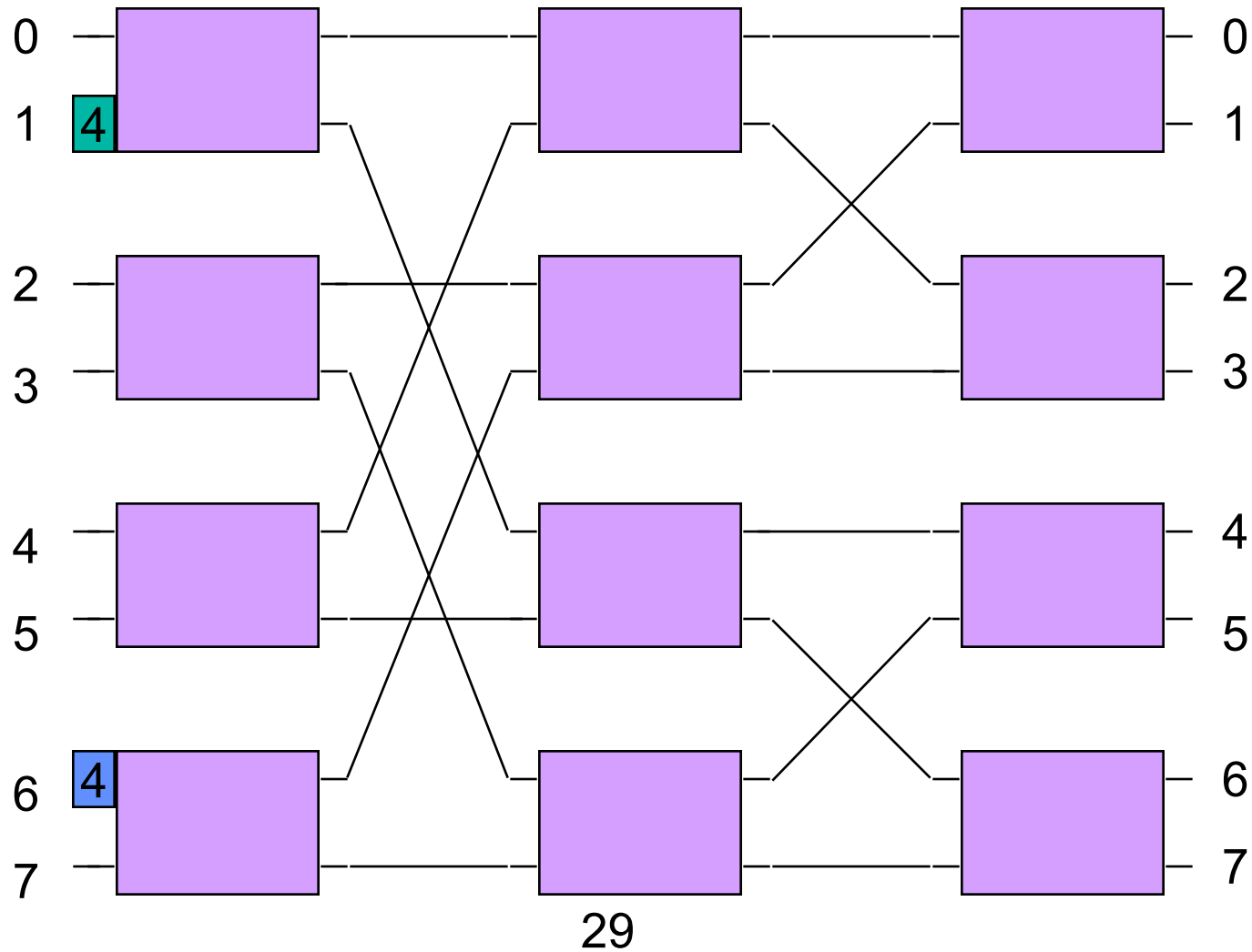
# Multiple Concurrent Paths



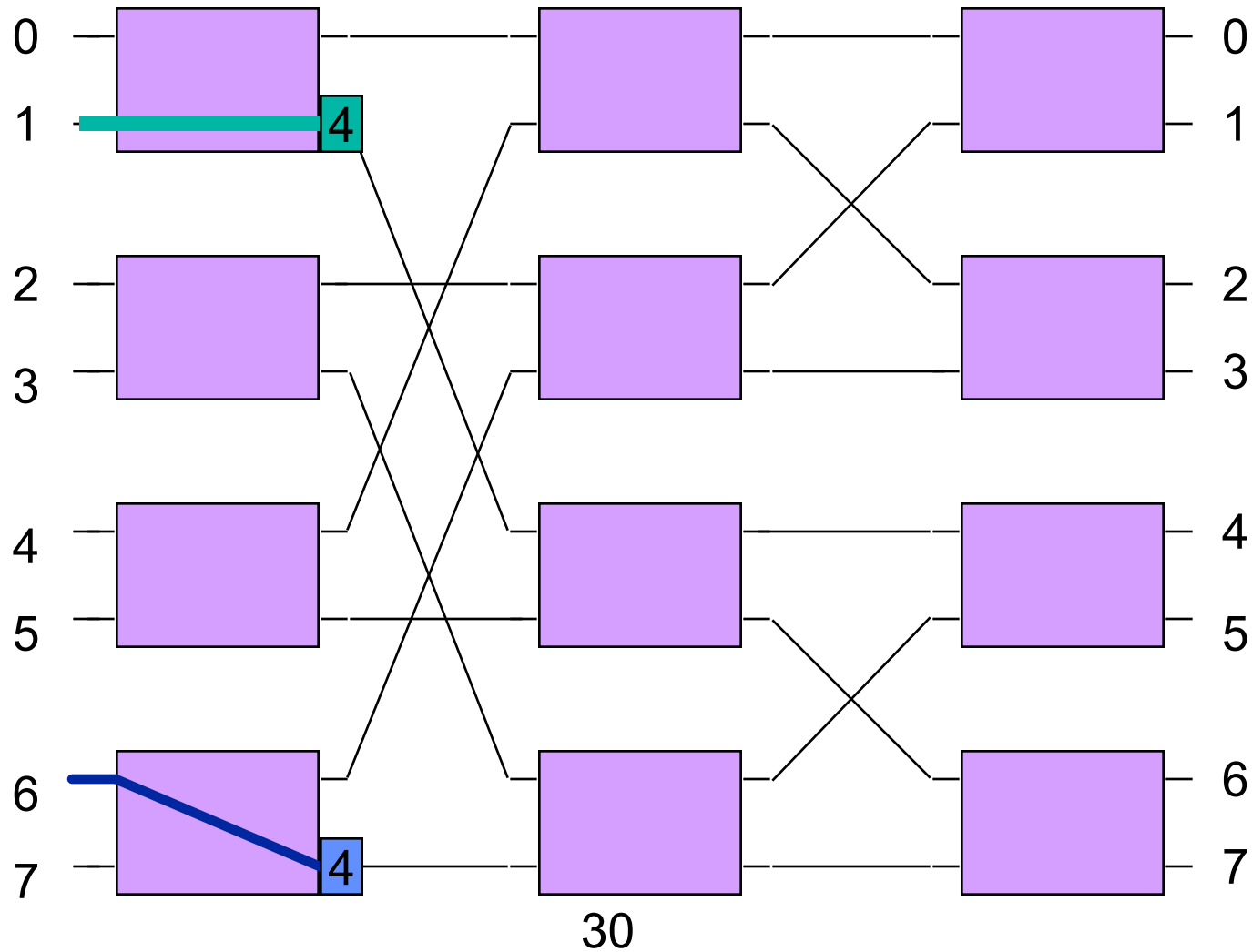
# Output Port Contention

- Up to now, all examples have worked wonderfully because each incoming cell was destined to a different output port
- What happens if more than one cell destined to same output port?
- Answer: output port contention
- Result: cell loss in a bufferless network
- Alternatives: buffering, deflection routing, recirculation, tandem banyans, ...

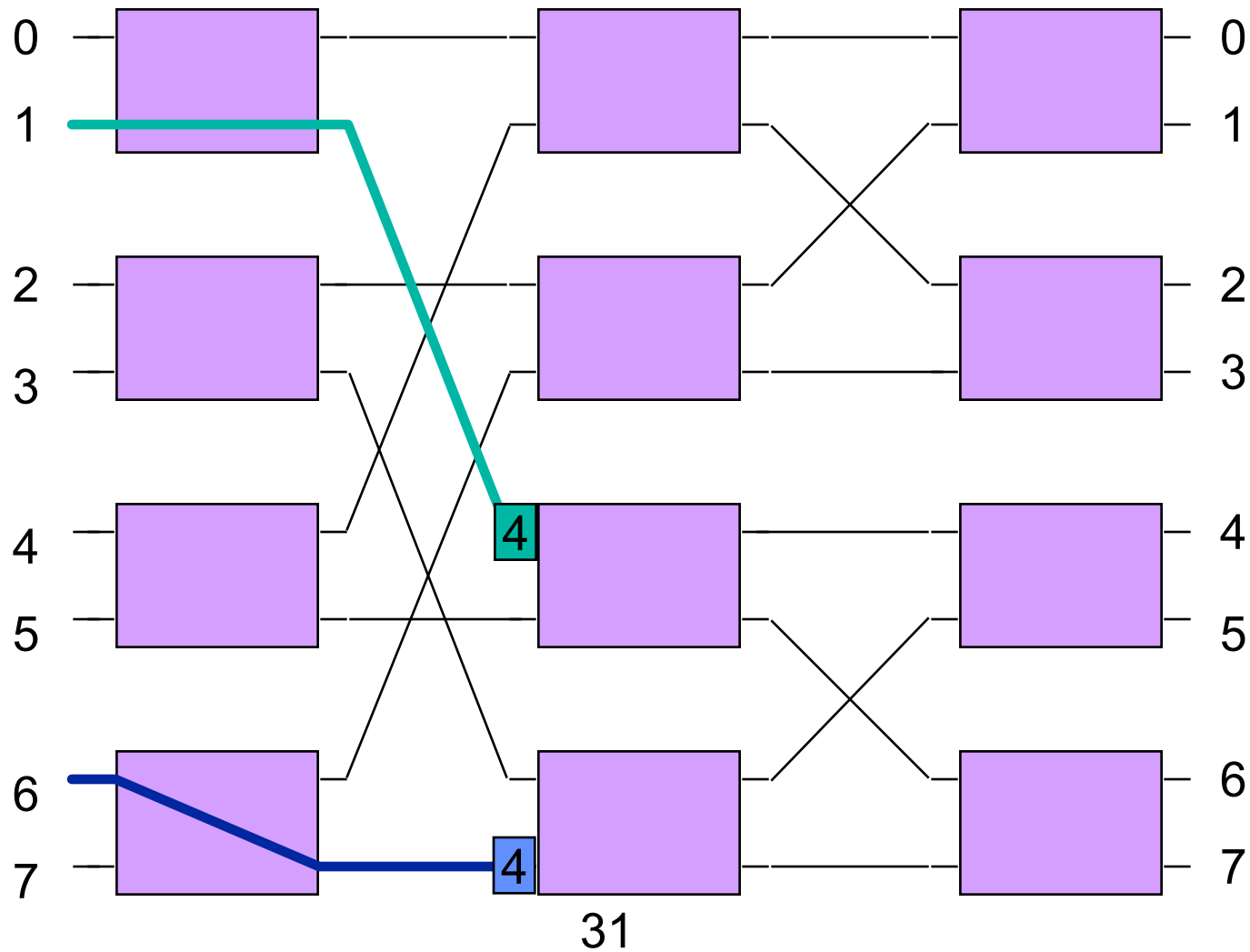
# Output Port Contention



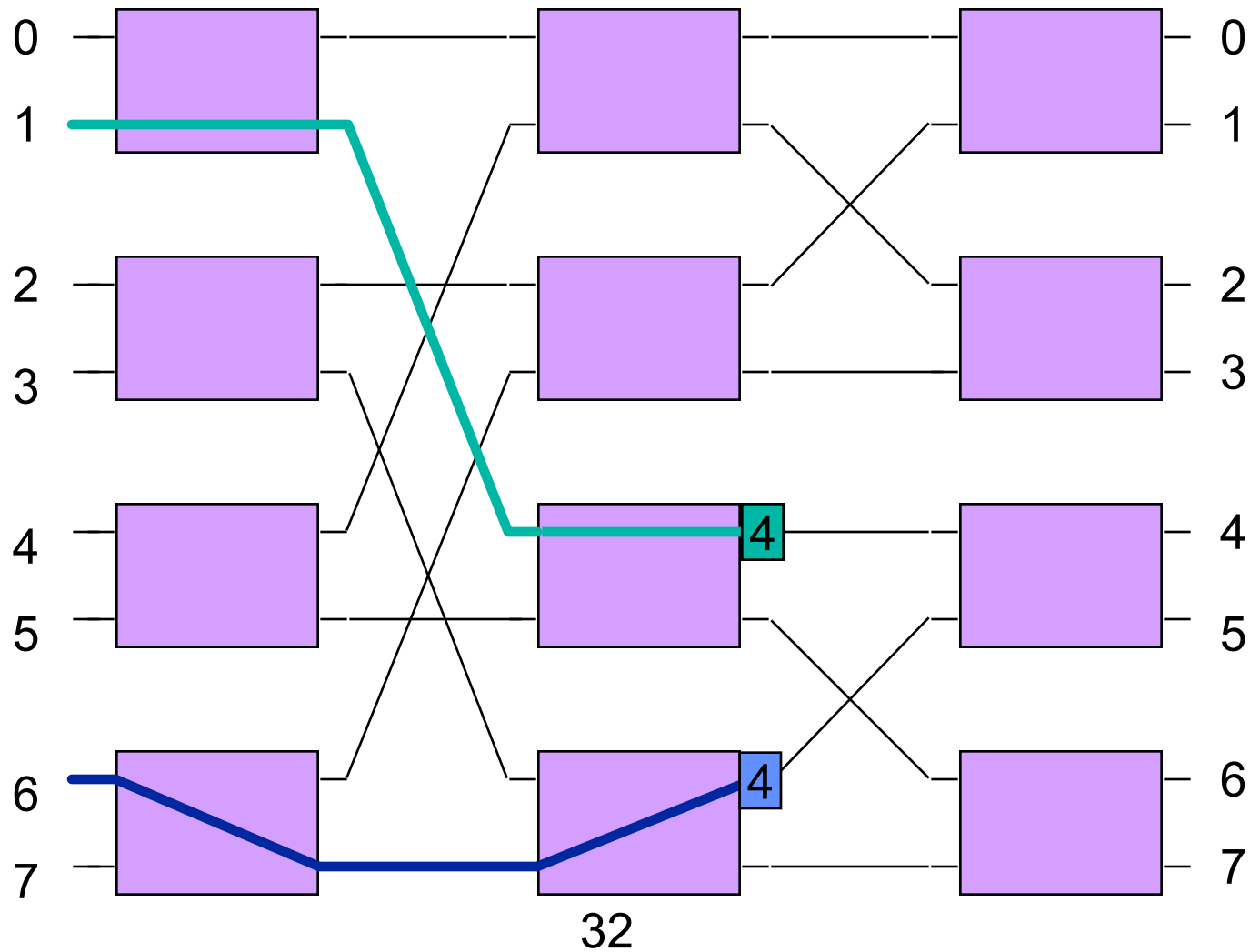
# Output Port Contention



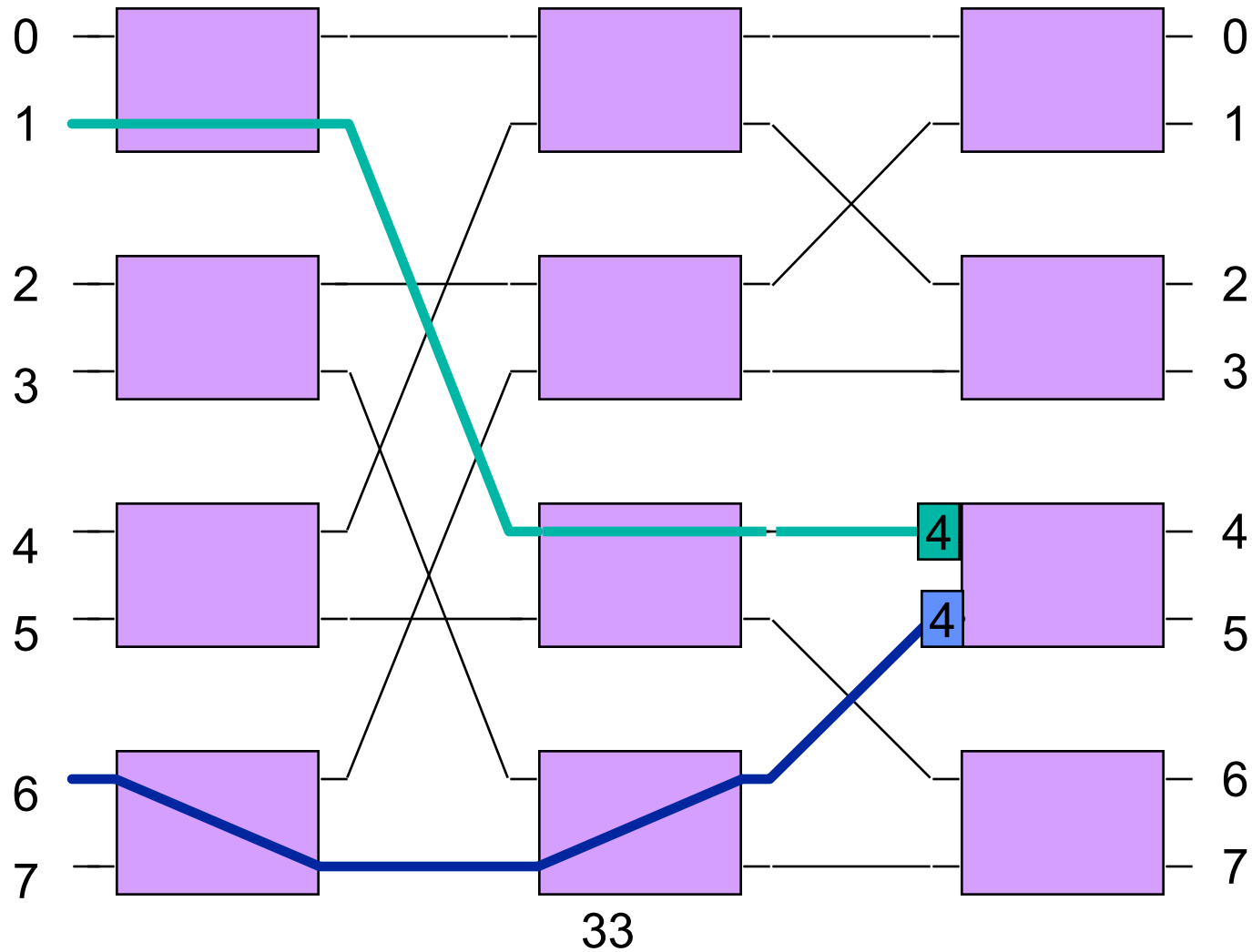
# Output Port Contention



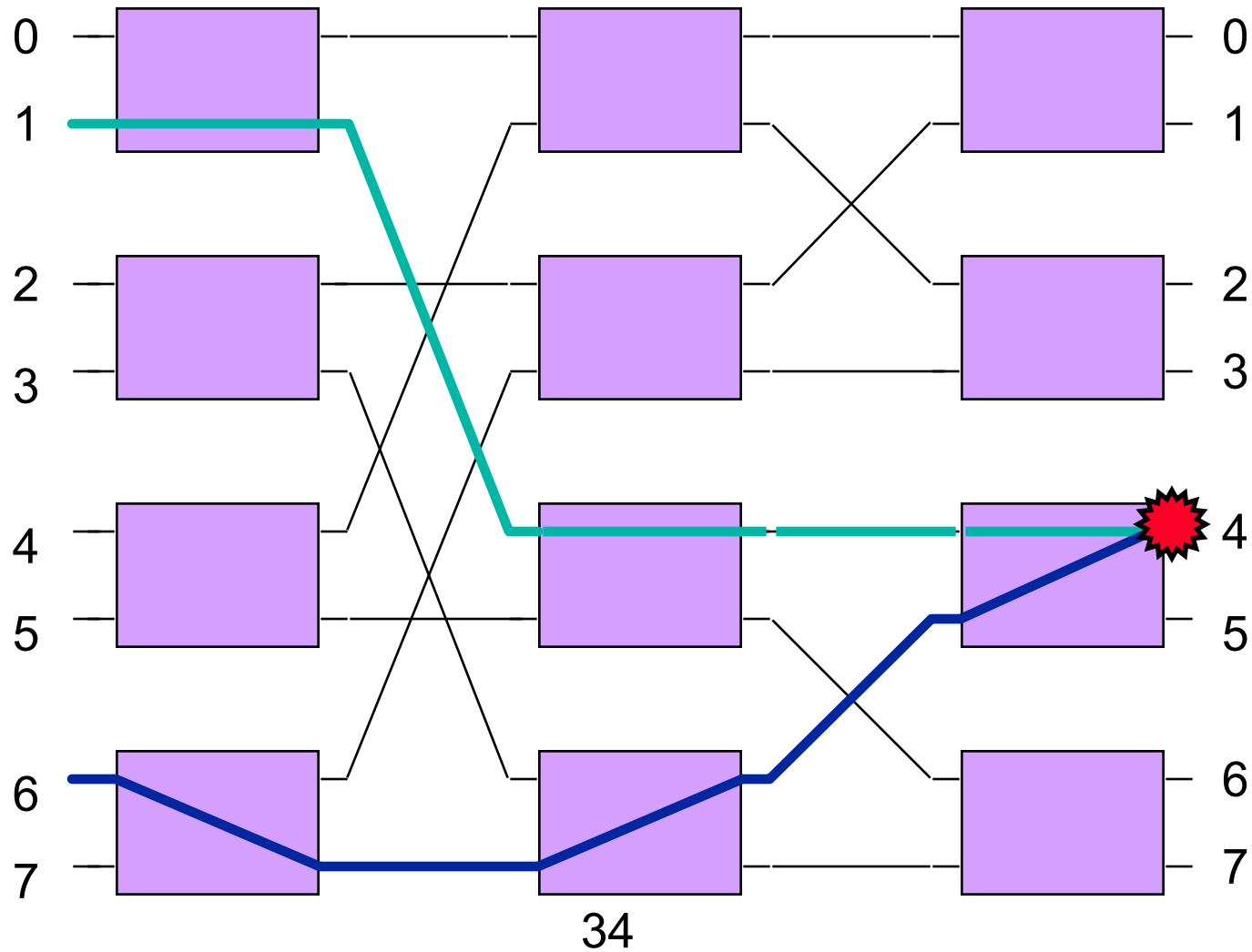
# Output Port Contention



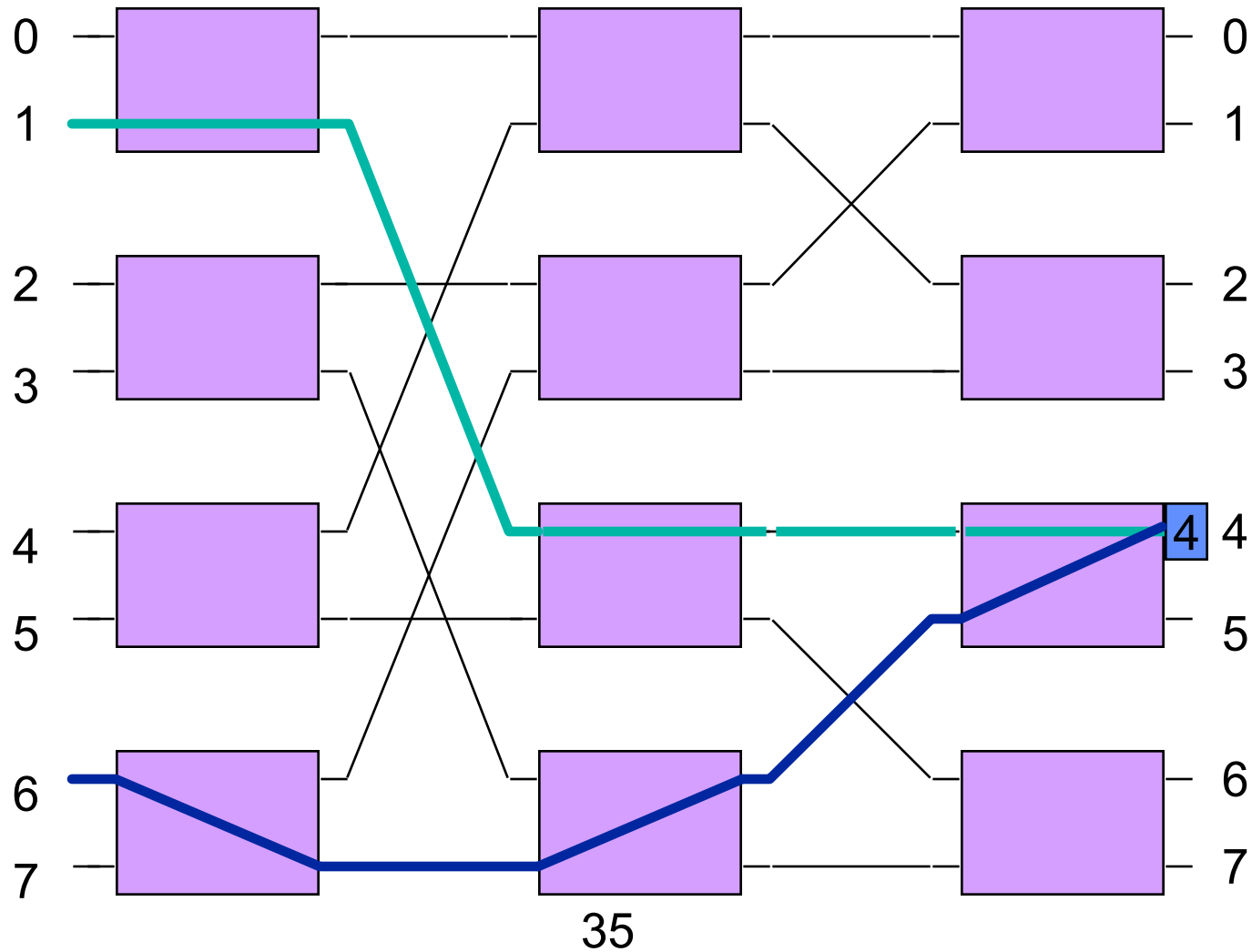
# Output Port Contention



# Output Port Contention



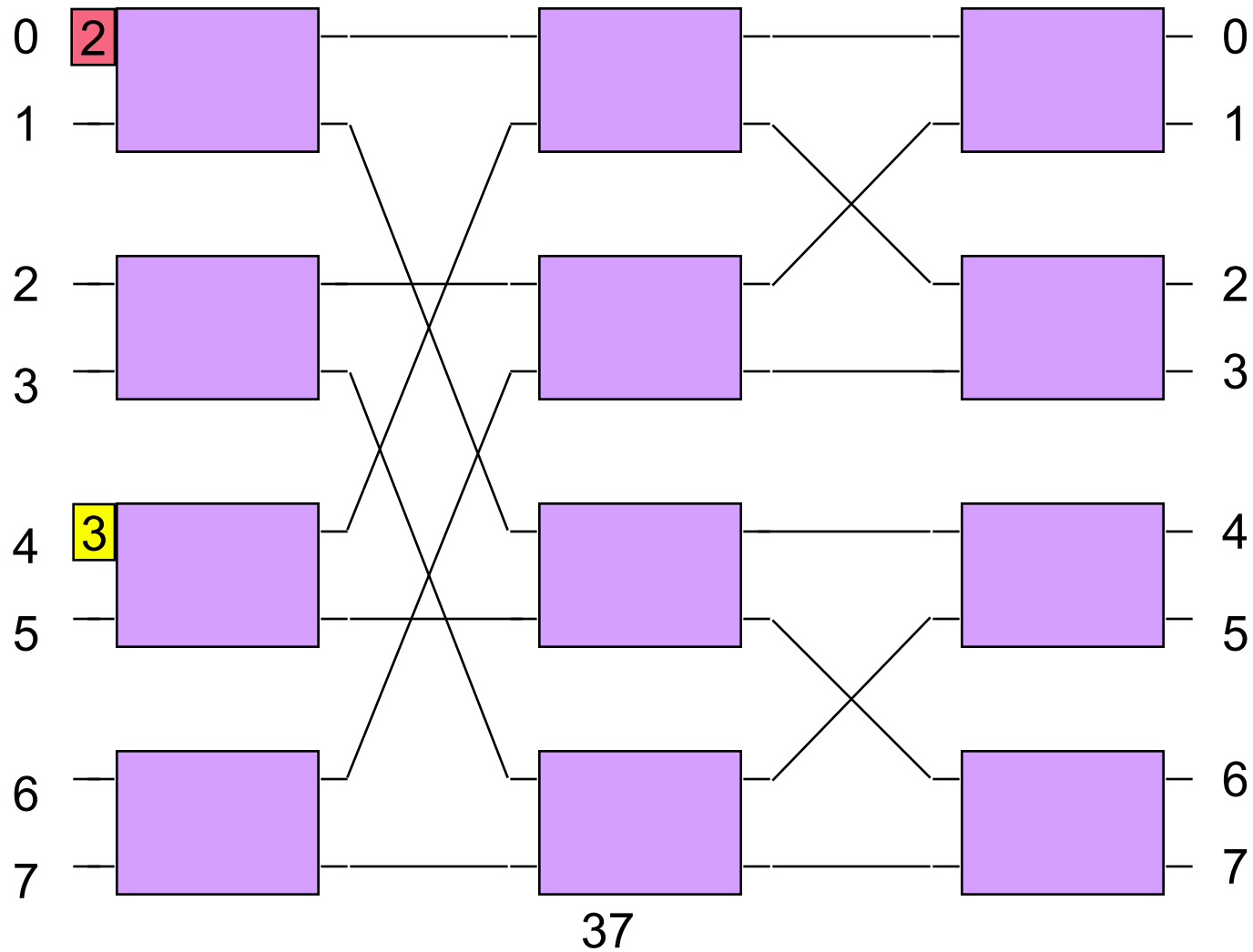
# Output Port Contention



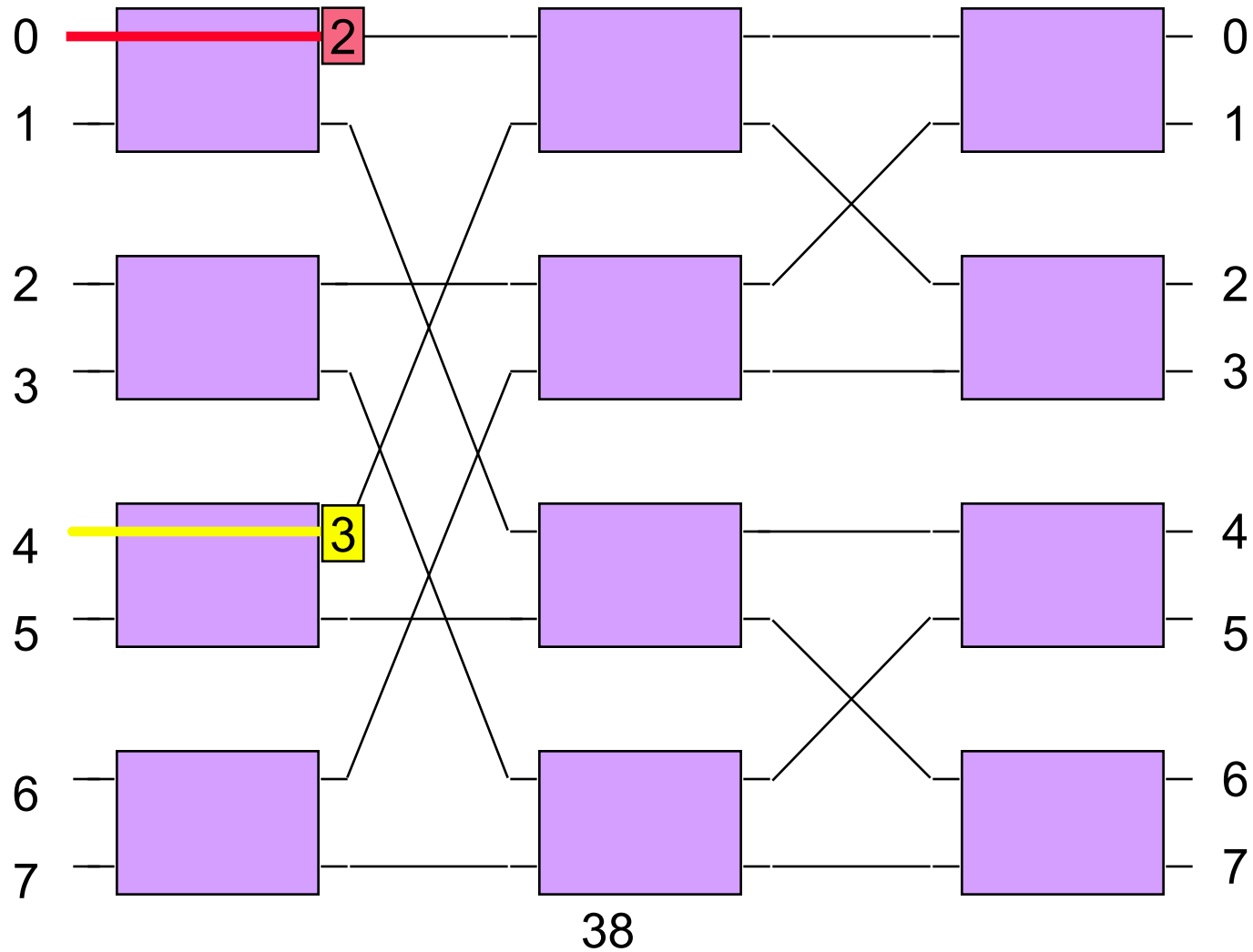
# Path Contention

- It is also possible for two incoming cells that are destined to different output ports to require the same internal link in the switch
- Called path contention or internal blocking
- Again, the result in a bufferless switch fabric is cell loss (one cell wins, one loses)
- Path contention and output port contention can seriously degrade the achievable throughput of the switch

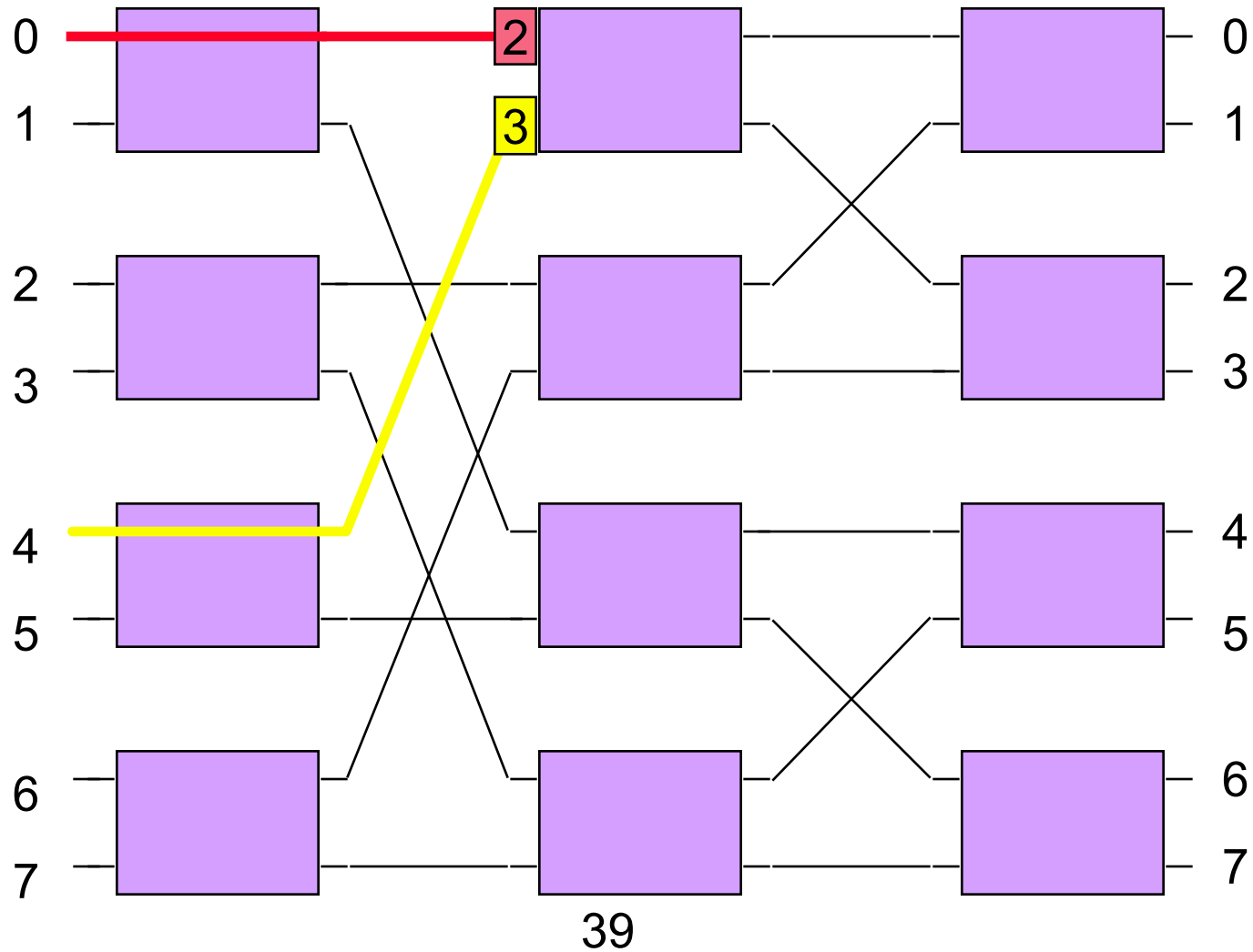
# Path Contention



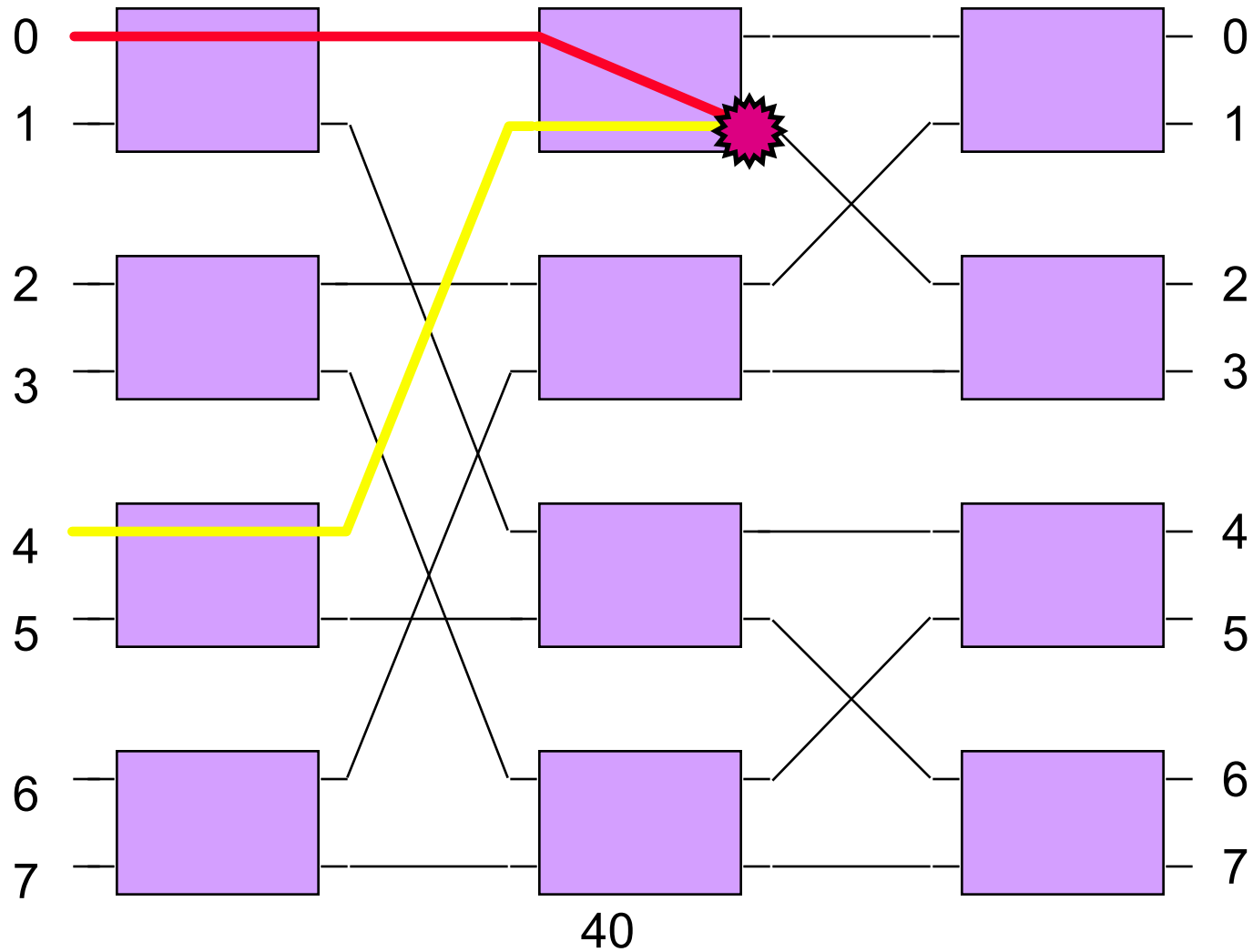
# Path Contention



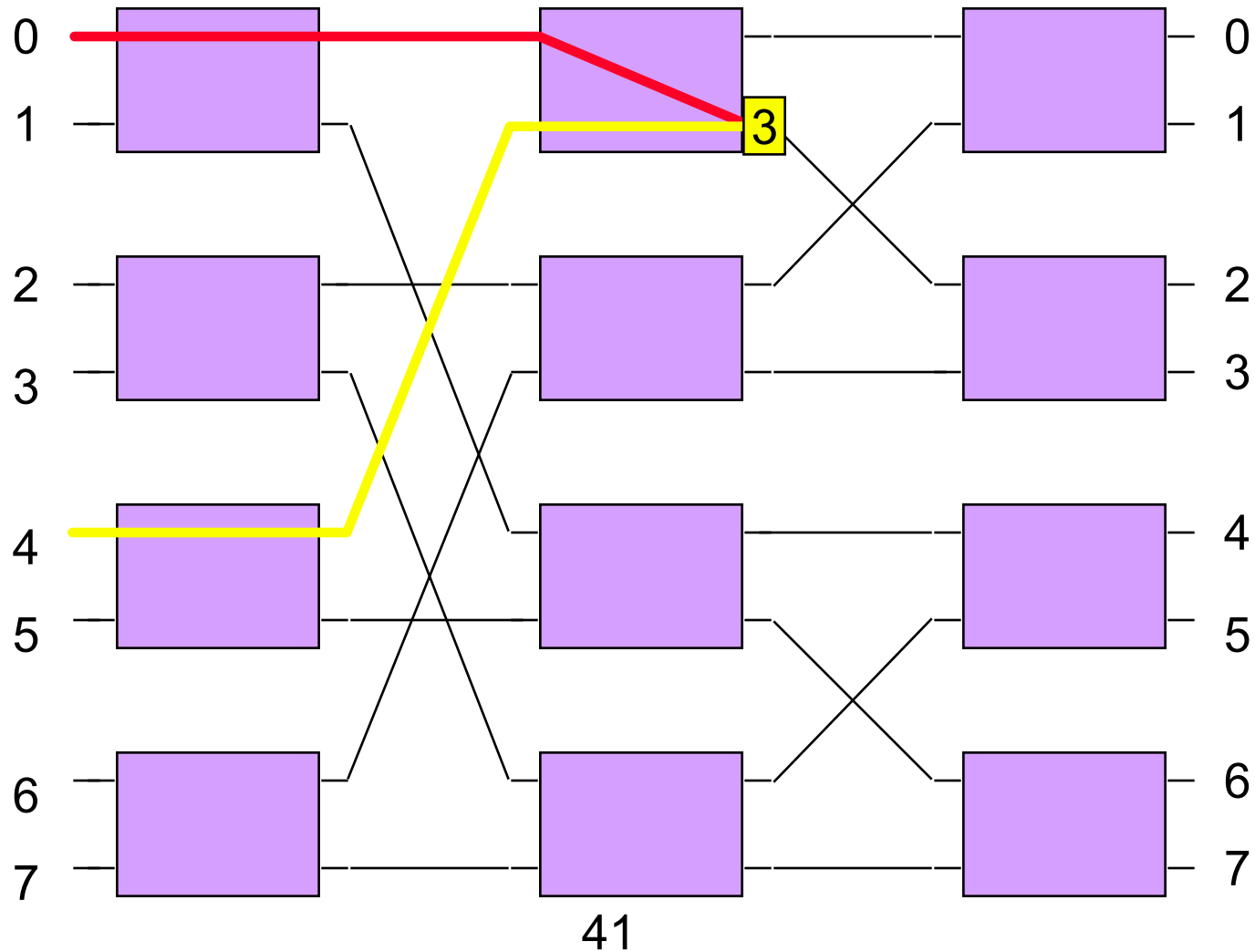
# Path Contention



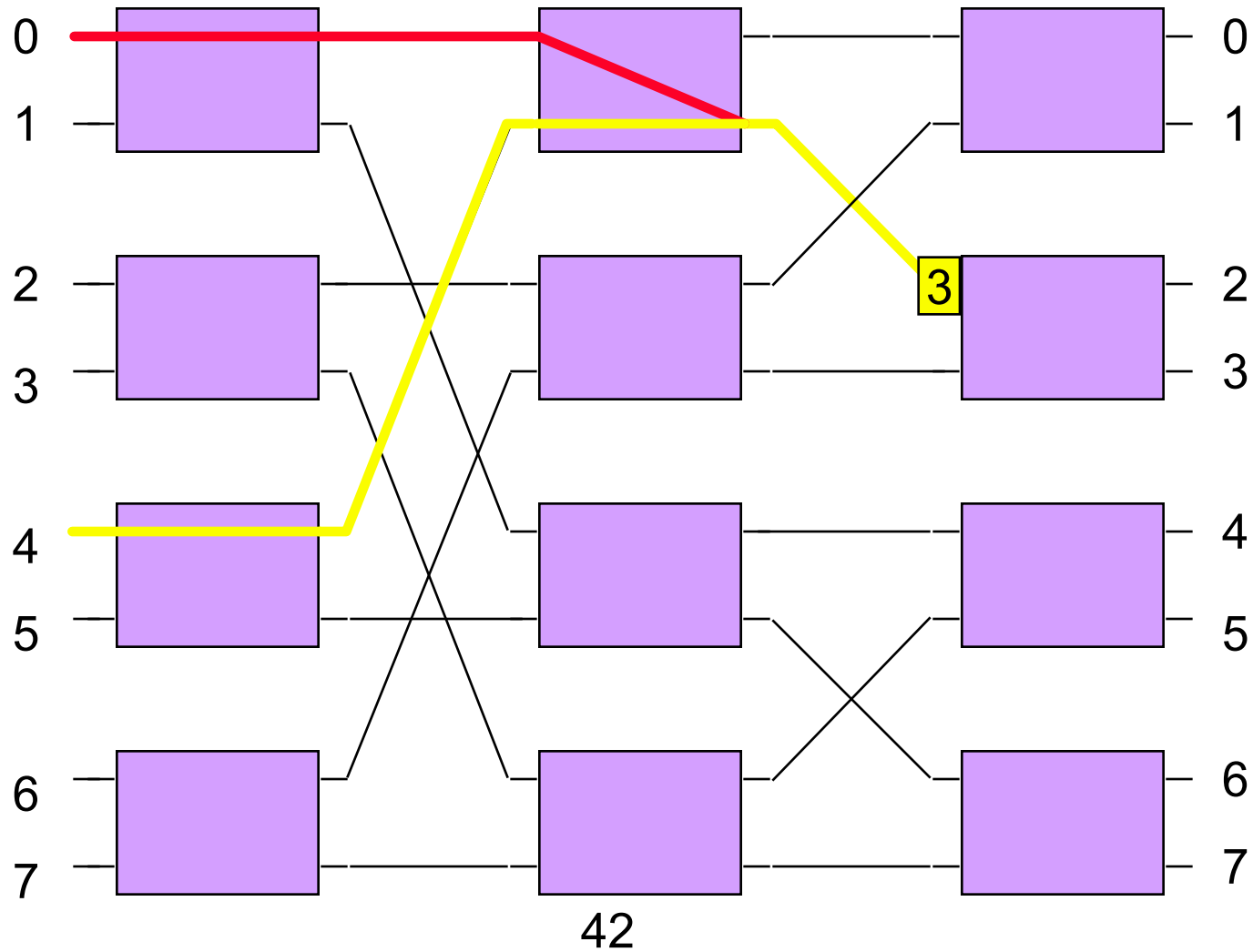
# Path Contention



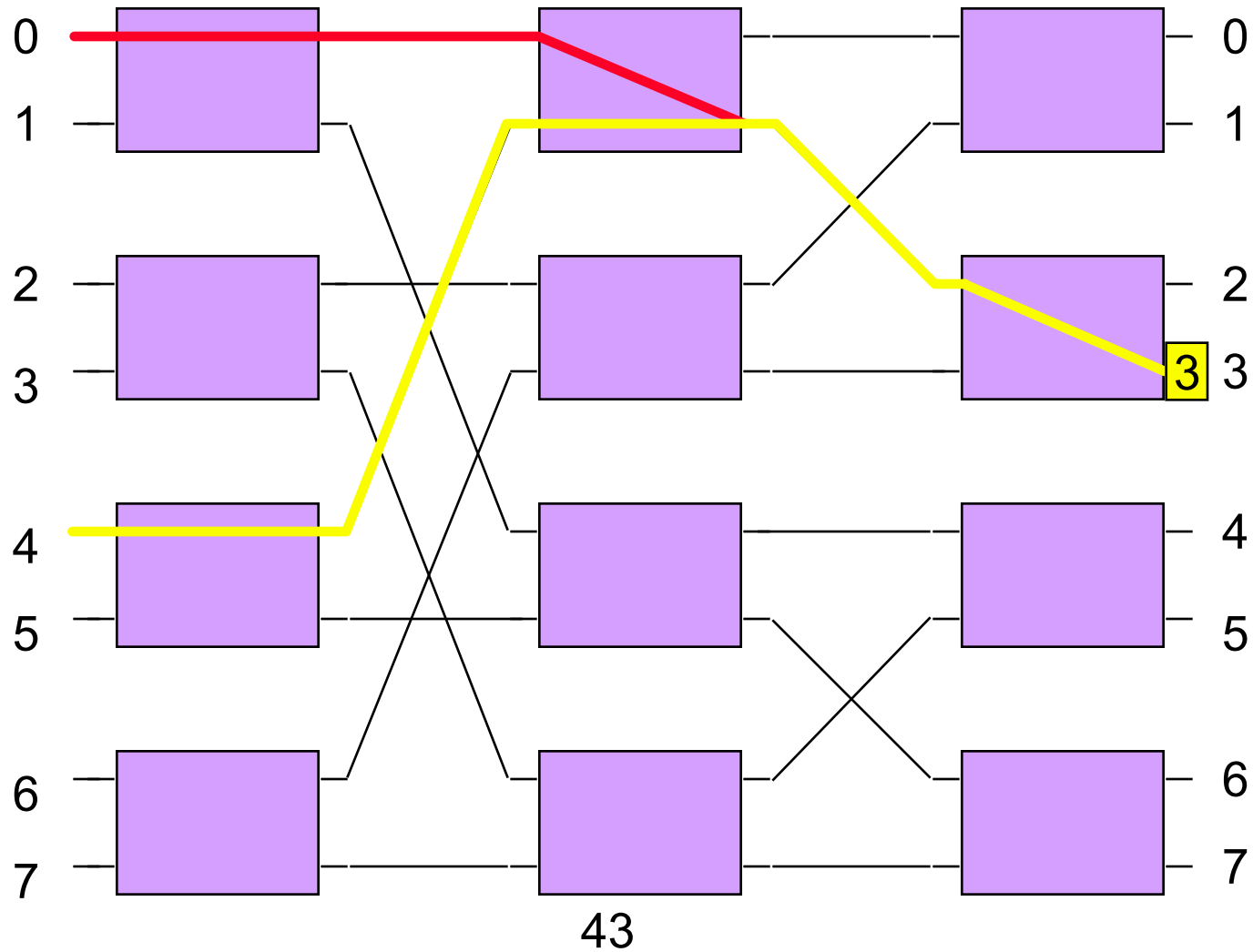
# Path Contention



# Path Contention

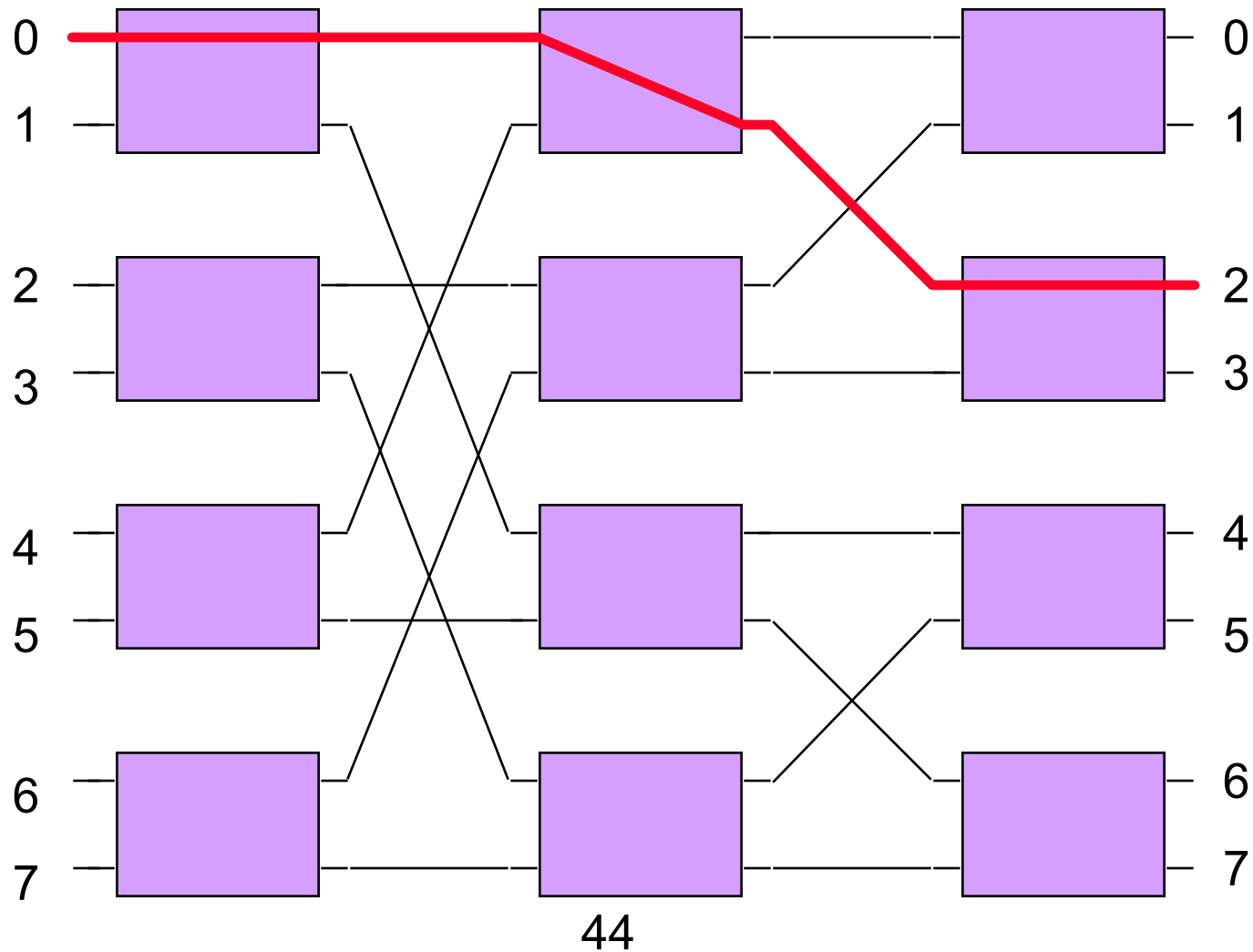


# Path Contention



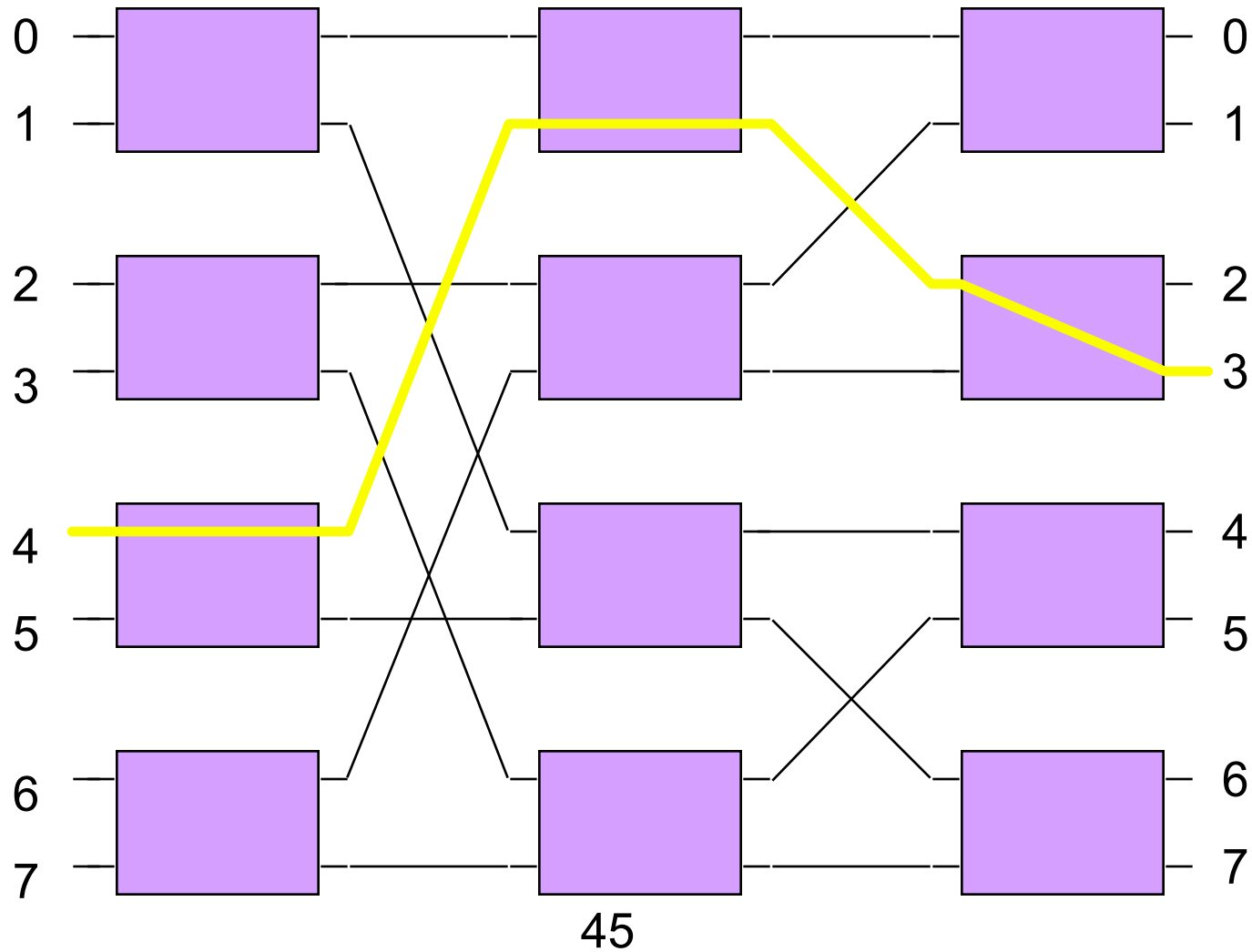
# 8 x 8 DELTA NETWORK

Cell on input port 0 destined for output port 2



# 8 x 8 DELTA NETWORK

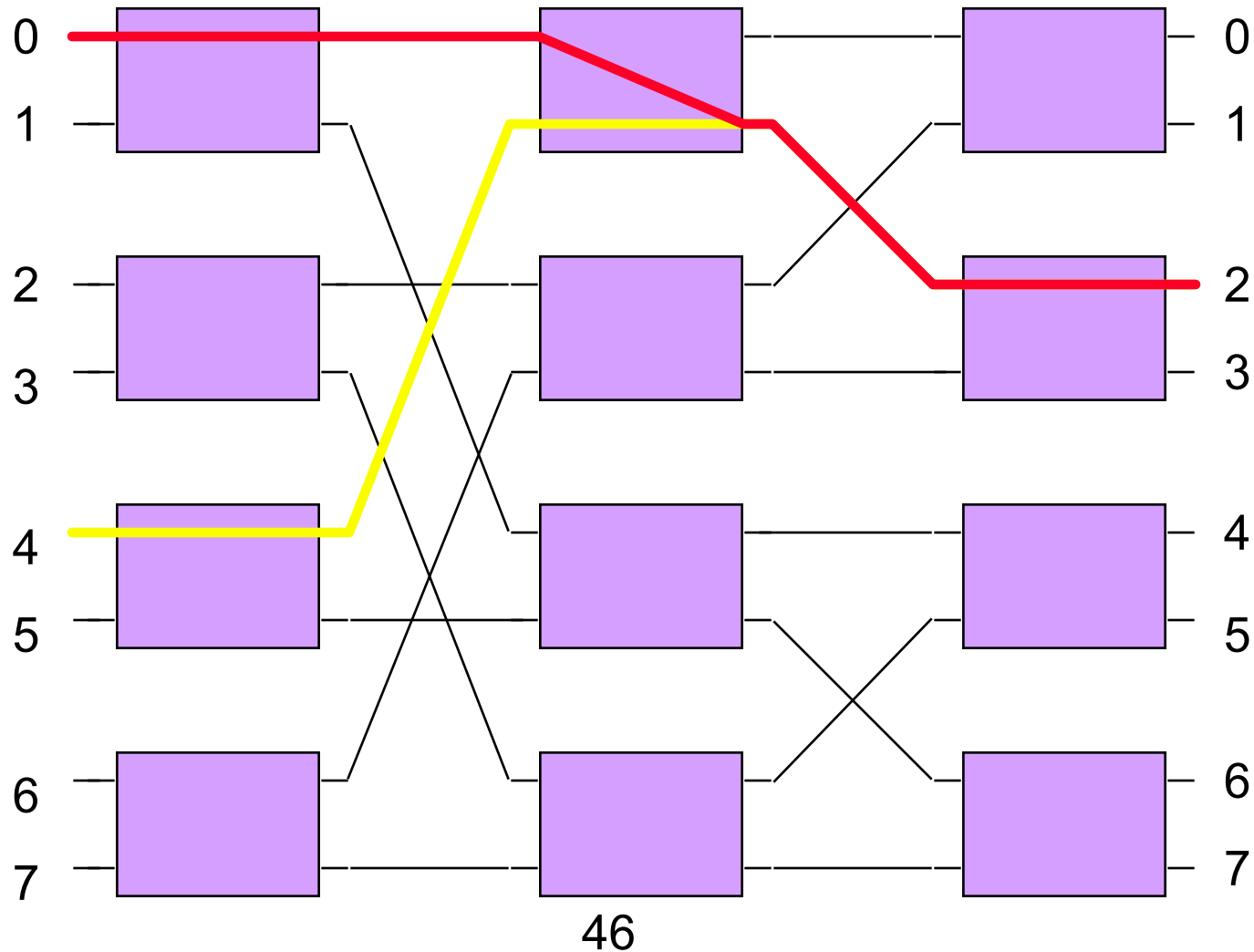
Cell on input port 4 destined for output port 3



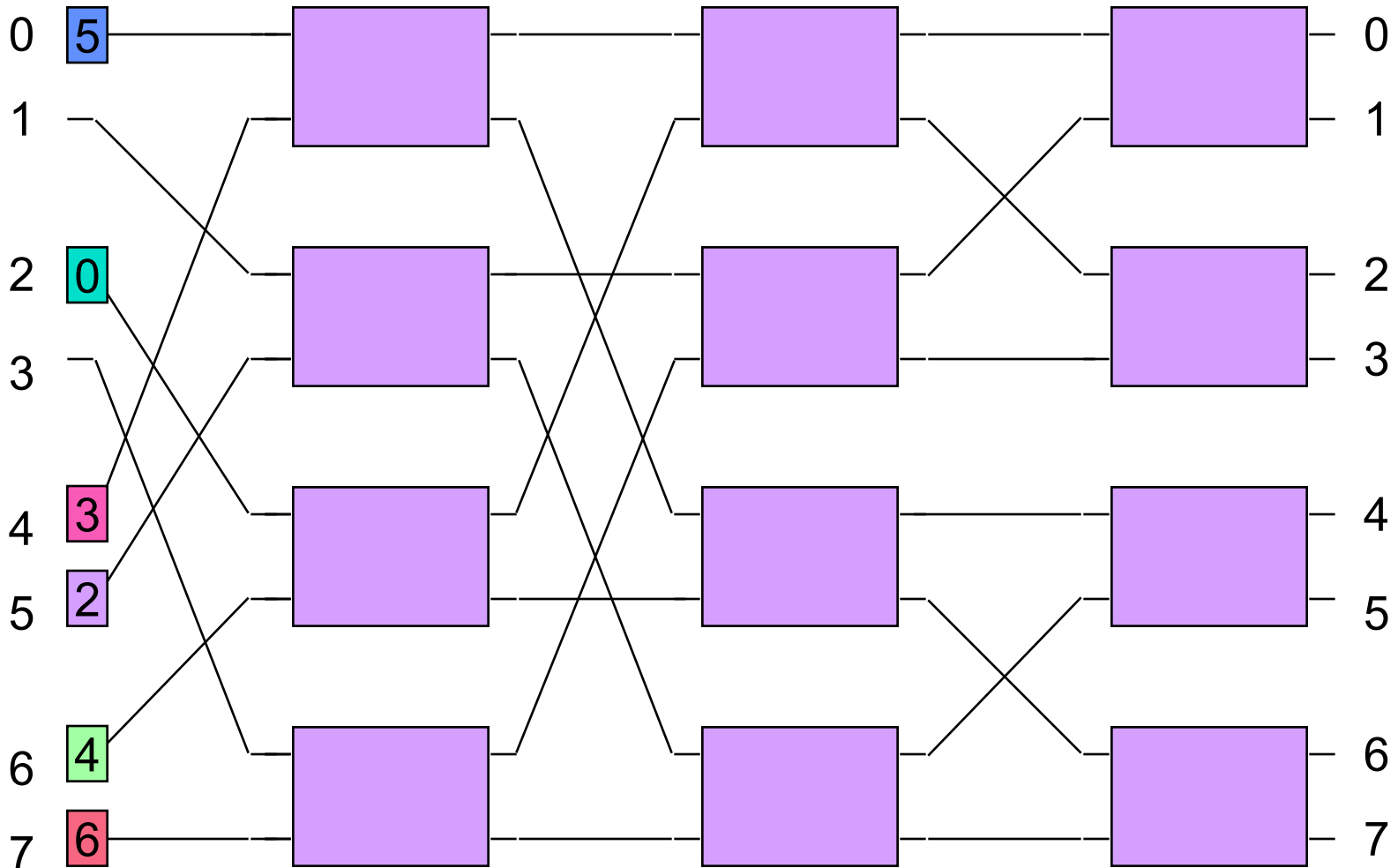
# INTERNAL BLOCKING

Cell on input port 0 destined for output port 2

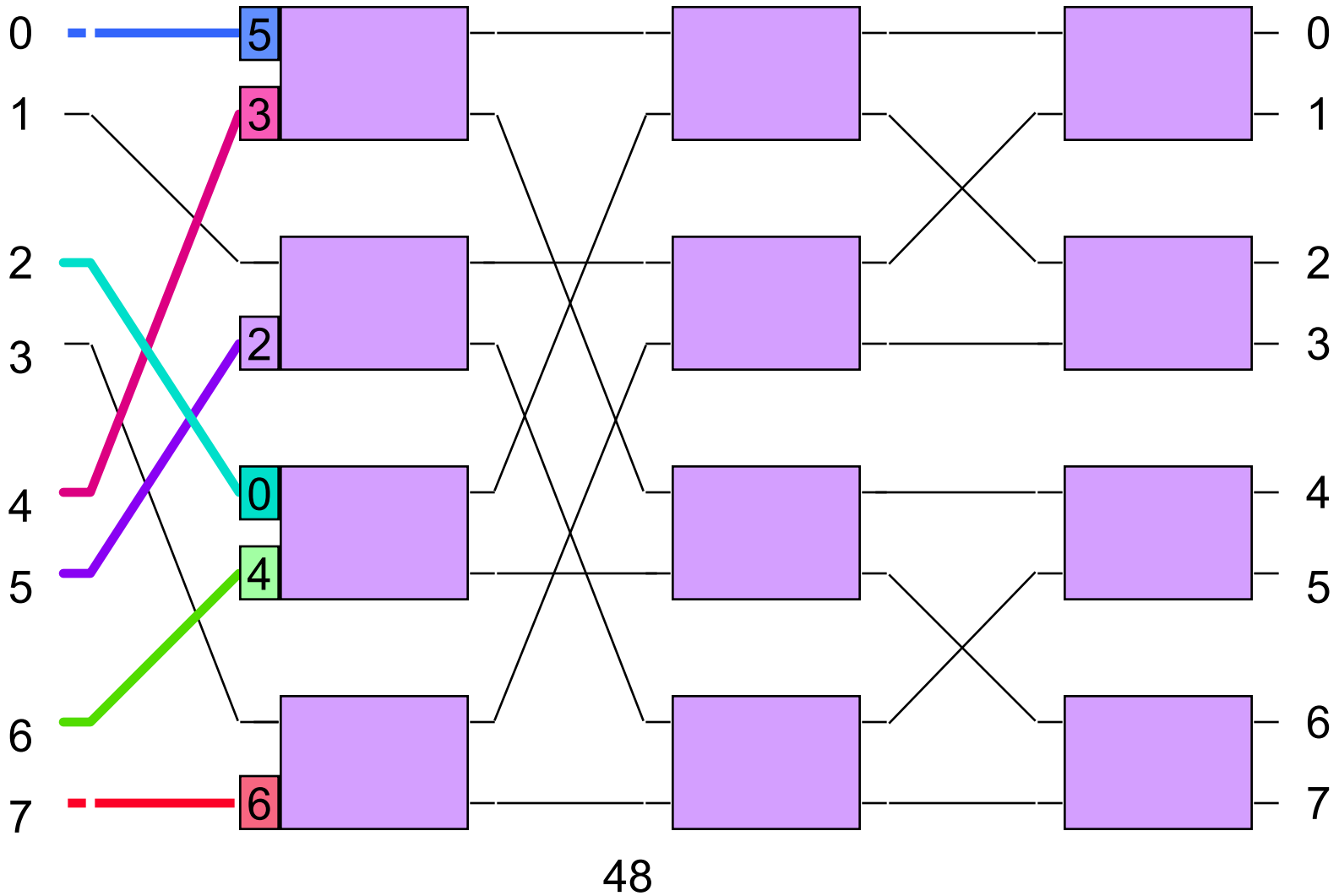
Cell on input port 4 destined for output port 3



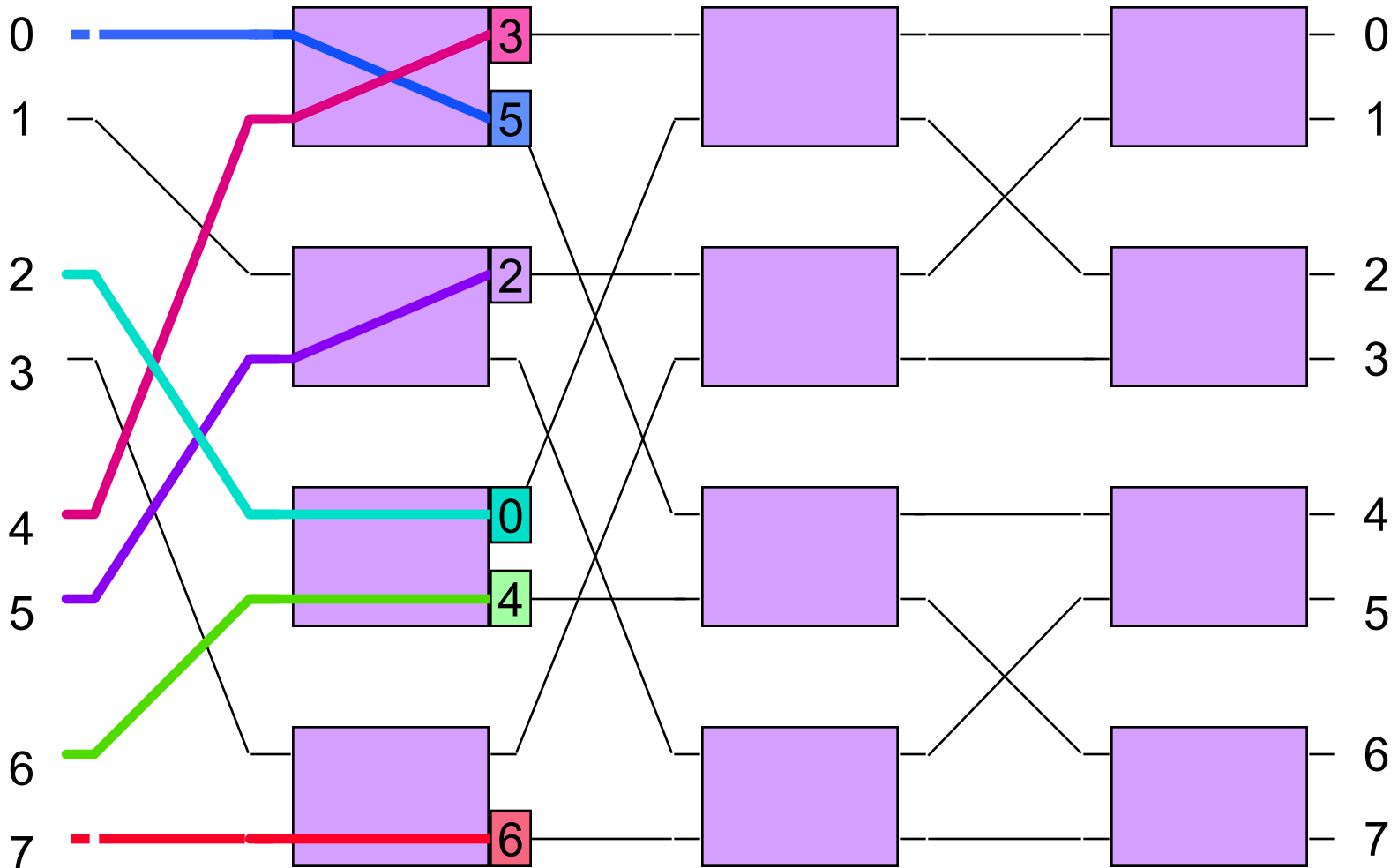
# Performance Degradation



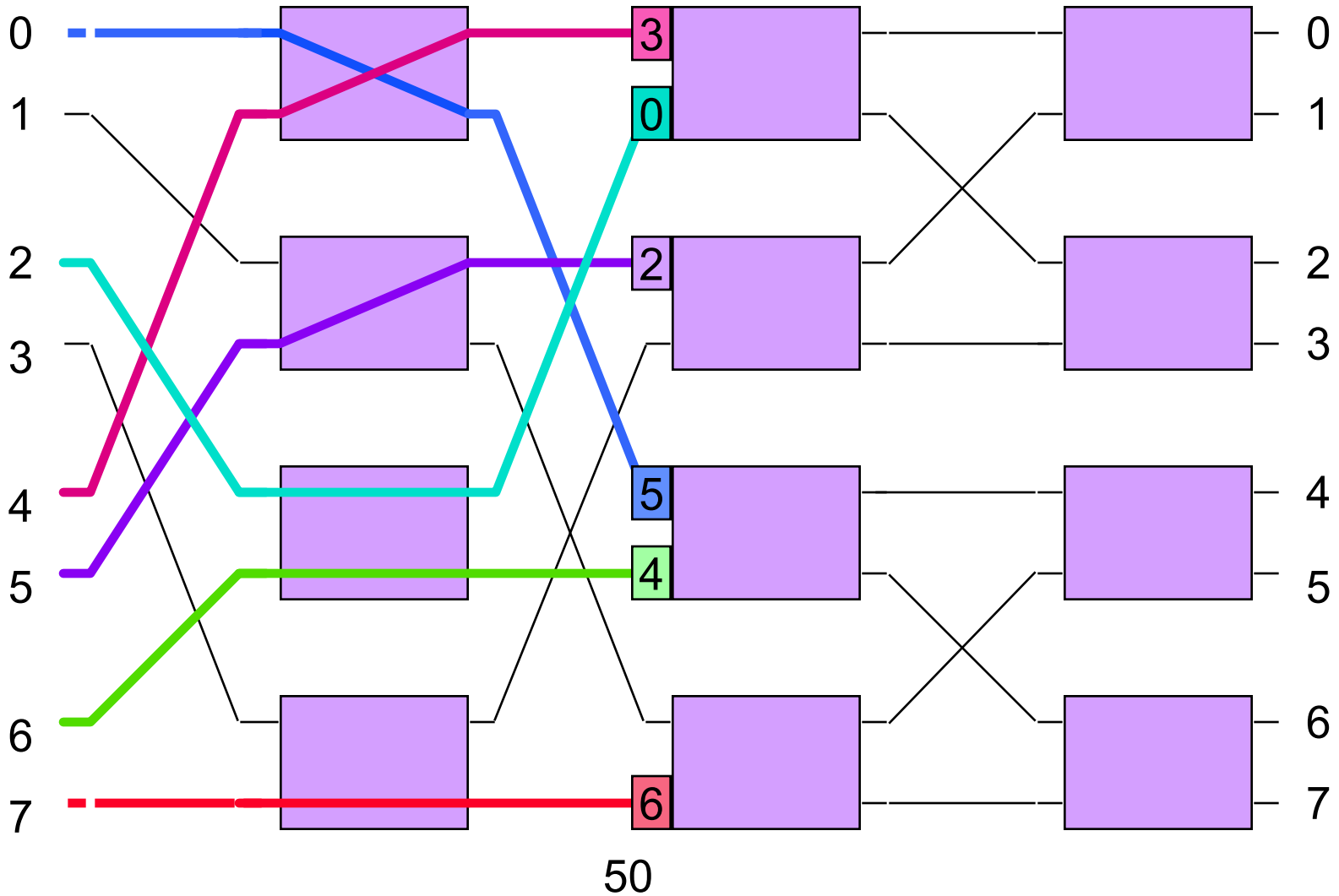
# Performance Degradation



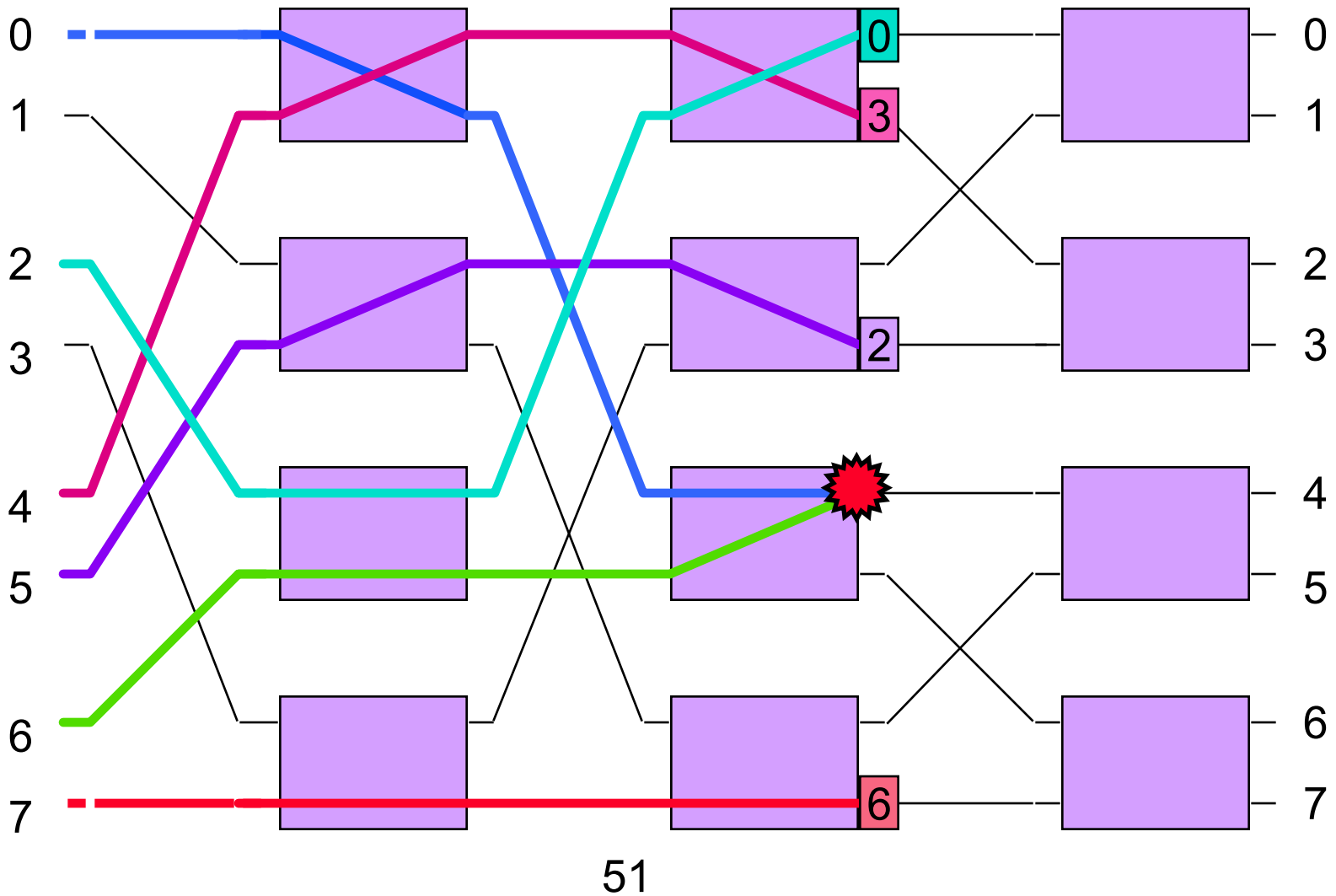
# Performance Degradation



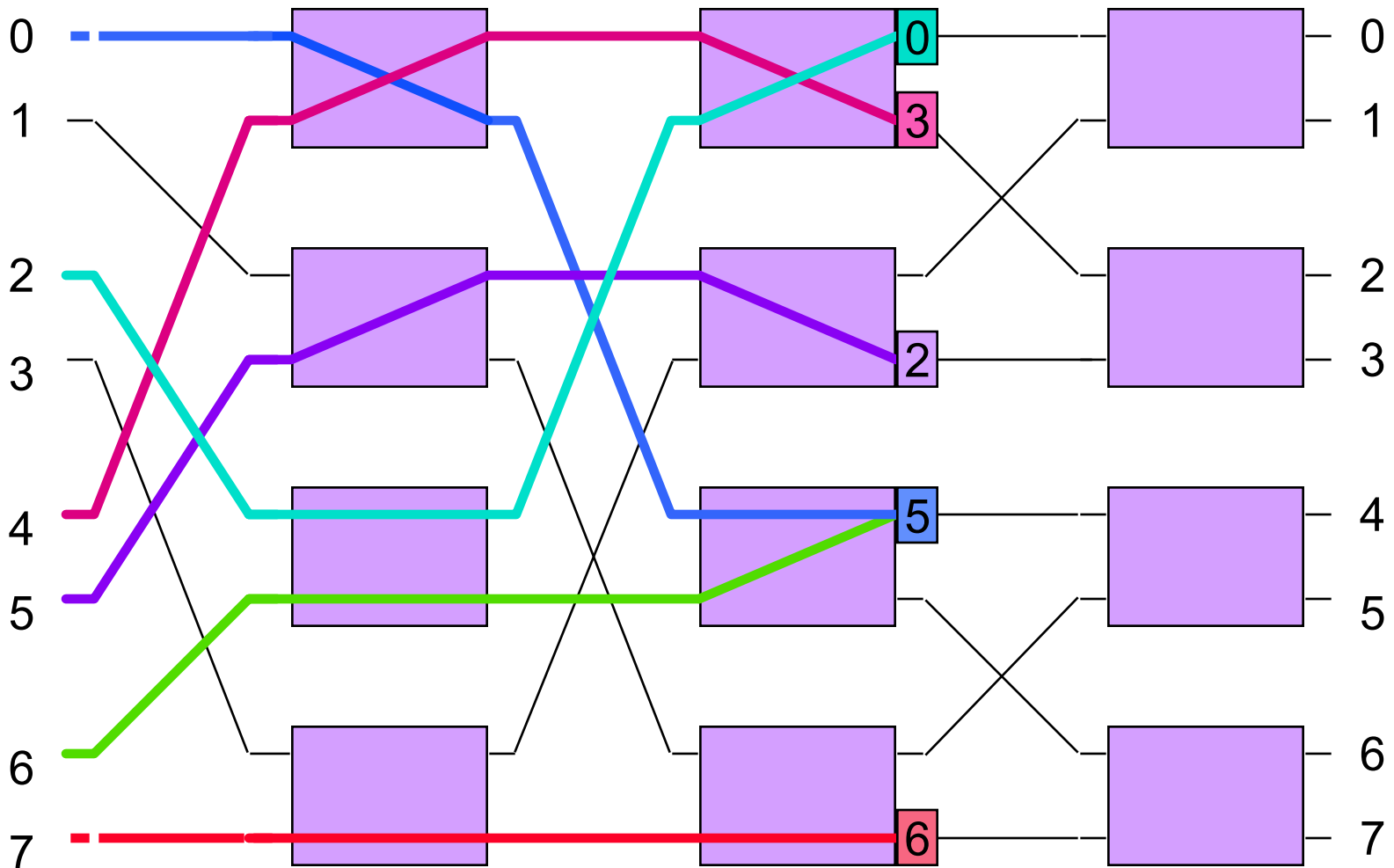
# Performance Degradation



# Performance Degradation

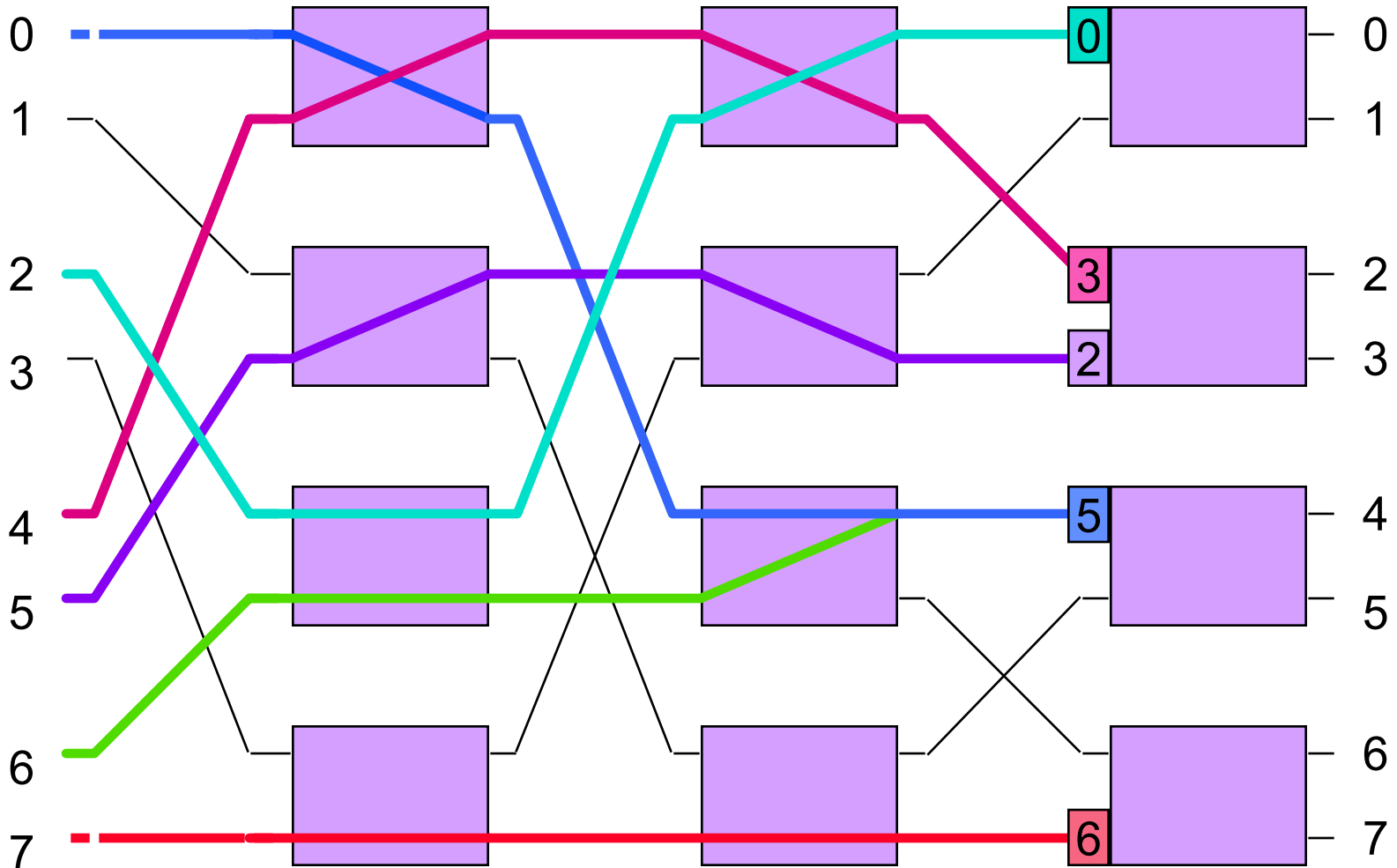


# Performance Degradation



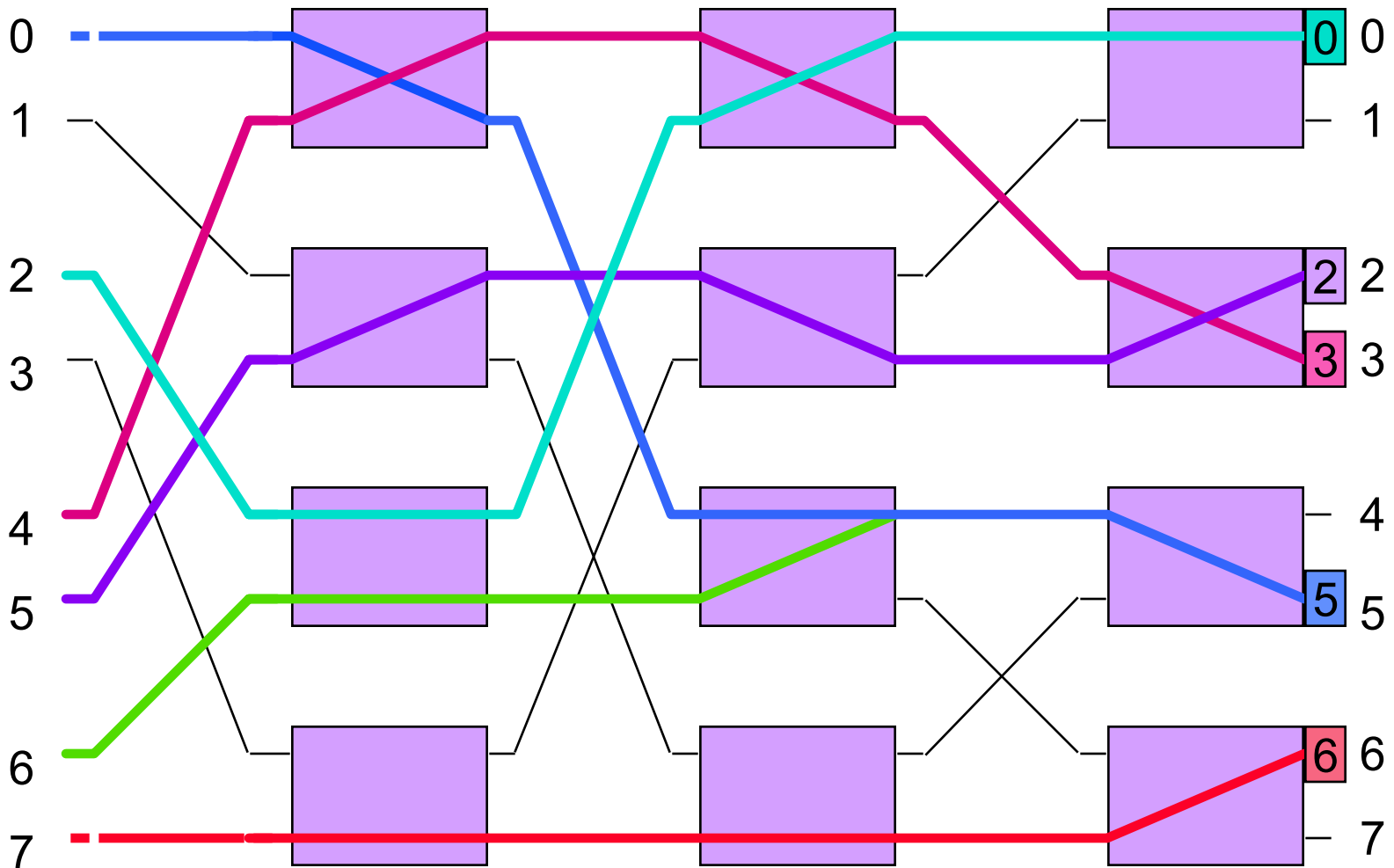
52

# Performance Degradation



53

# Performance Degradation



54

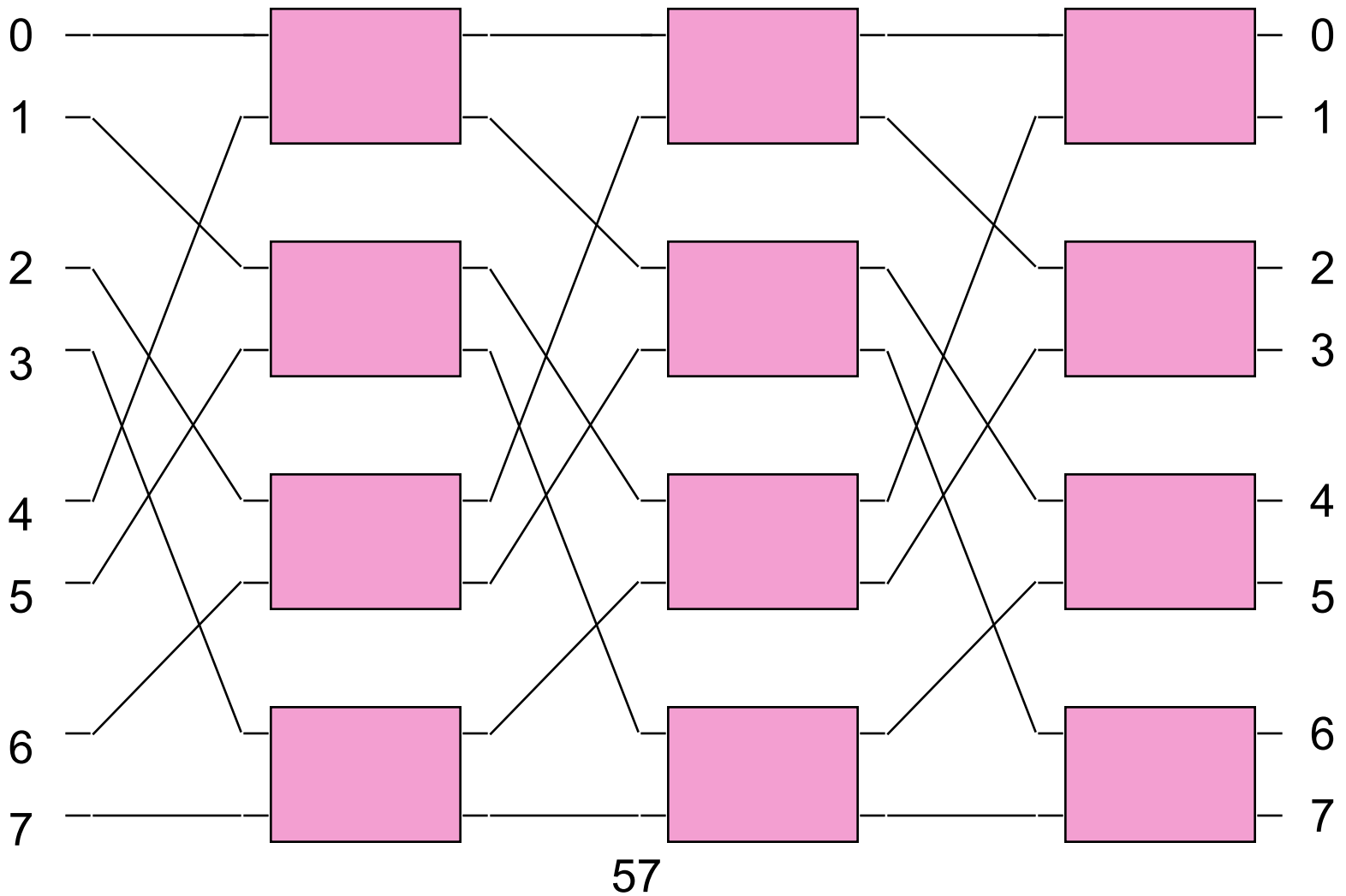
# Omega Network

- The omega network is another example of a banyan multistage interconnection network that can be used as a switch fabric
- The omega differs from the delta network in the pattern of interconnections between the stages
- The omega MIN uses the “perfect shuffle”

# Perfect Shuffle

- The interconnections between stages are defined by the logical “rotate left” of the bits used in the port ids
- Example: 000 ---> 000 ---> 000 ---> 000
- Example: 001 ---> 010 ---> 100 ---> 001
- Example: 011 ---> 110 ---> 101 ---> 011
- Example: 111 ---> 111 ---> 111 ---> 111

# 8 x 8 OMEGA NETWORK

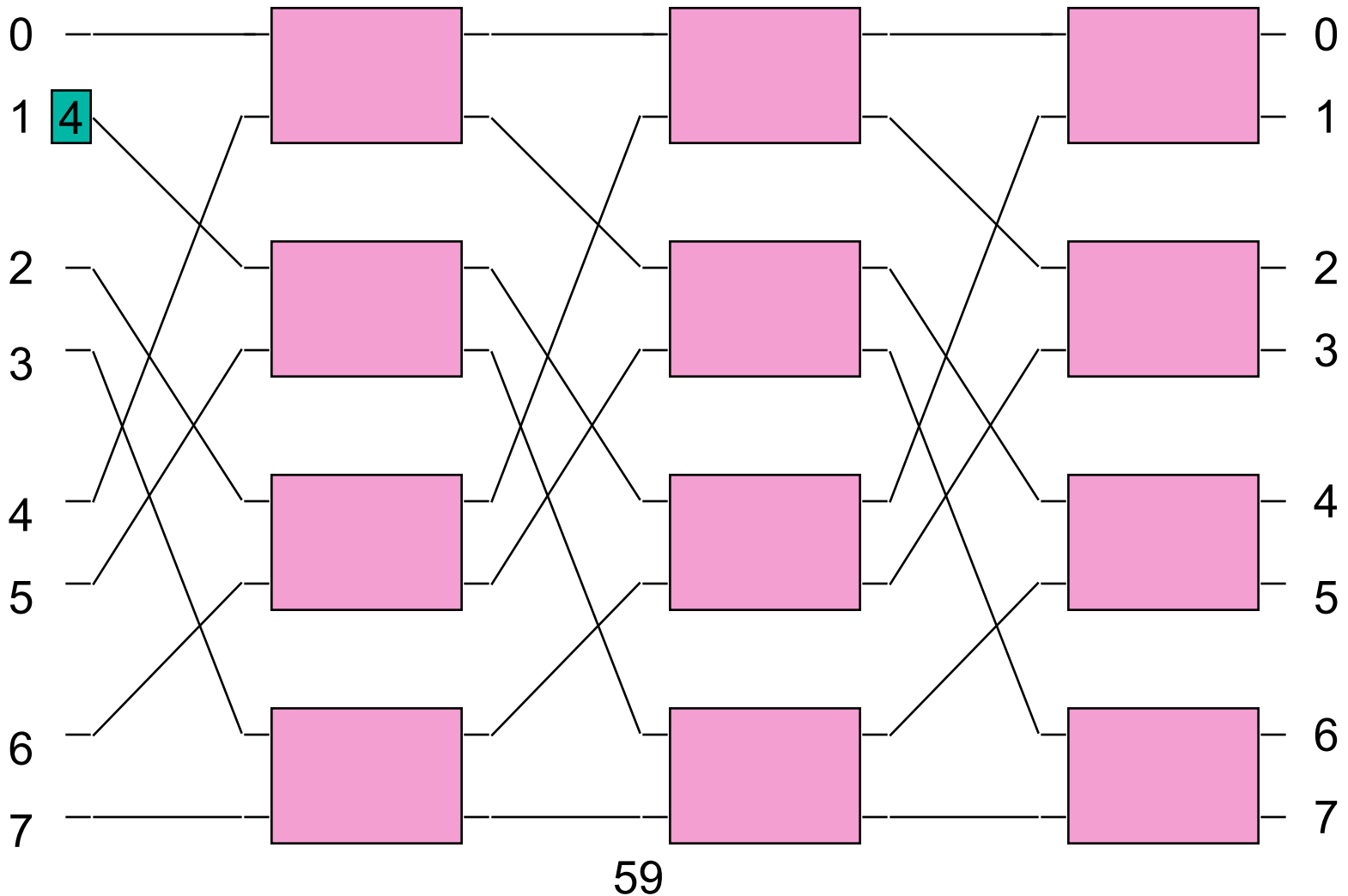


# Self Routing

- Omega network has self-routing property
- The path for a cell to take to reach its destination can be determined directly from its routing tag (i.e., destination port id)
- Stage k of the MIN looks at bit k of the tag
- If bit k is 0, then send cell out upper port
- If bit k is 1, then send cell out lower port
- Works for every possible input port (really!)

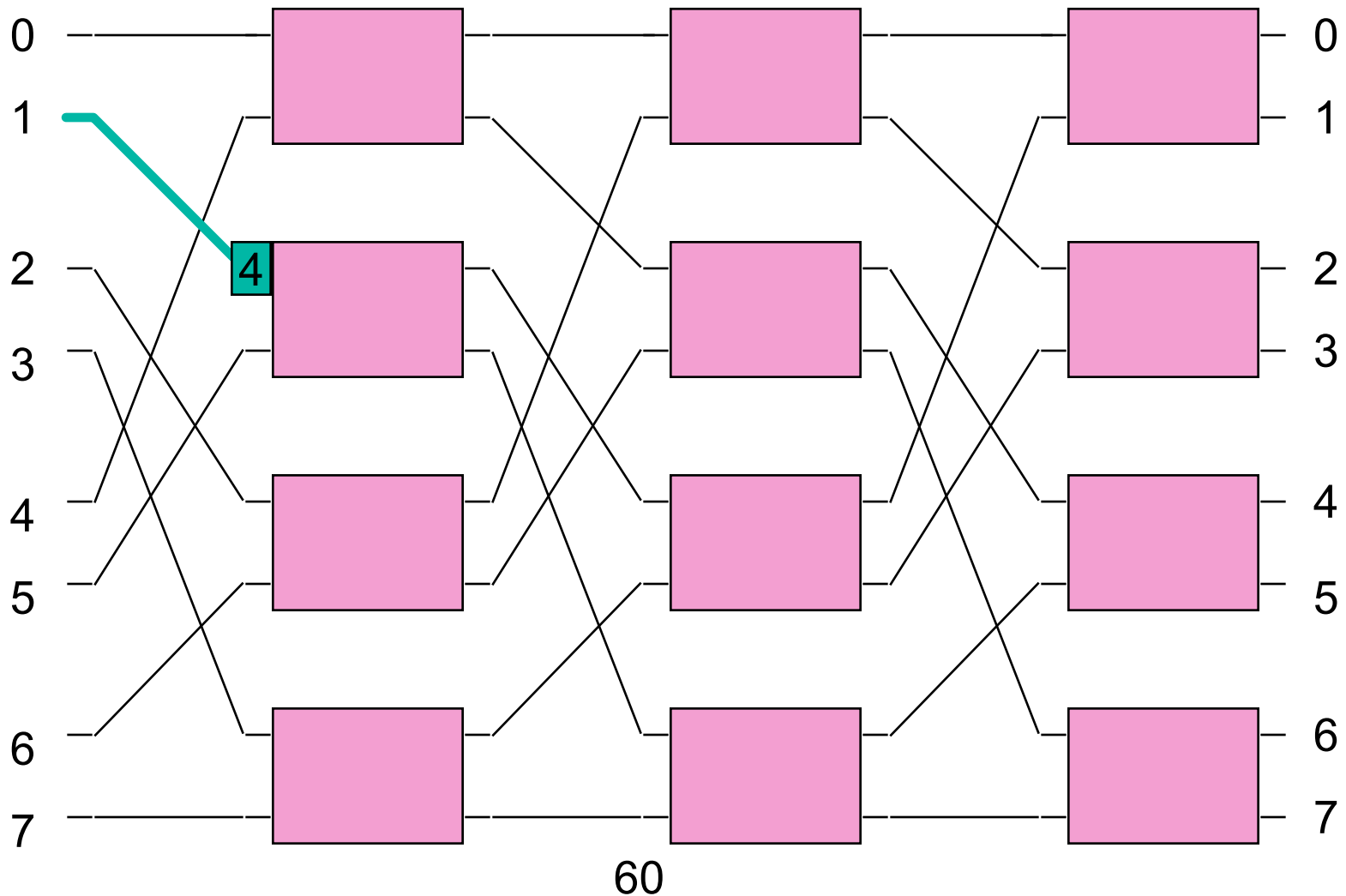
# Example of Self Routing

Cell destined for output port 4 ( $= 100_2$ )



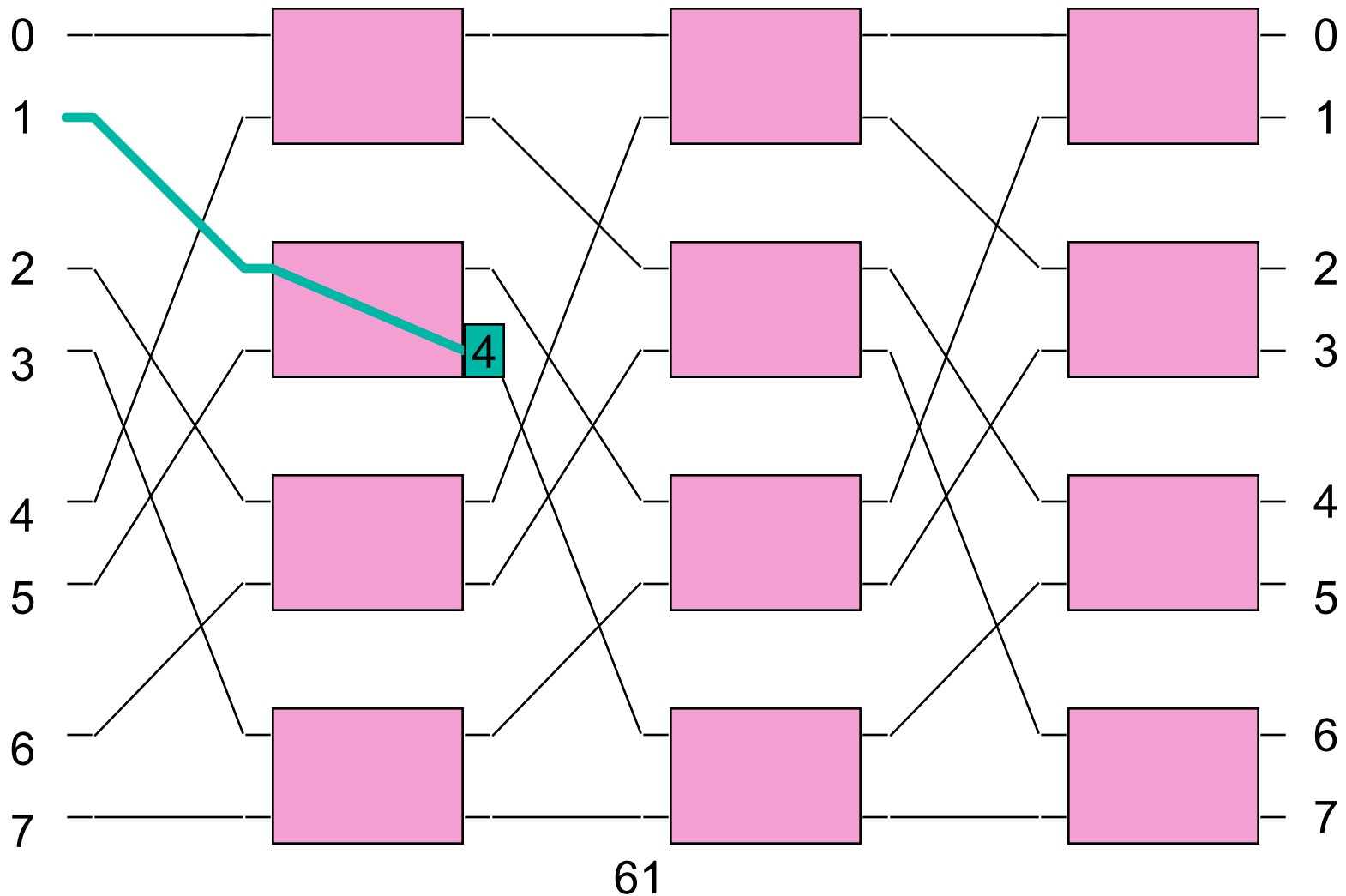
# Example of Self Routing

Cell destined for output port 4 ( $= 100_2$ )



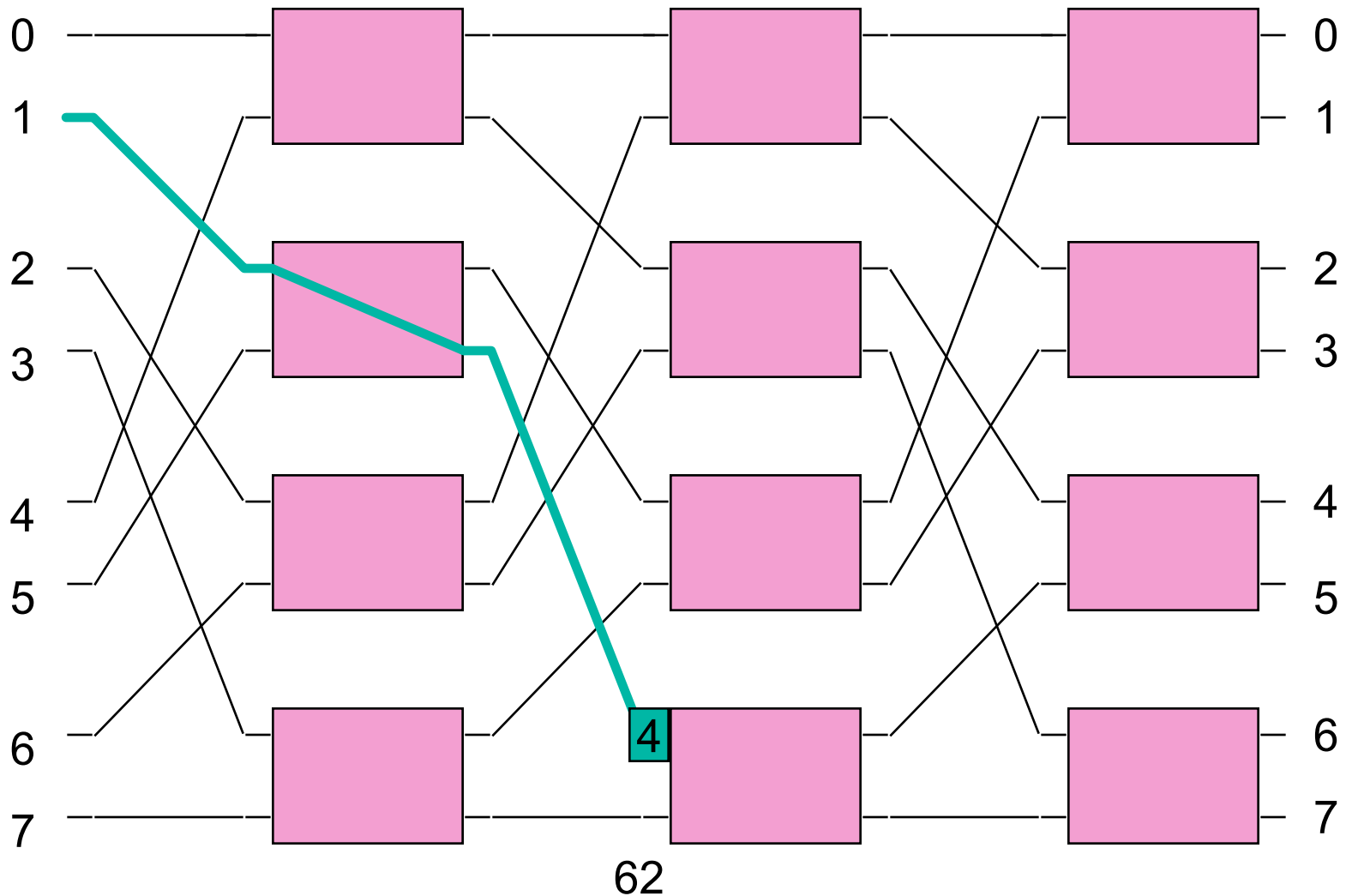
# Example of Self Routing

Cell destined for output port 4 ( $= 100_2$ )



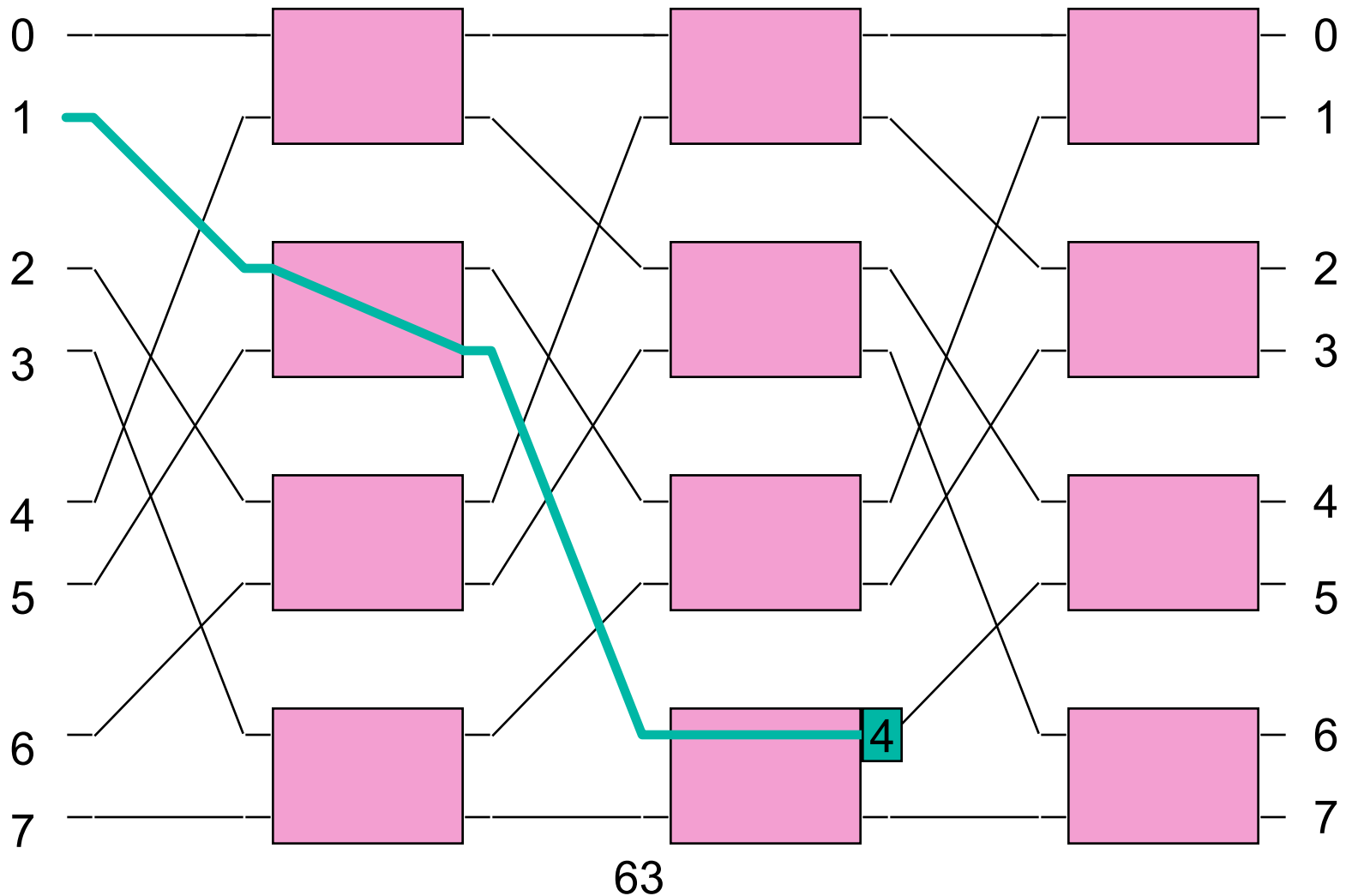
# Example of Self Routing

Cell destined for output port 4 ( $= 100_2$ )



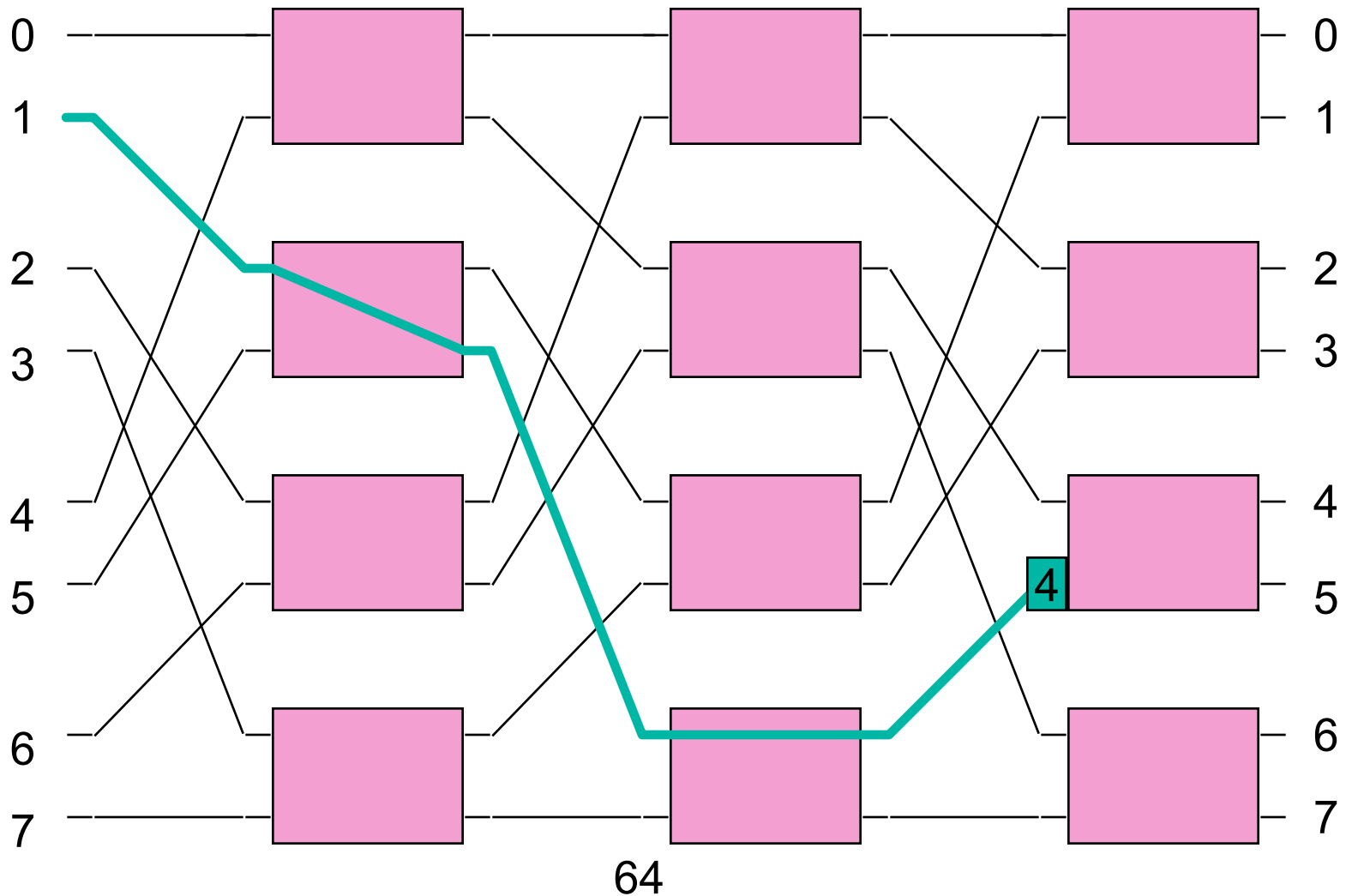
# Example of Self Routing

Cell destined for output port 4 ( $= 100_2$ )



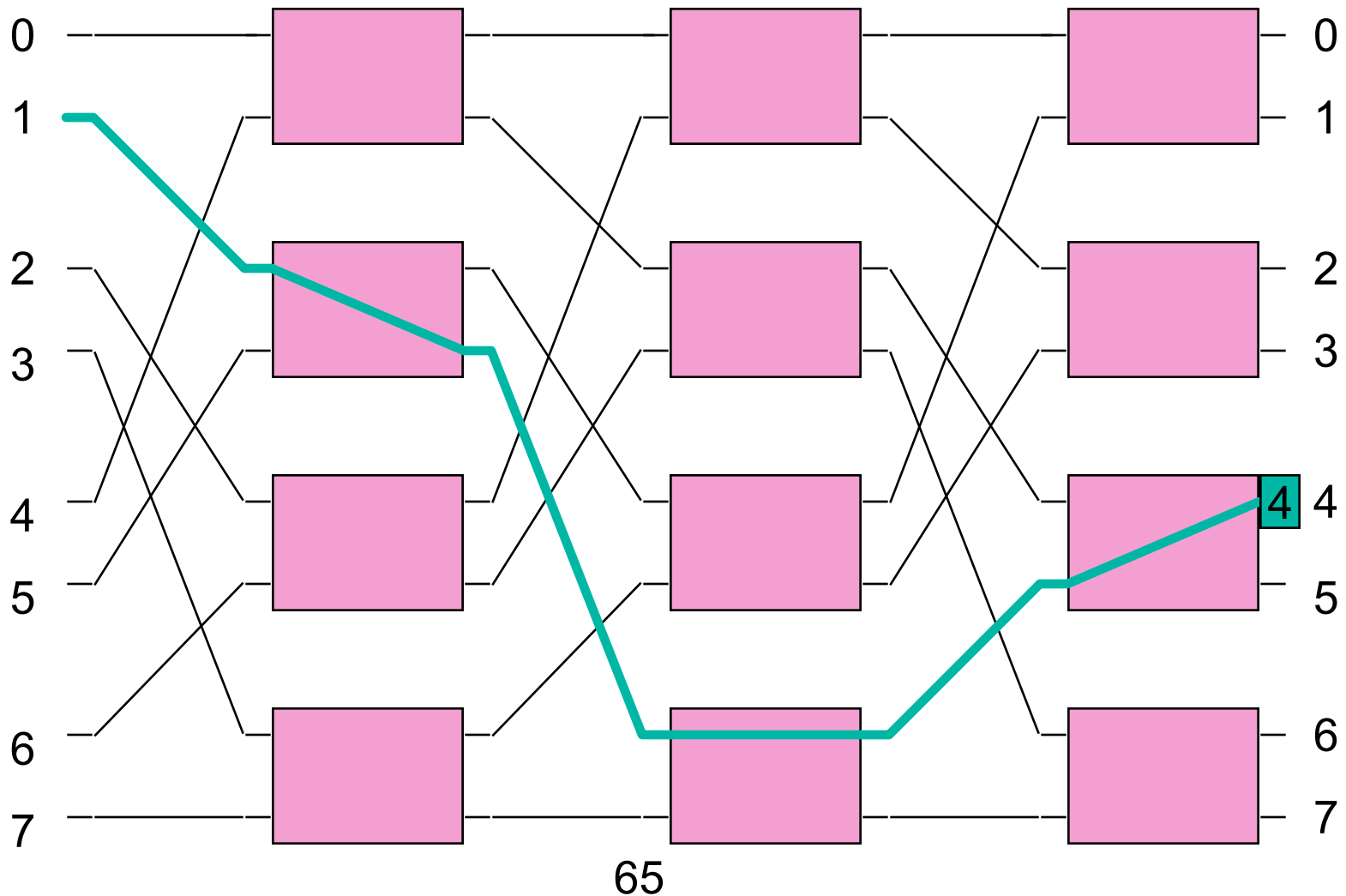
# Example of Self Routing

Cell destined for output port 4 ( $= 100_2$ )



# Example of Self Routing

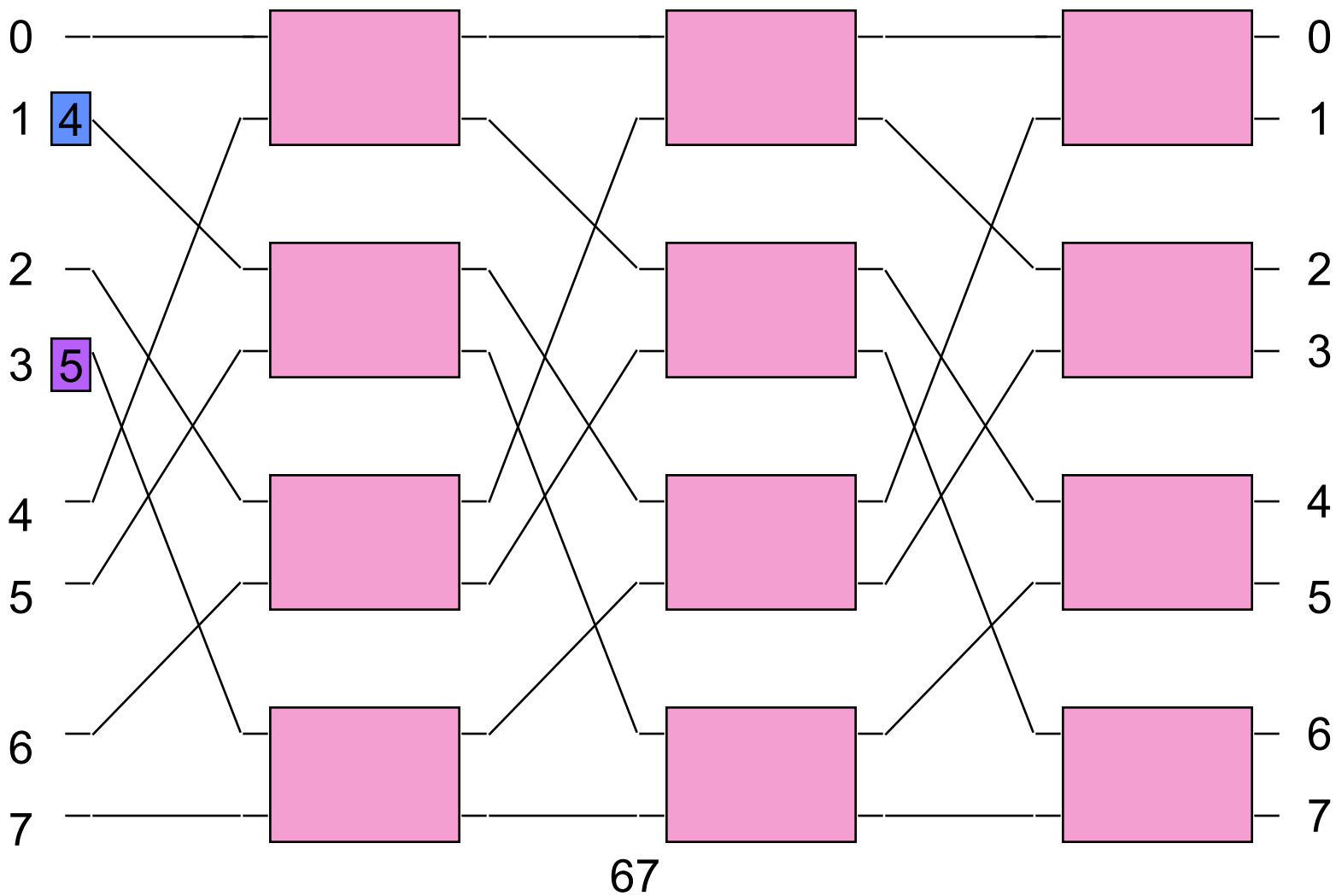
Cell destined for output port 4 ( $= 100_2$ )



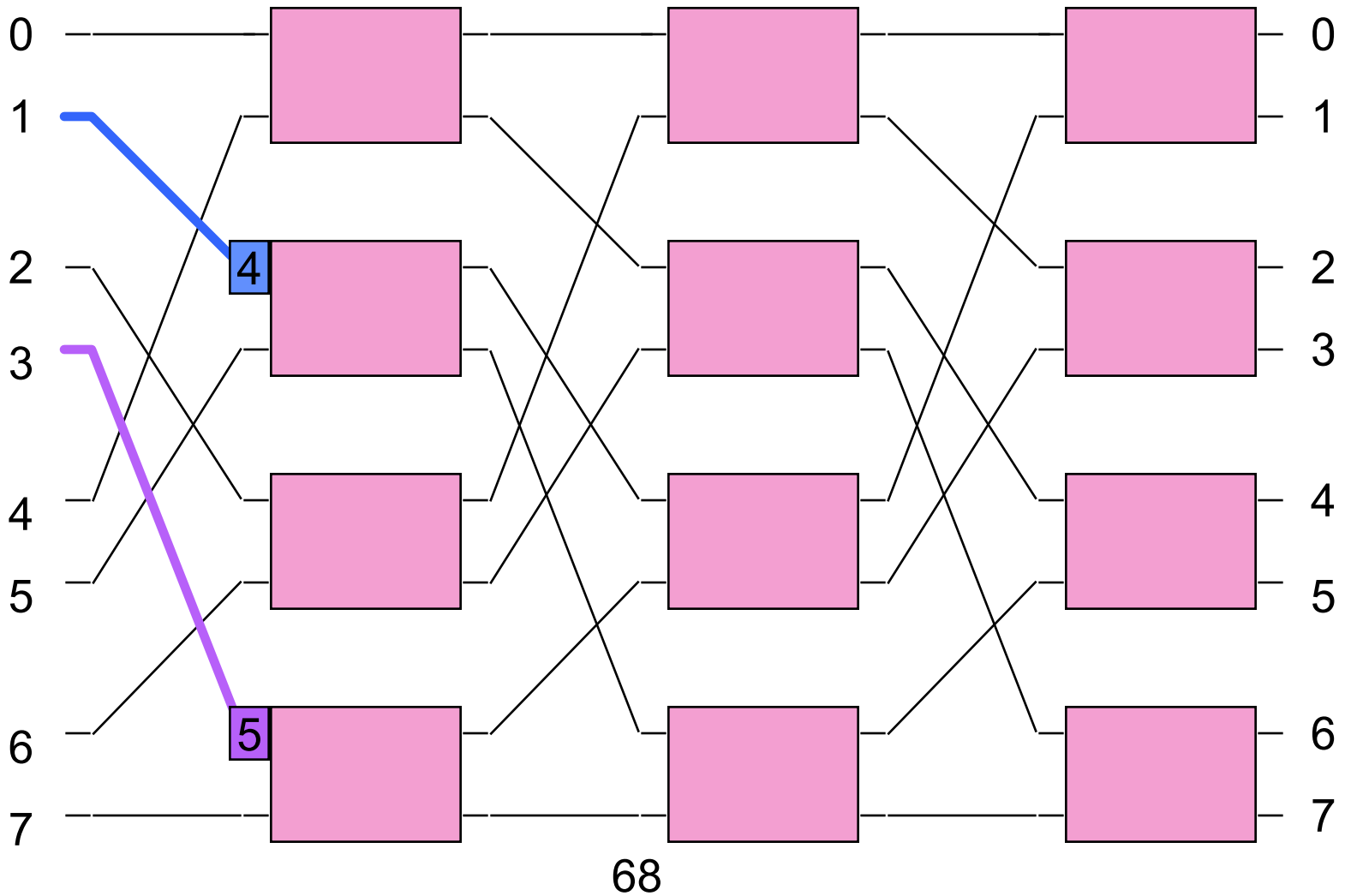
# Path Contention

- The omega network has the problems as the delta network with output port contention and path contention
- Again, the result in a bufferless switch fabric is cell loss (one cell wins, one loses)
- Path contention and output port contention can seriously degrade the achievable throughput of the switch

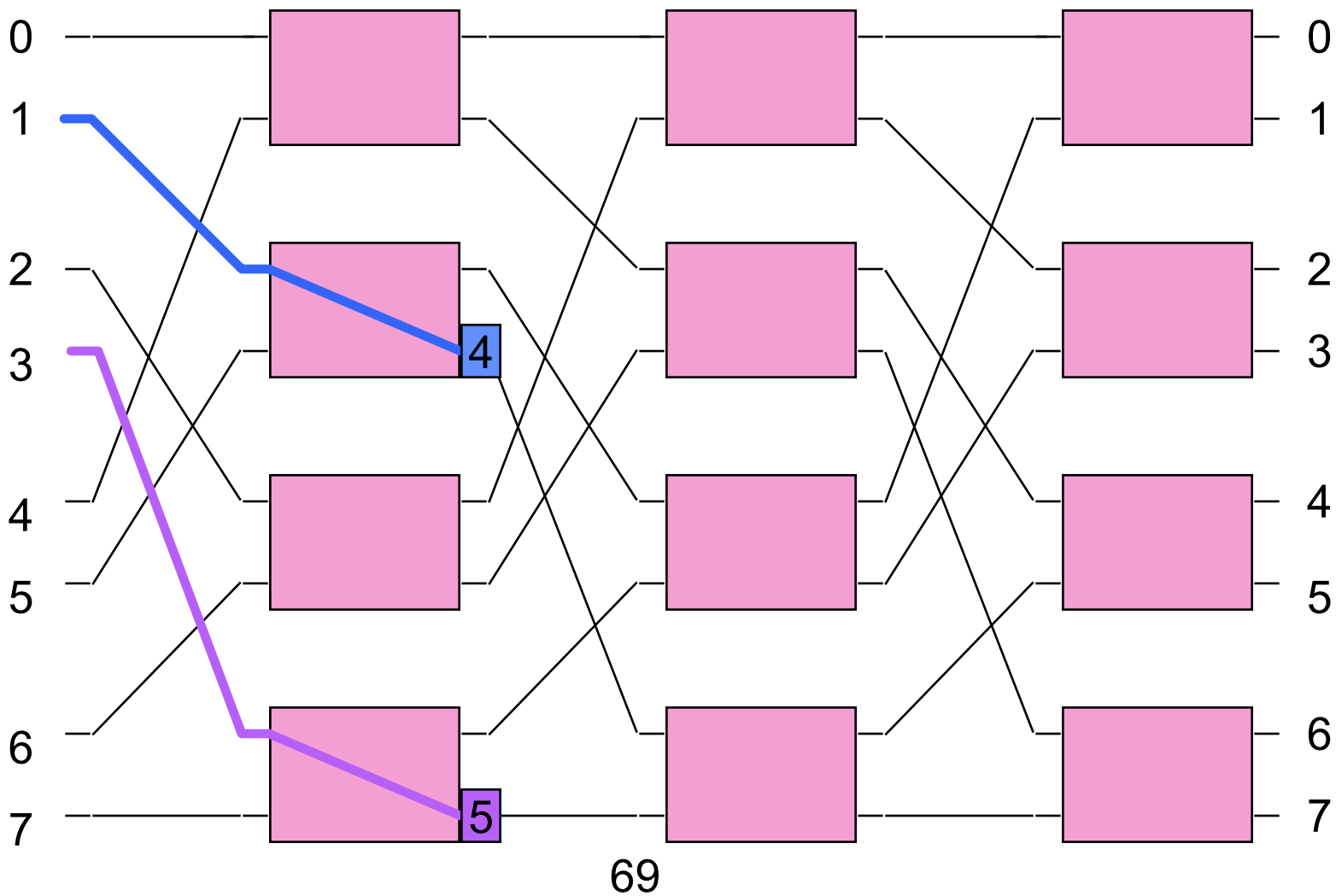
# Path Contention



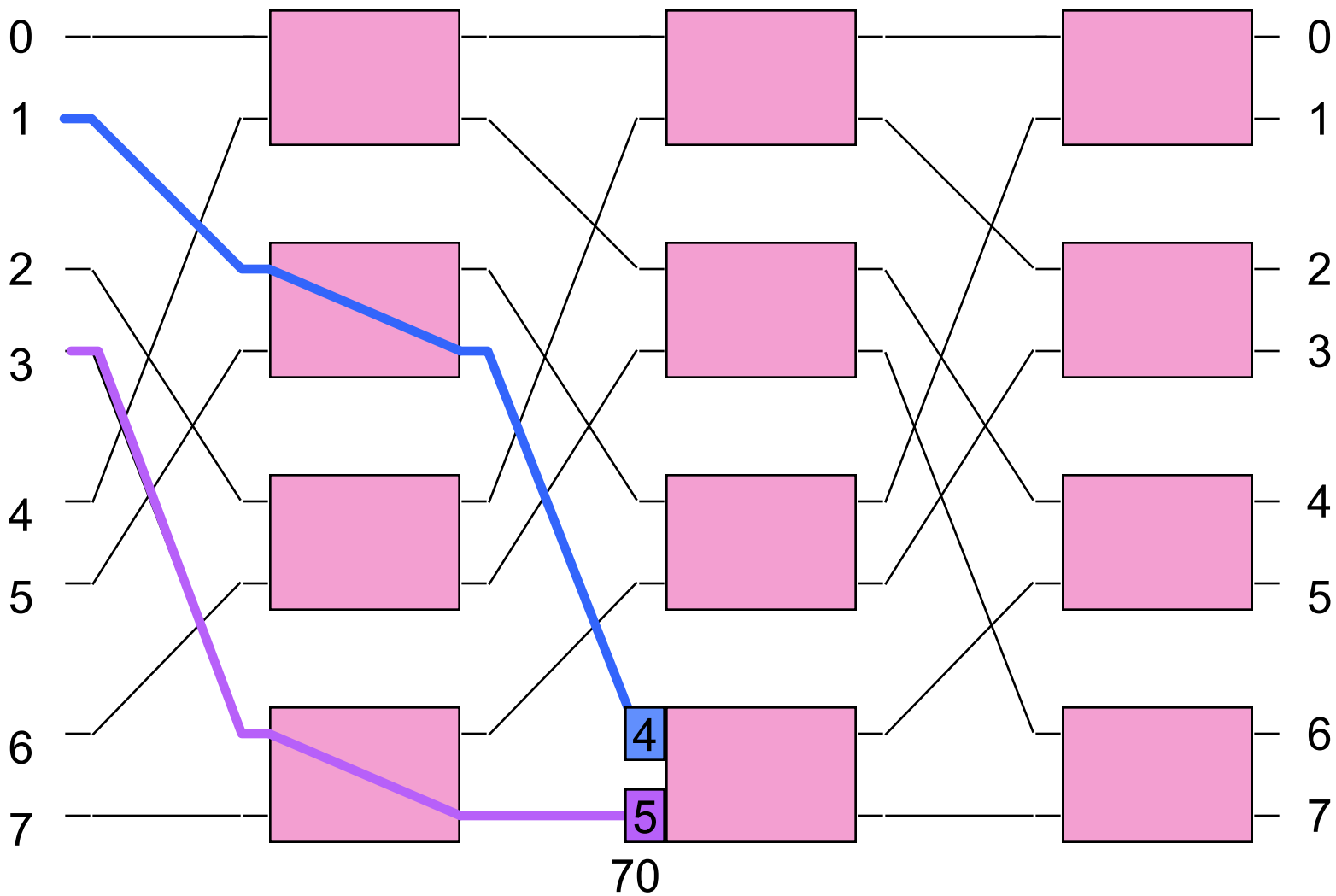
# Path Contention



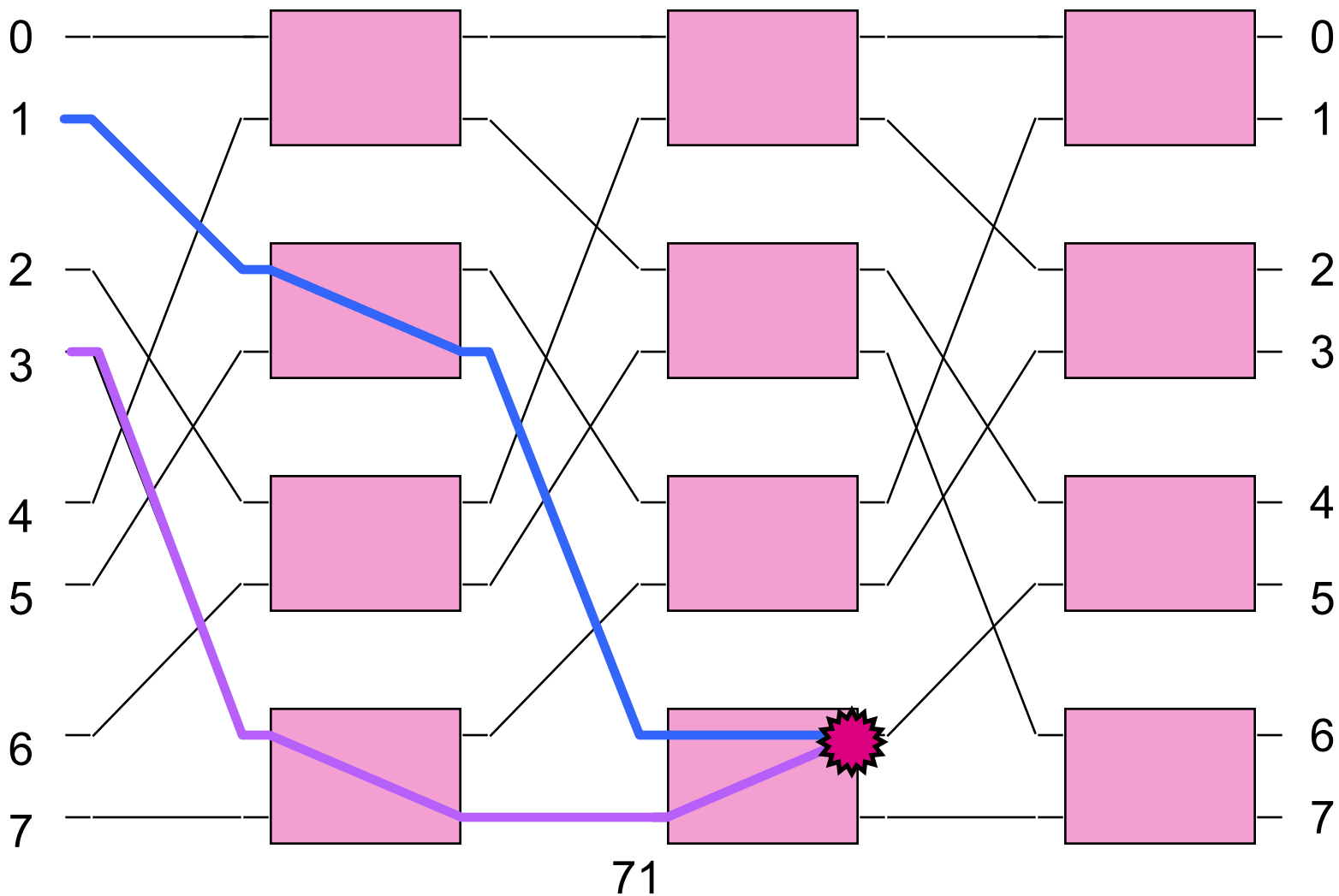
# Path Contention



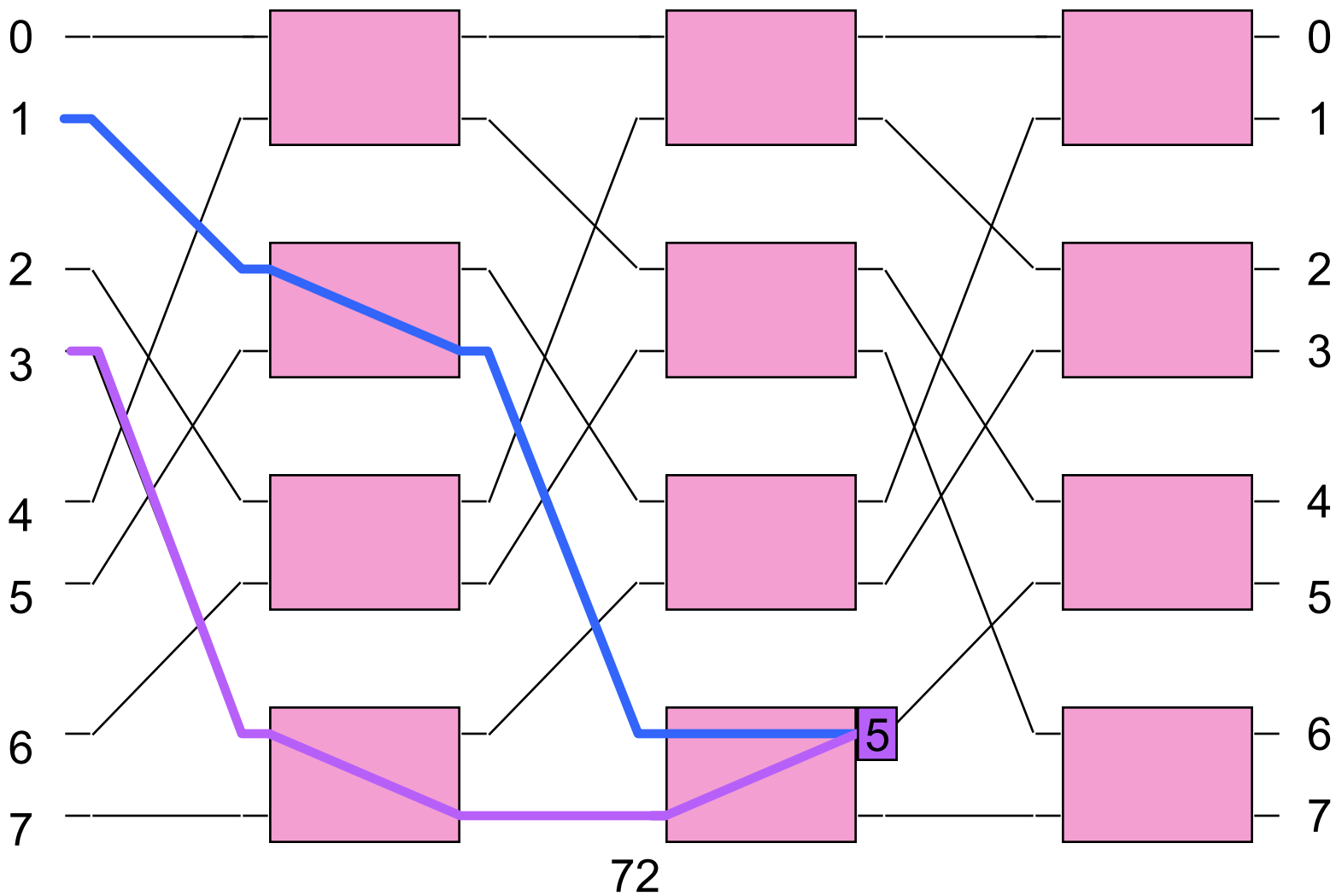
# Path Contention



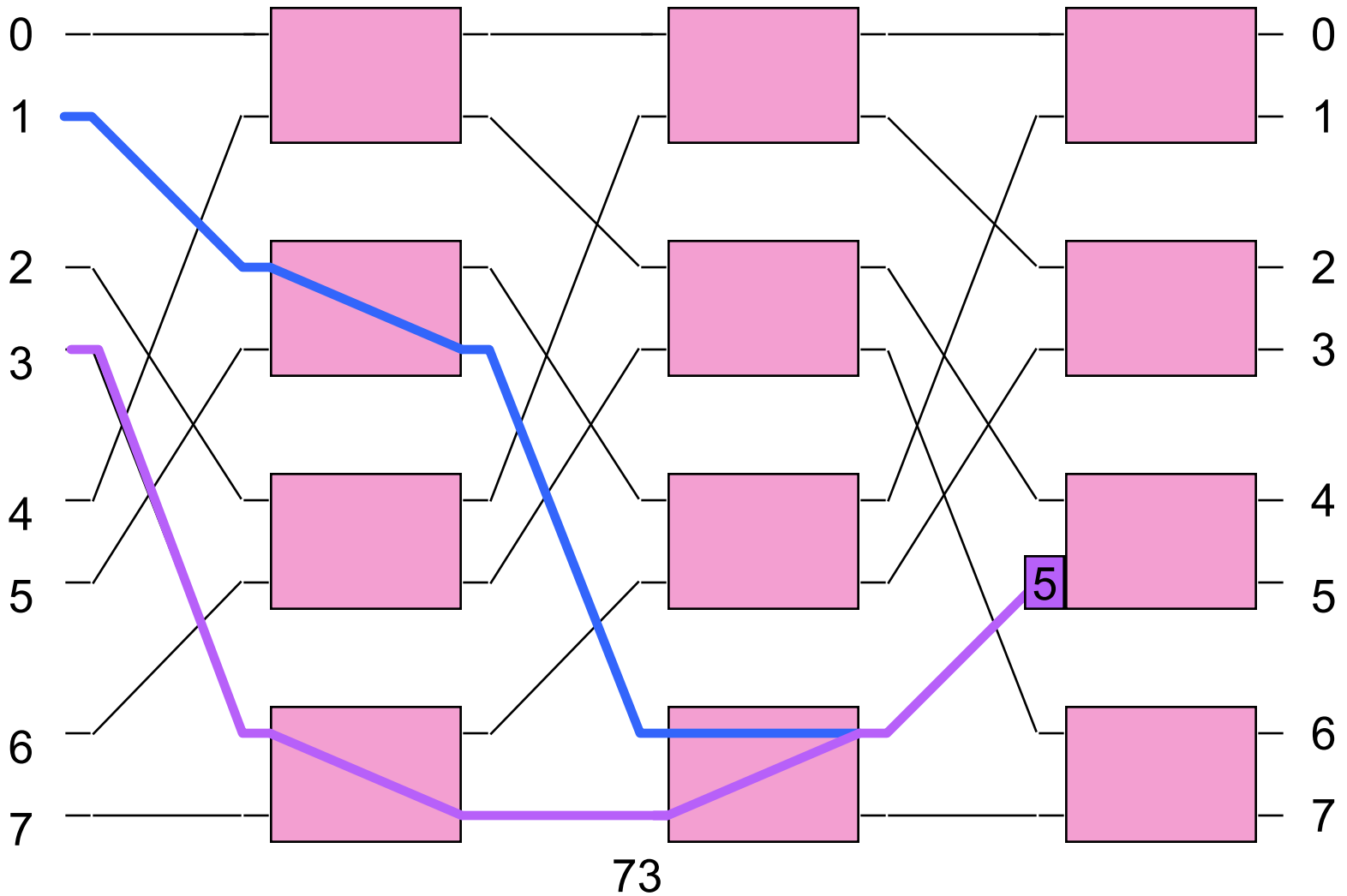
# Path Contention



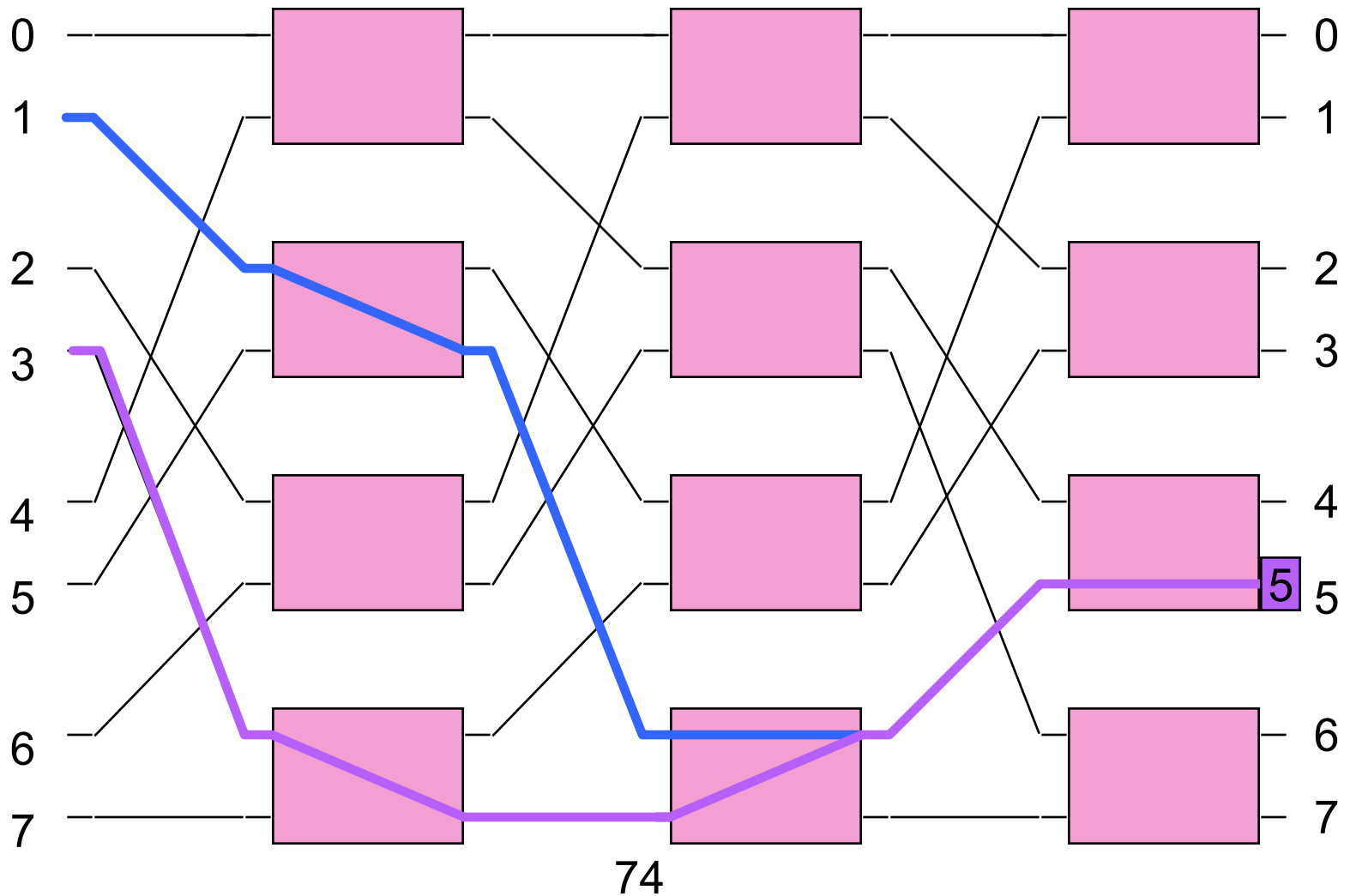
# Path Contention



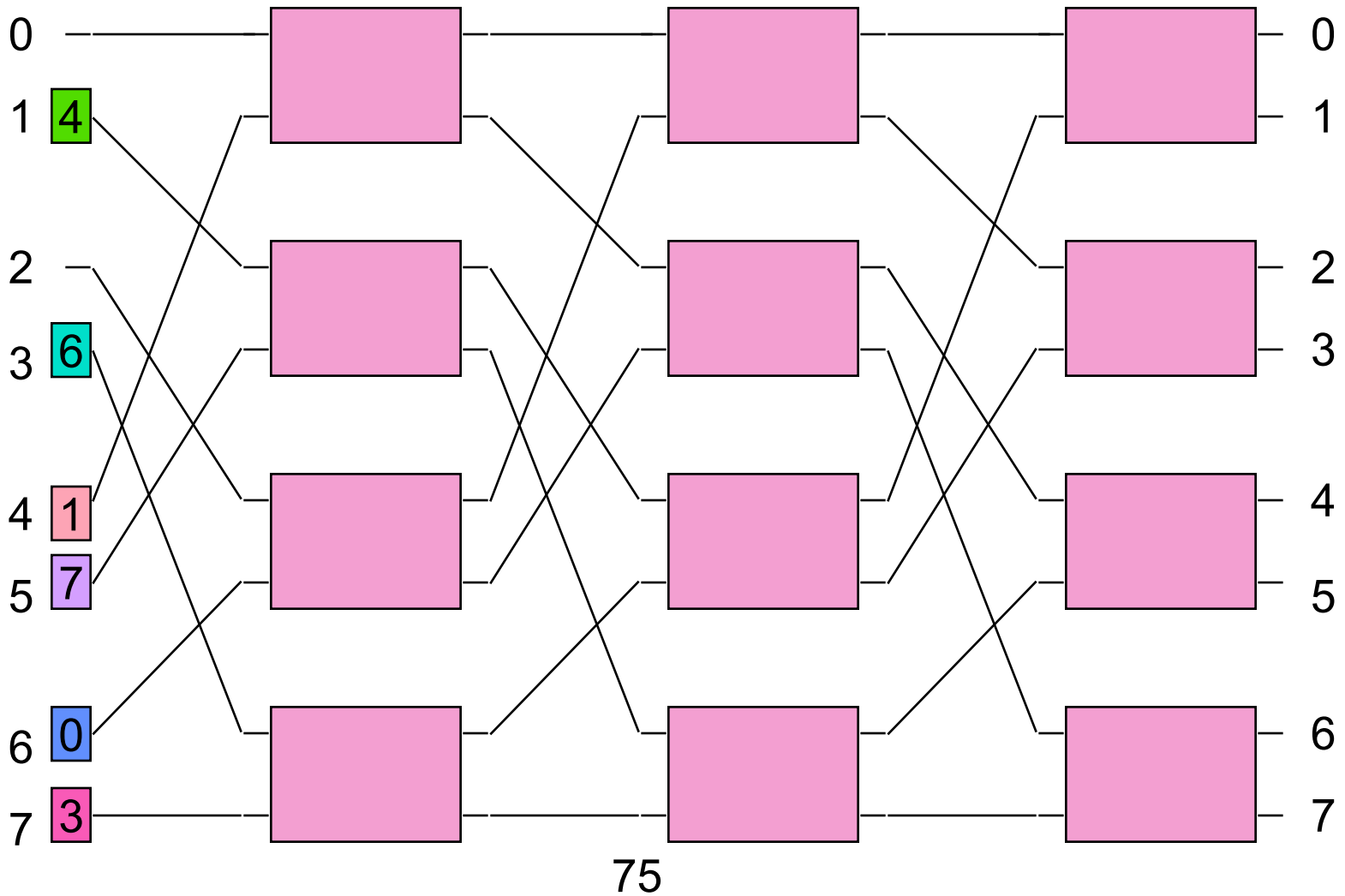
# Path Contention



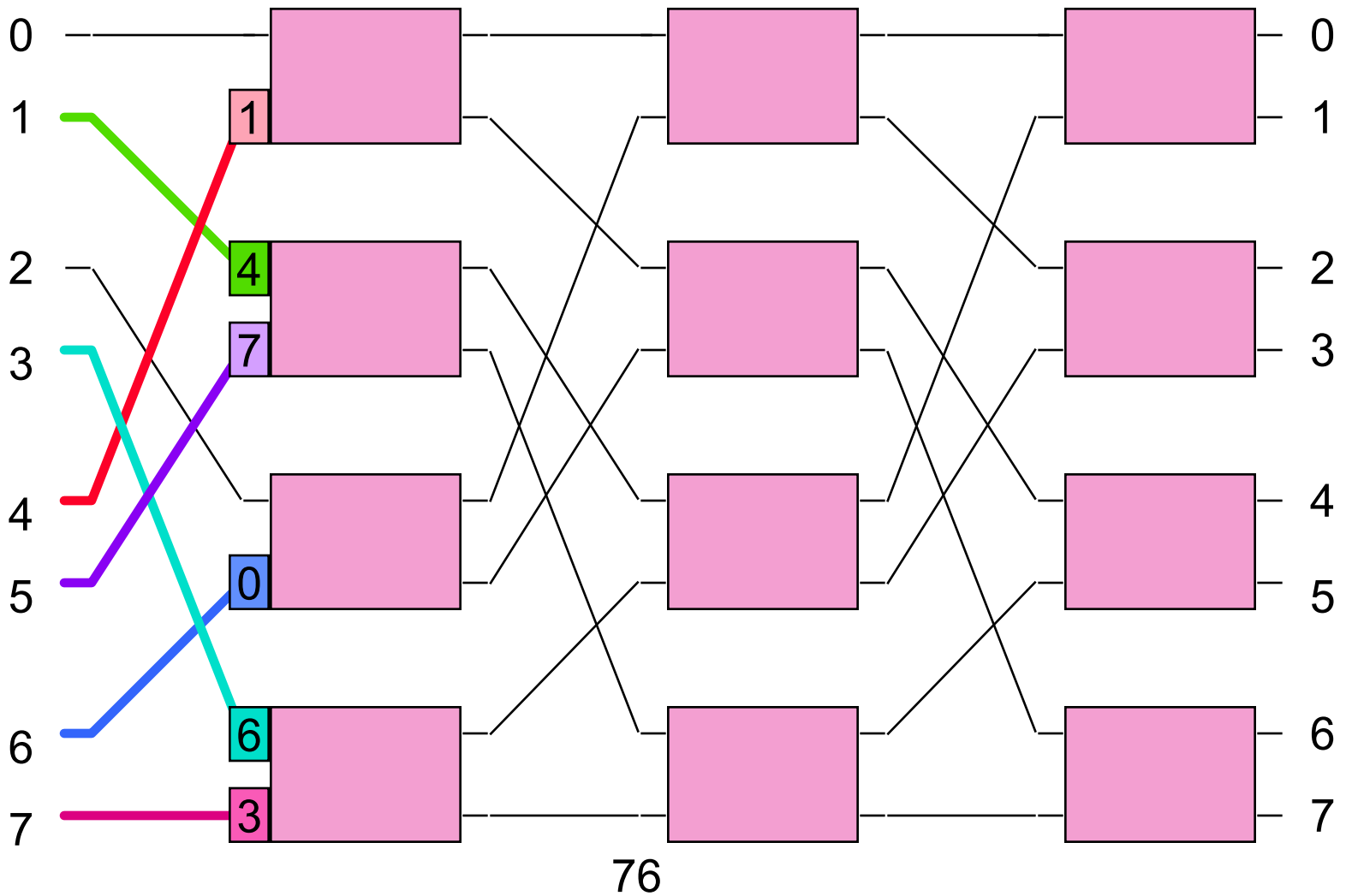
# Path Contention



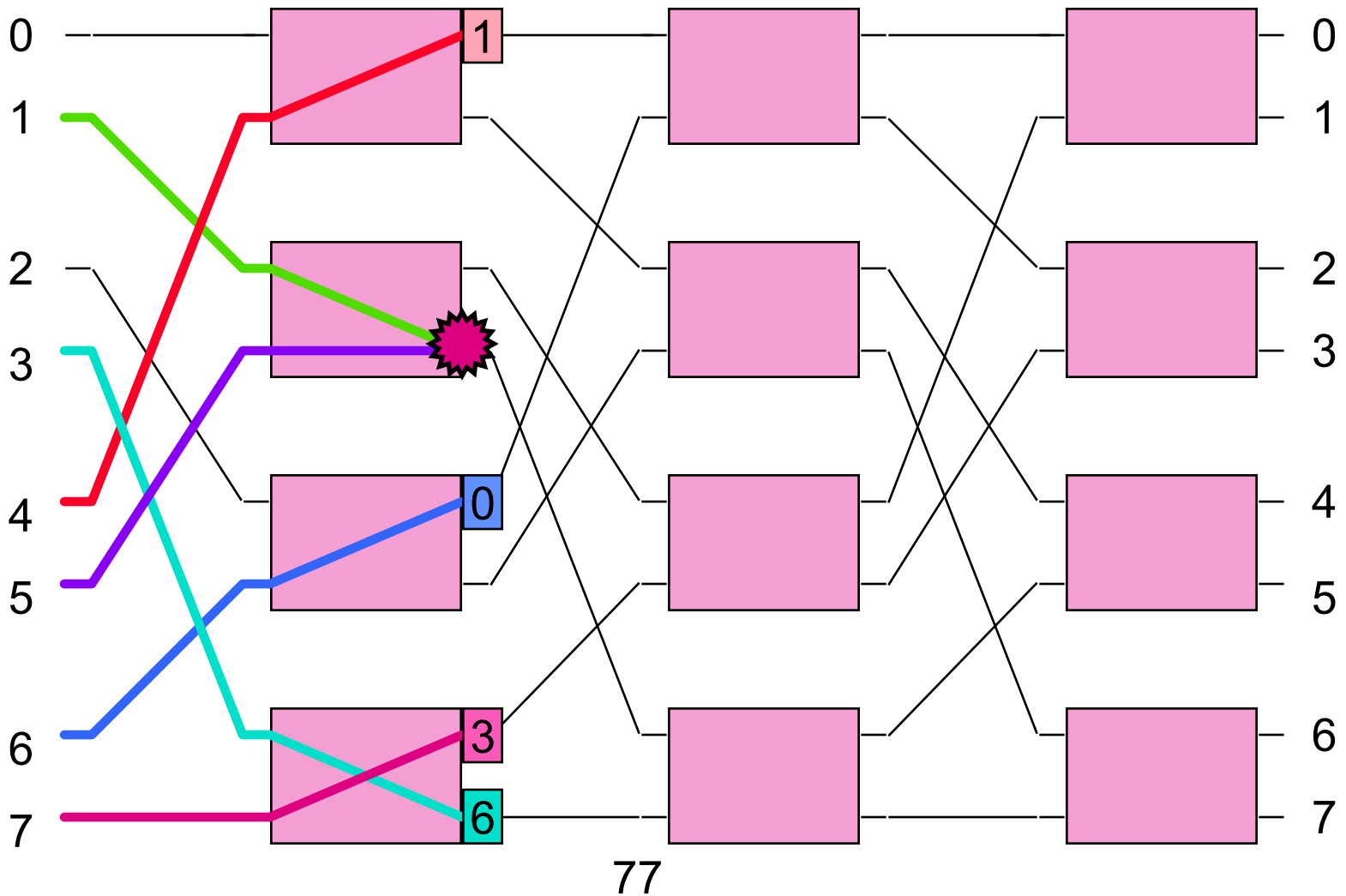
# Performance Degradation



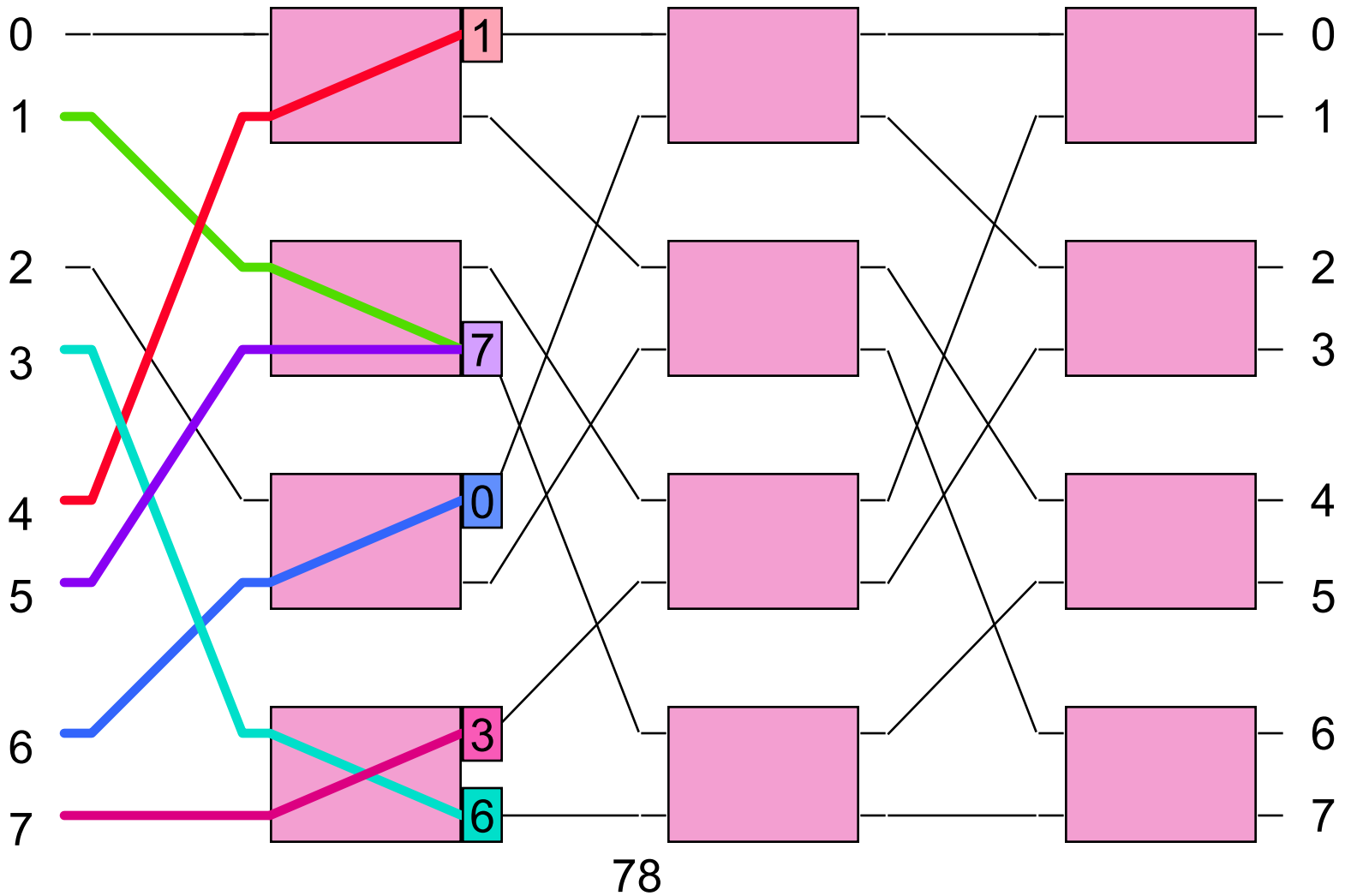
# Performance Degradation



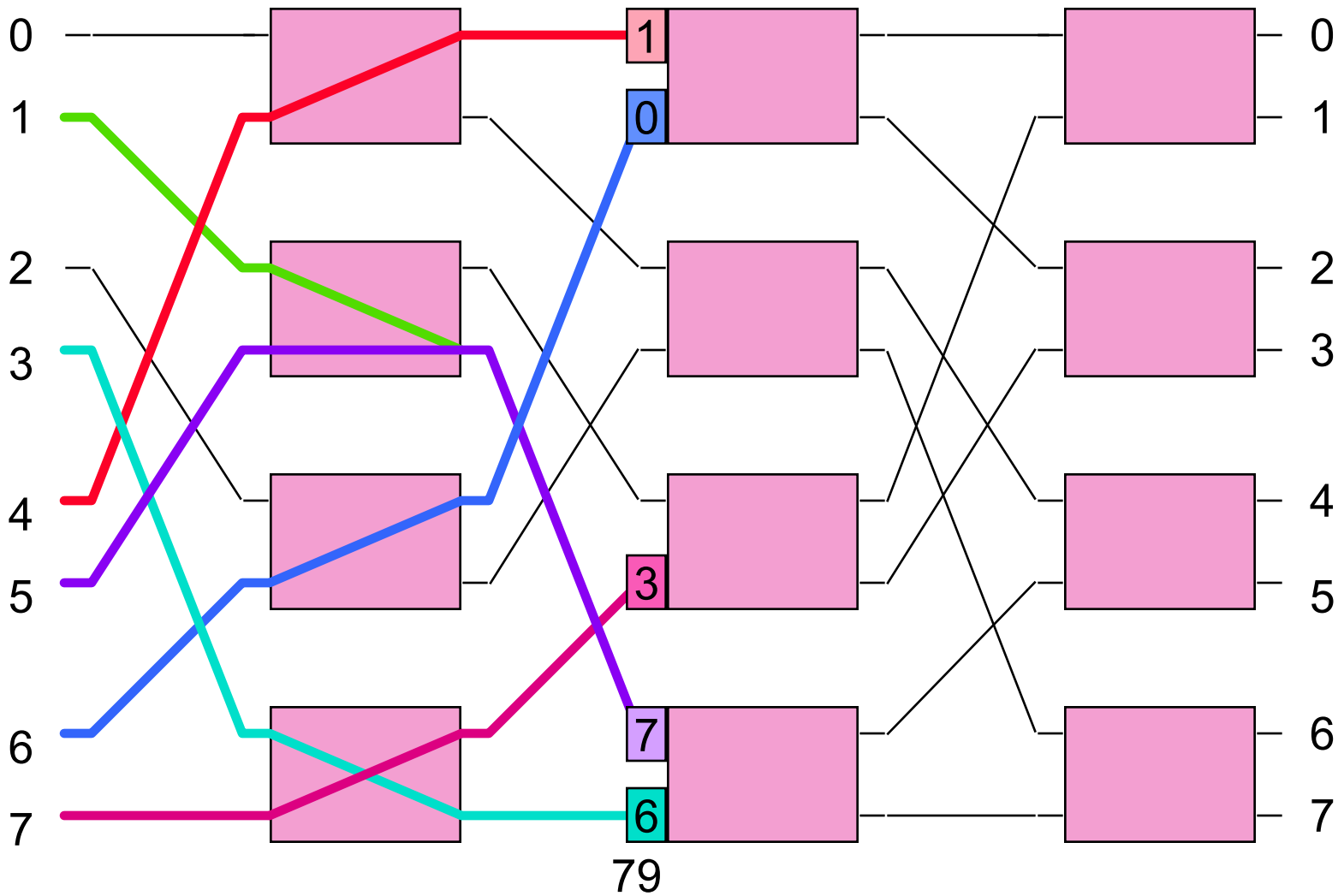
# Performance Degradation



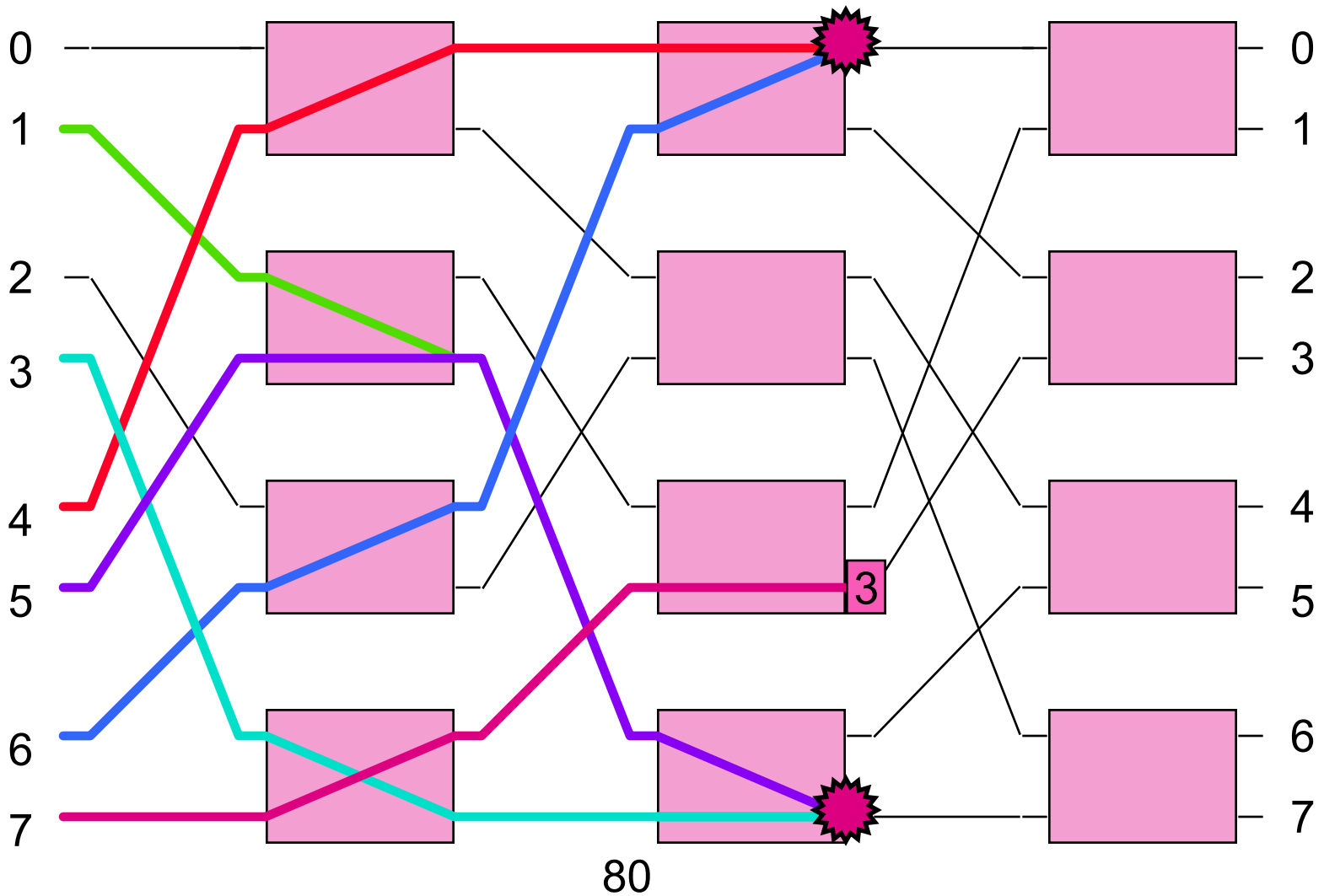
# Performance Degradation



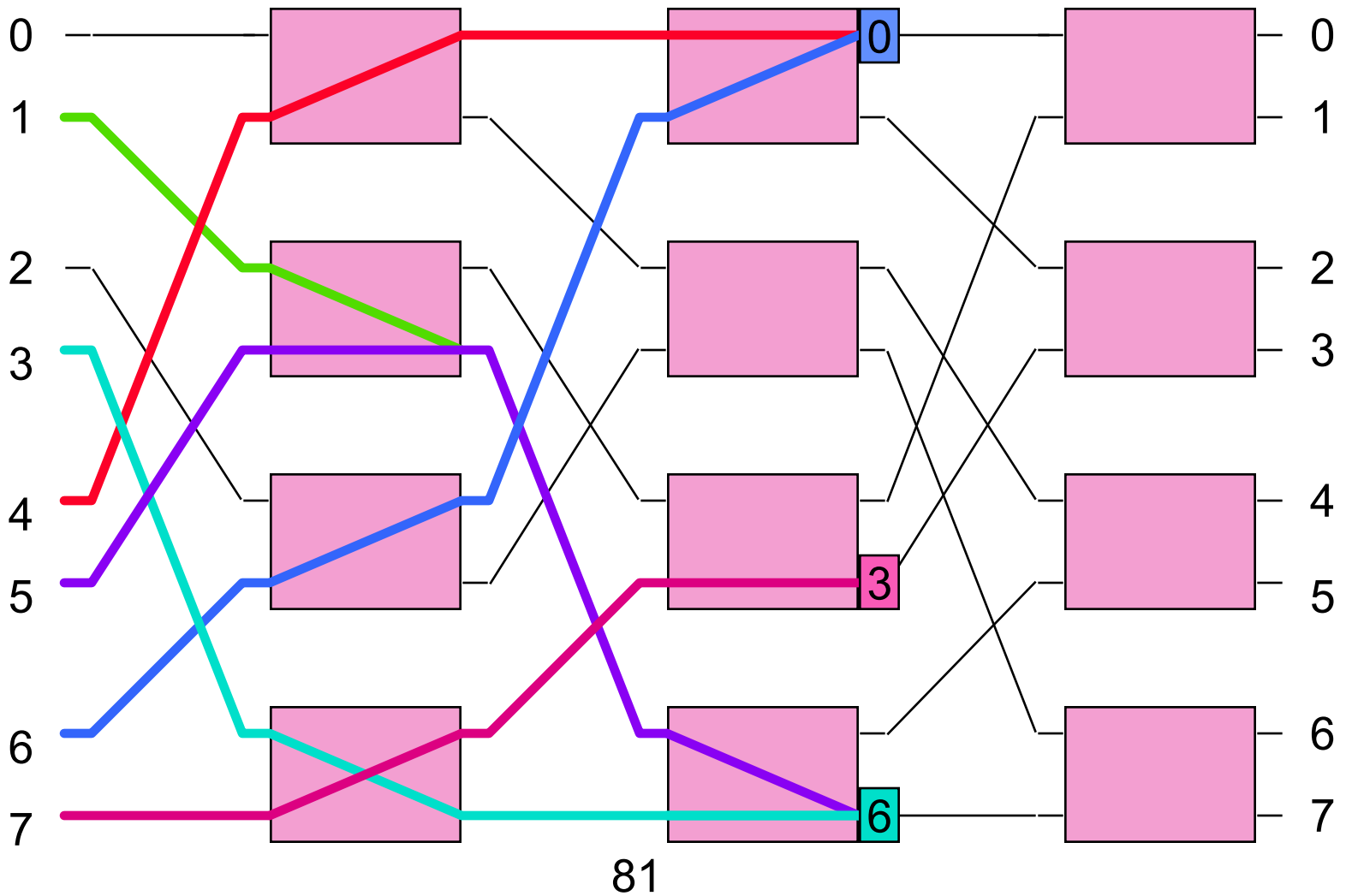
# Performance Degradation



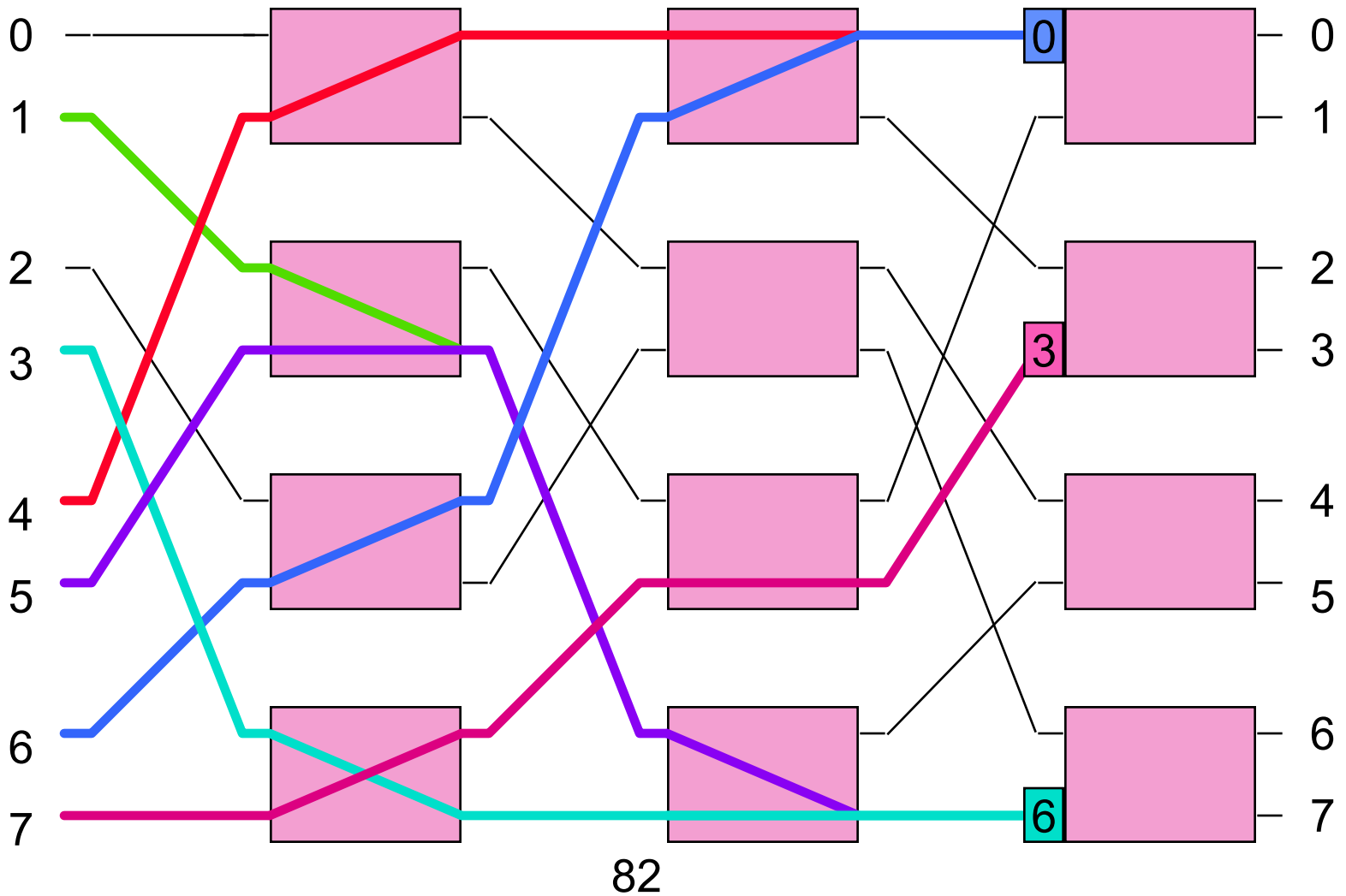
# Performance Degradation



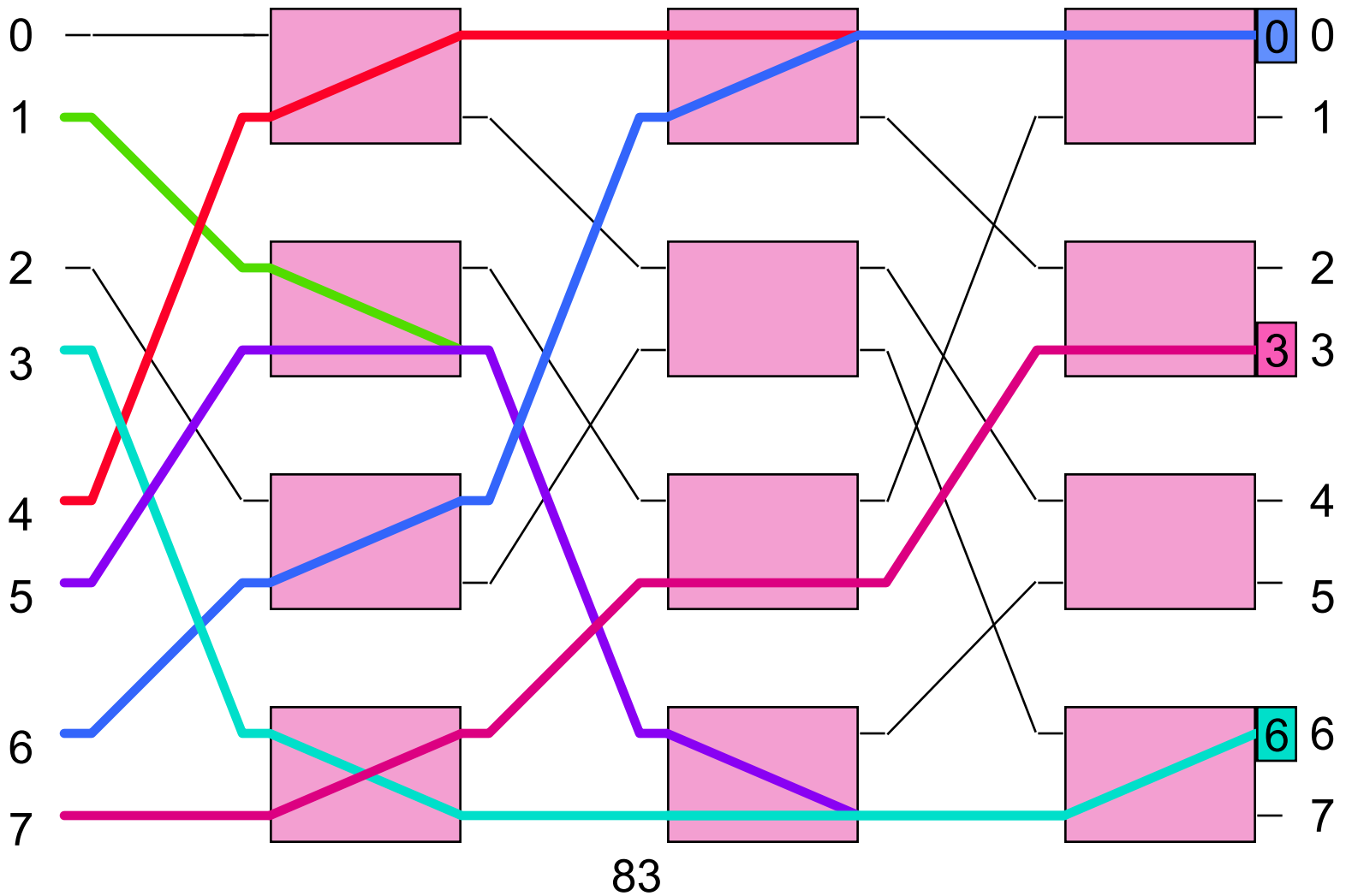
# Performance Degradation



# Performance Degradation



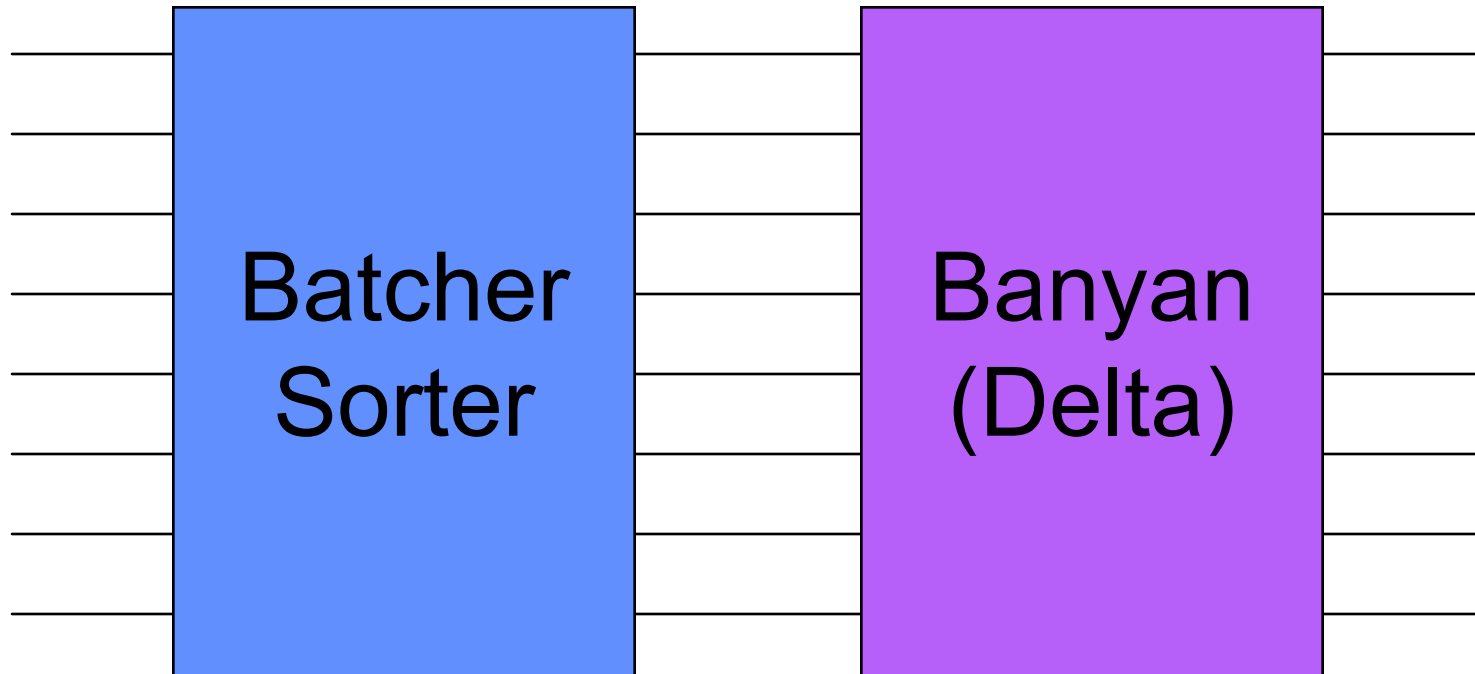
# Performance Degradation



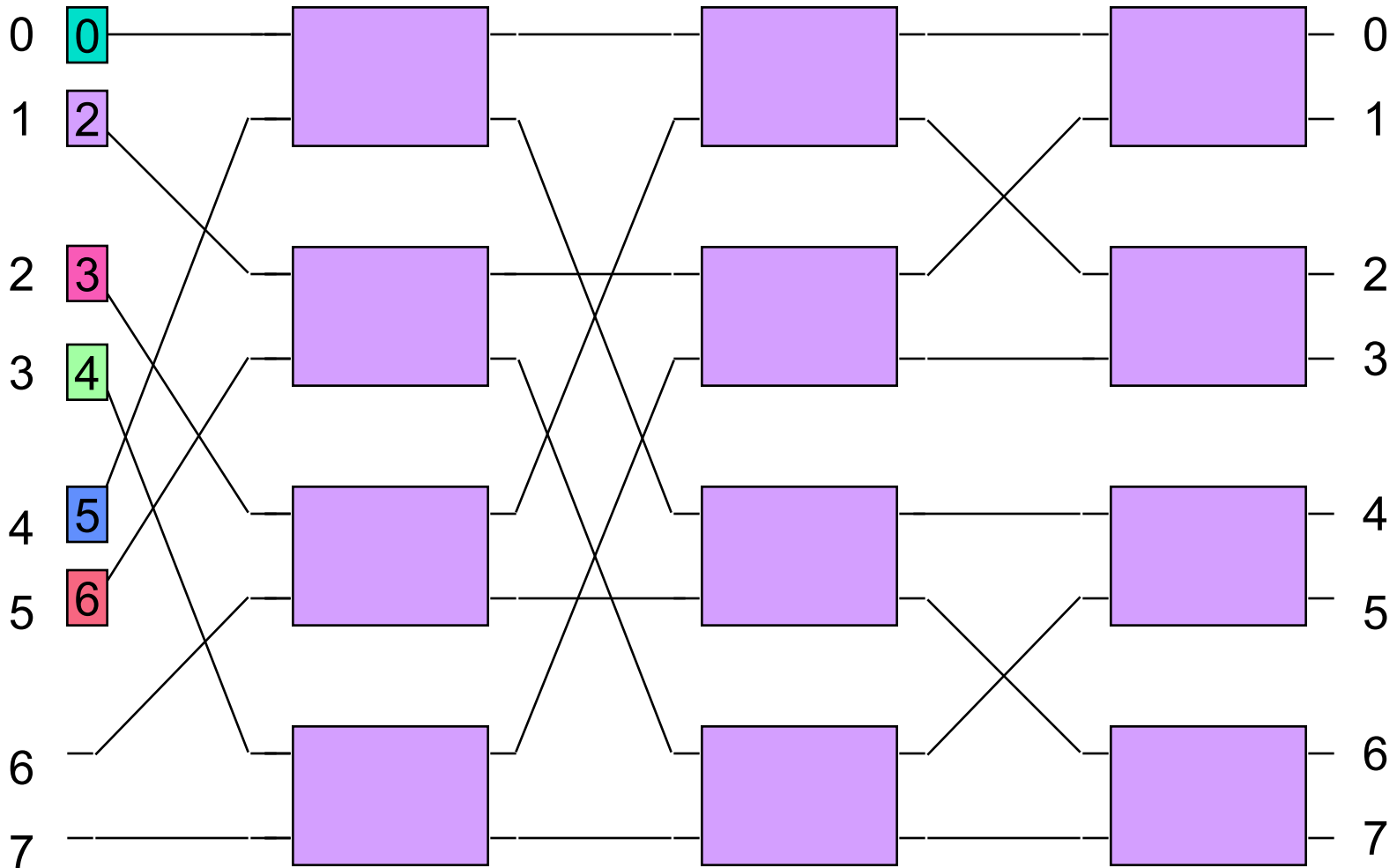
# A Solution: Batcher Sorter

- One solution to the contention problem is to sort the cells into monotonically increasing order based on desired destination port
- Done using a bitonic sorter called a Batcher
- Places the M cells into gap-free increasing sequence on the first M input ports
- Eliminates duplicate destinations

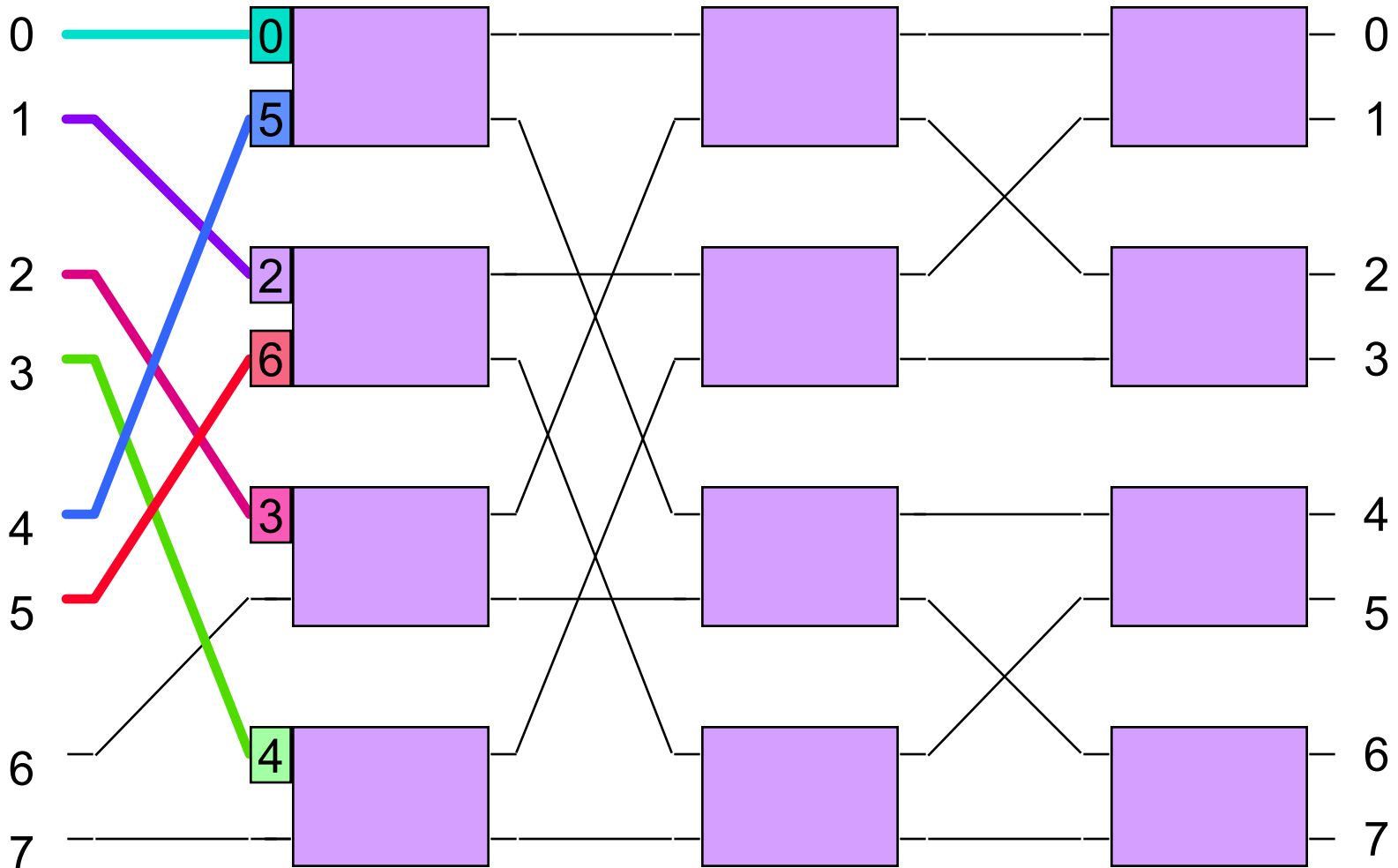
# Batcher-Banyan



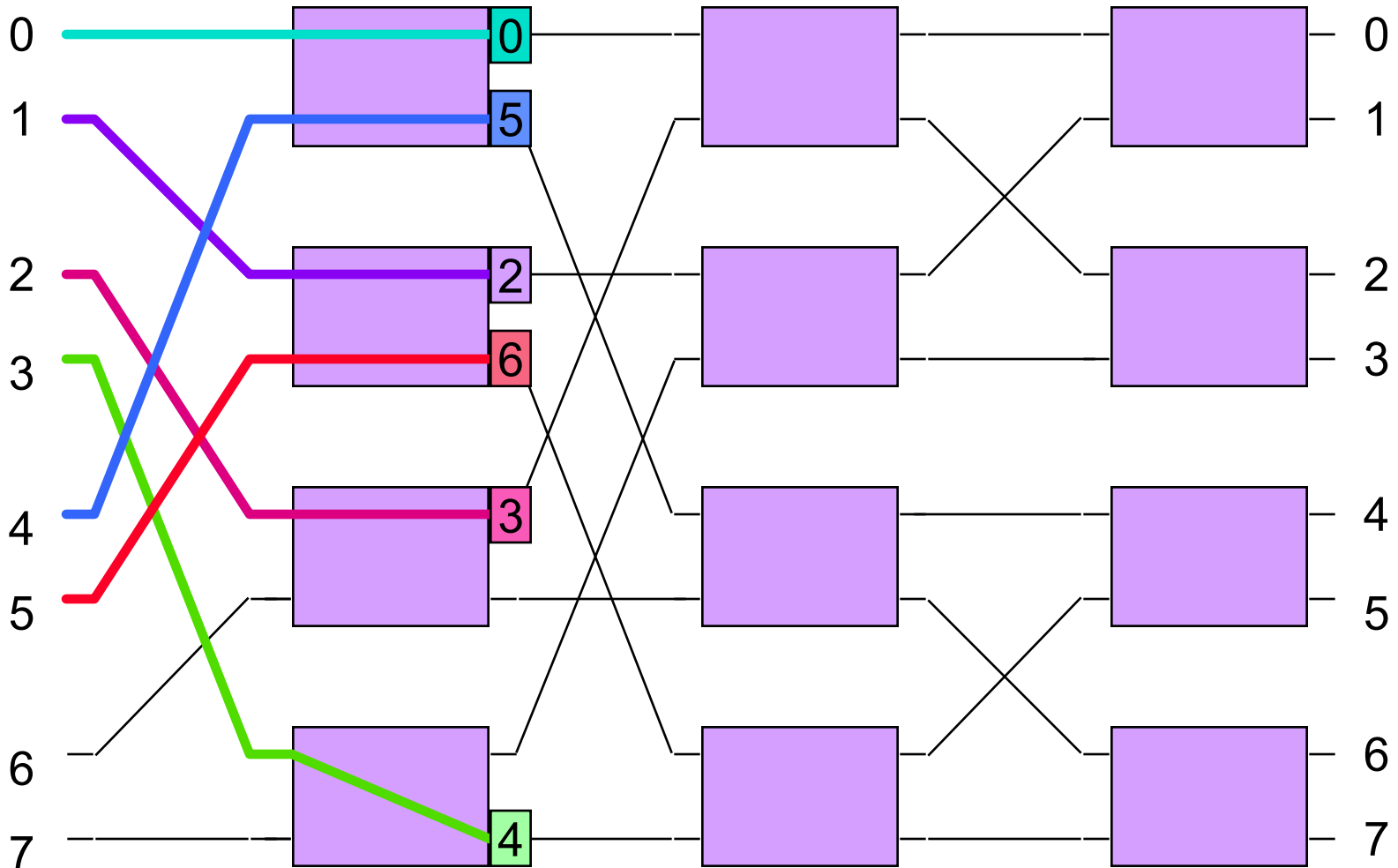
# Batcher-Banyan Example



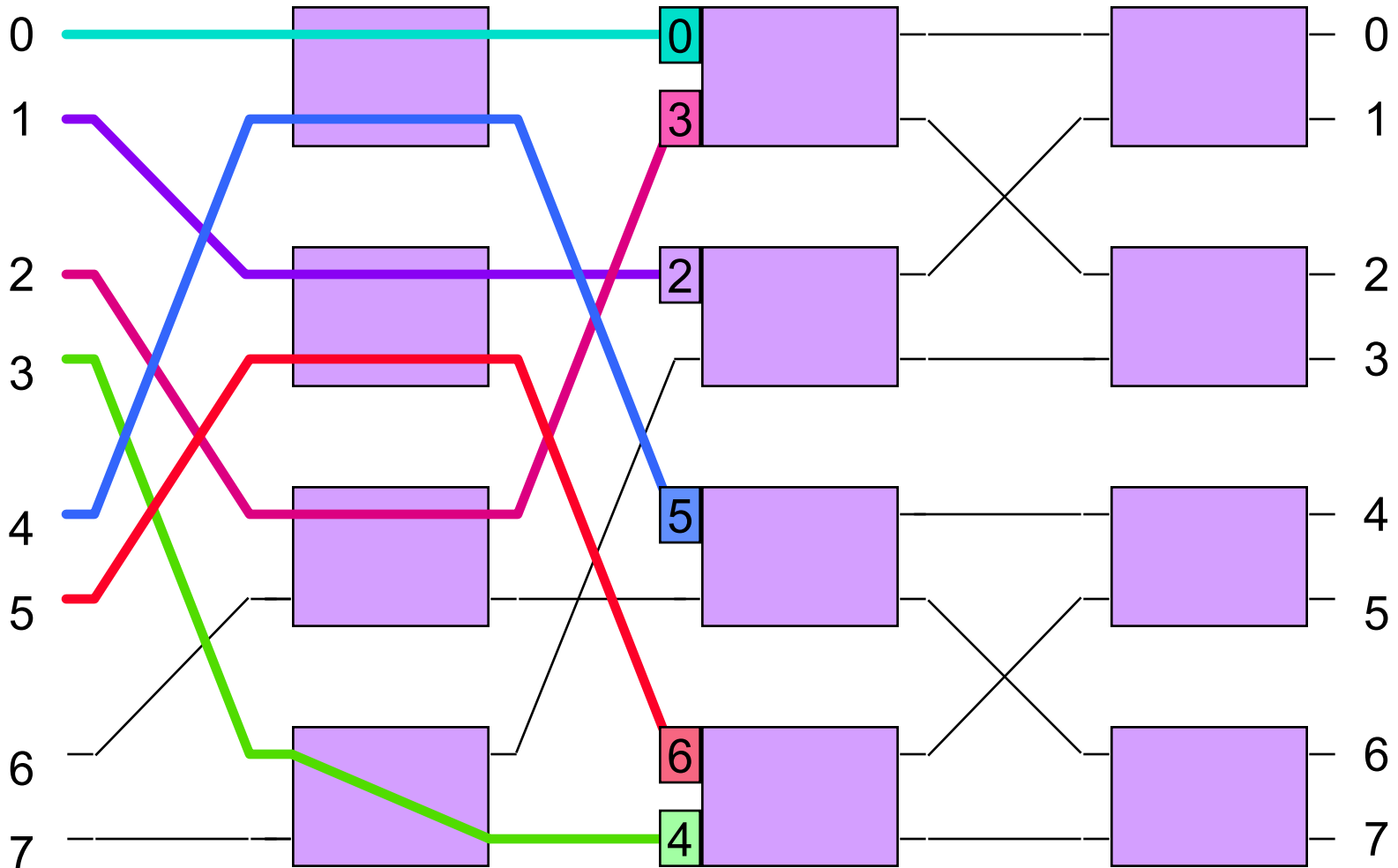
# Batcher-Banyan Example



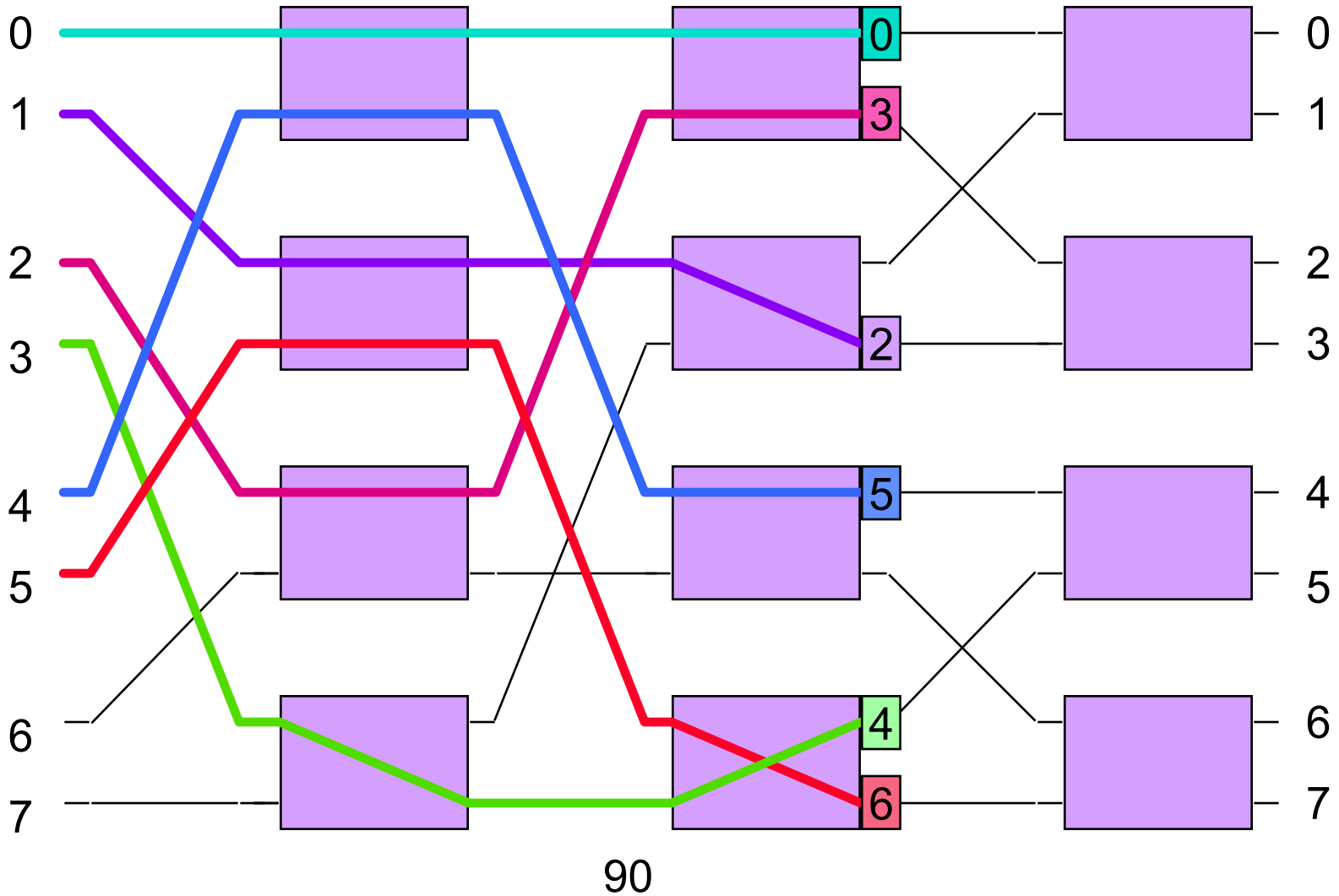
# Batcher-Banyan Example



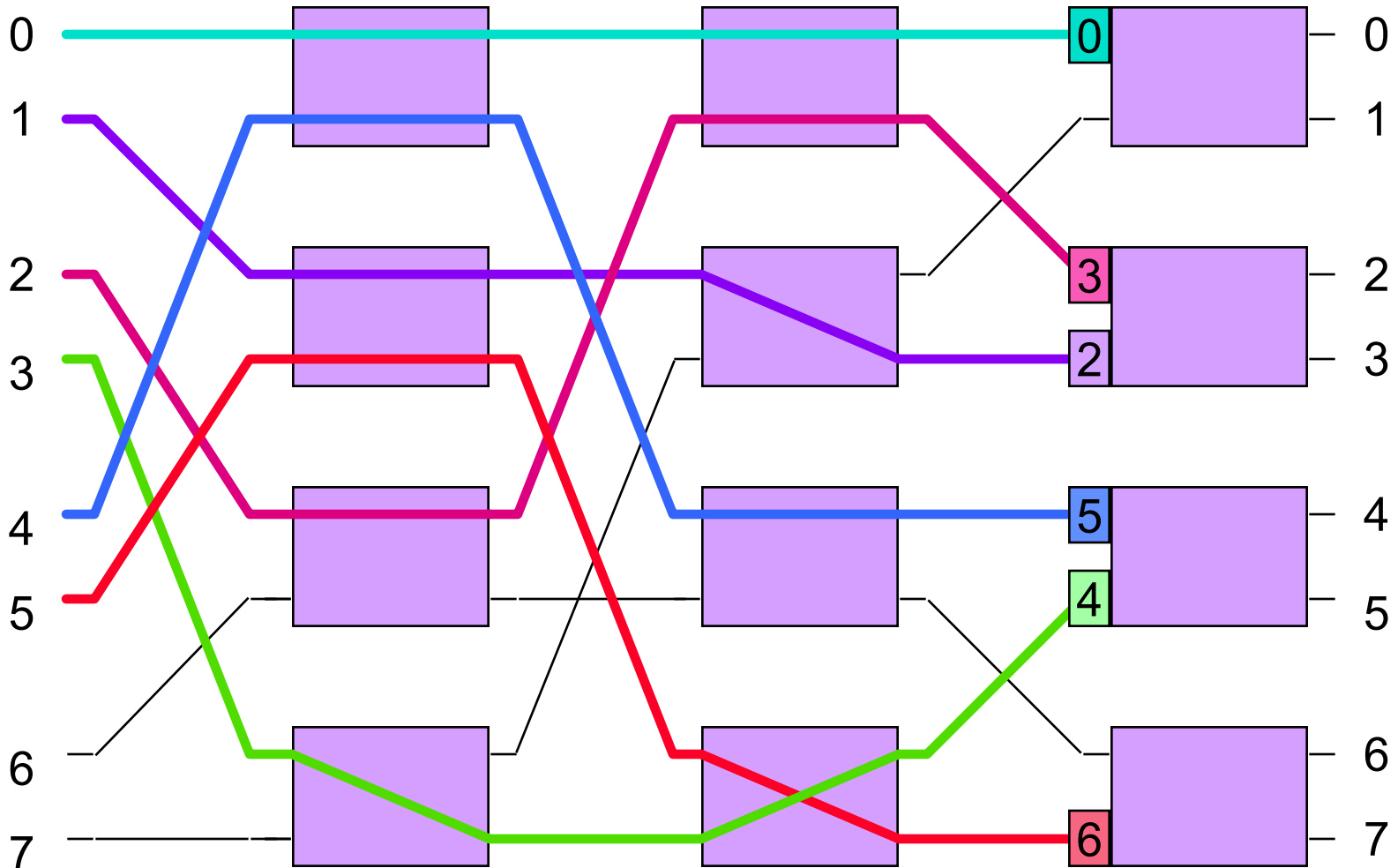
# Batcher-Banyan Example



# Batcher-Banyan Example



# Batcher-Banyan Example



# Batcher-Banyan Example

